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High Speed Back-Bias Voltage (VBB) Generator with Improved Pumping Current

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Abstract: Due to the advance of dynamic random access memory (DRAM) technologies with the steadfast increase of density with aggressively scaled storage capacitors, the supply voltage has been lowered to under 1 V to reduce power consumption. The above progress has been accompanied by the increasingly difficult task of sensing cell data reliably. One of the essential methods to preserve sustainable data retention characteristic is to curtail the sub-threshold leakage current by using a negative voltage bias for the bulk of access transistors. This negative back-bias is generated by a back-bias voltage generator. This paper proposes a novel high-speed back-bias voltage (VBB) generator with a cross-coupled hybrid pumping scheme. The conventional circuit uses one fixed voltage to control the gates of discharge of the p-channel metal oxide semiconductor (PMOS) and transfer n-channel metal oxide semiconductor (NMOS), respectively. However, the proposed circuit adds an auxiliary pump, thereby able to control more aptly with a lower negative voltage when discharging and a higher positive voltage when transferring. As a result, the proposed circuit achieves a faster pump-down speed and higher pumping current at a lower supply voltage compared to conventional circuits. The H-simulation program with integrated circuit emphasis (HSPICE) simulation results with the Taiwan semiconductor manufacturing company (TSMC) 0.18 um process technology indicates that the proposed circuit has about a 20% faster pump-down speed at a supply voltage of voltage common collector (VCC) = 1.2 V and about 3% higher pumping current at VBB from −0.6 V to −1 V with the ability to generate a near 3% higher ratio of |VBB|/VCC at VCC = 0.6 V compared to conventional circuits. Hence, the proposed circuit is extremely suitable and promising for future low-power and high-performance DRAM applications.

Keywords: charge pump; low-voltage generator; DRAM circuit; NEGATIVE voltage generator; back-bias voltage (VBB) generator

1. Introduction

As semiconductor technology advances rapidly, dynamic random access memory (DRAM) density is escalating aggressively. The DRAM storage capacitor retaining data is getting smaller, and it is becoming increasingly difficult to sense the data reliably with very small charges in the storage node. To tackle this issue, the cell sub-threshold leakage current in DRAM depicted in Figure 1 should be eradicated or maintained at the very minimum to ensure long-cycled, power-saving operations in DRAM. To serve this purpose, back-bias voltage (VBB) generation technique has been used in high density DRAM technology. With back-bias voltage, the junction capacitance is reduced, cut-off characteristics of the access transistors are improved, and the device isolation and latch-up endurance are enhanced [1–4]. A back-bias voltage generator with a faster speed and improved current drivability is needed for future DRAM technology [5,6]. Based on the previously researched VBB generator circuits in which a cross-coupled hybrid pumping circuit with auxiliary pump [2,5,7] is used to make the circuits operate at high-speed and without threshold voltage loss, our work also adapts this cross-coupled

hybrid pumping circuit structure. However, different from previous works [2,5,7], the proposed circuit adds an auxiliary pumping unit to control the gates of discharge PMOS and transfer NMOS, respectively, with a lower negative voltage when discharging and a higher positive voltage when transferring. This scheme makes the back-bias voltage generator achieve the target voltage faster and sustain the higher pumping current especially under very low VBB voltage conditions. The three conventional circuits are introduced and discussed in Section 2. The structure and operation of the proposed circuit is discussed in Section 3. The H-simulation program with integrated circuit emphasis (HSPICE) simulation results are presented in Section 4 with the performance attributes of the pump-down speed, the |VBB|/VCC ratio, and the pumping current as a function of VBB. Finally, the conclusion is made in Section 5.

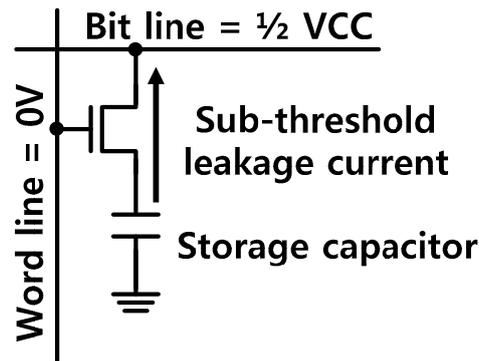**Figure 1.** A subthreshold leakage current in the dynamic random access memory (DRAM) access transistor.

2. Conventional VBB Generation Circuits

2.1. Conventional Cross-Coupled Hybrid Pumping Circuit (Conv 1)

To produce a negatively biased voltage, VBB generator circuits in various structures using a NMOS system or a PMOS system with a hybrid pumping circuit (HPC) have been proposed. However, there still have been problems of sacrificial threshold voltage loss of NMOS and PMOS transistors, respectively. Also, these problems cause reductions in the pump-down speed and the efficiency of the circuits [8,9]. To overcome these shortcomings, a cross-coupled configuration with origin in the voltage doubler [10] was applied in the cross-coupled hybrid pumping circuit 1 (CHPC1) [2]. This circuit which is to be referred to as Conv 1 in this paper is depicted in Figure 2. Conv 1 consists of two pumping capacitors, one load capacitor, four transistors, and two anti-phase clock signals. The four transistors include the transfer transistors (MN1 and MN2) and are the discharge transistors (MP1 and MP2). The transfer transistors clamp the nodes between the node N_{VBB} and the node N1 or N2. The discharge transistors discharge the charges from the nodes N1 and N2. The gates of MN1 and MP1 are controlled by N2 and the gates of MN2 and MP2 are controlled by N1. The sequential operation for Conv 1 is described in Table 1. In the first phase, the initial voltage at N2 (V_{N2}) is initially as high as the supply voltage VCC because of the capacitive coupling from the capacitor C2. The voltage on the gate of MP2 is 0 V because of capacitive coupling, so MP2 is turned on and the voltage of the node N2 is $|V_{tp}|$ in which V_{tp} is its threshold voltage. In the second phase, the voltage of the node N2 is $|V_{tp}|-VCC$ and develops at the gate of MP1.
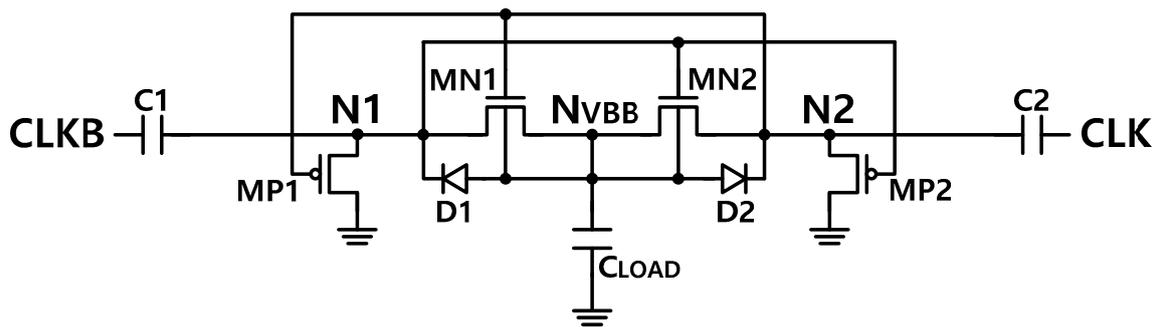
Figure 2. Conventional cross-coupled hybrid pumping circuit (Conv 1) [2].

Table 1. Sequential operation for the conventional circuit Conv1.

Phase	CLK	CLKB	MP1	MP2	MN1	MN2	V_{N1}	V_{N2}
1	High	Low	Off	On	On	Off	0	$\dfrac{VCC}{|V_{tp}|}$
2	Low	High	On	Off	Off	On	$\dfrac{VCC}{0}$	$|V_{tp}|-VCC$
3	High	Low	Off	On	On	Off	$-VCC$	$\dfrac{|V_{tp}|}{0}$
4	Low	High	On	Off	Off	On	0	$-VCC$
5	High	Low	Off	On	On	Off	$-VCC$	0

With MP1 turned on, the voltage of the node N1 turns from VCC to 0 V as the charges on the node N1 are discharged. As the voltage of the node N1 is fed into the gate of MN2, MN2 turns on and clamps the node N2 at the negative voltage for the node N_{VBB}. In the third phase, the voltage of the node N1 becomes −VCC from 0 V and this voltage fed into the gate of MP2 turns it on. So the voltage at N2 becomes 0 V from $|V_{tp}|$. After repetition of these procedures, the voltage at the node N_{VBB} becomes −VCC [2]. From the cross-coupled configuration of the scheme, the threshold voltage loss problem is solved. However, there is another problem that emerges from the cross-coupled structure. When MN1 or MN2 turns on, clamping the node N_{VBB}, reverse charge sharing from the node N_{VBB} to the node N1 or N2 occurs. This reverse charge sharing affects the controlling voltages at the gate of MP1 or MP2. So the pump-down speed, the pumping current, and the efficiency are reduced.

2.2. Conventional Cross-Coupled Hybrid Pumping Circuit (Conv 2)

Another back-bias voltage generator is the cross-coupled hybrid pumping circuit 2 (CHPC2) and this circuit is now referred to as Conv 2 [5]. Conv 2 is depicted in Figure 3. It also inherits the cross-coupled structure like Conv 1. Conv 2 consists of four pumping capacitors, six transistors, and two anti-phase clock signals. Two NMOS transistors, MN1 and MN2, are transfer transistors, and two PMOS transistors, MP1 and MP2, are discharge transistors. Two PMOS transistors, MP3 and MP4, compose an auxiliary pump unit. To solve the reverse charge sharing problem posed for Conv 1, Conv 2 uses the scheme that isolates the node, and clamps the node N_{VBB} to the other node that controls the gate of the discharge transistors. Without any charge sharing problem, the voltages of the nodes N3 and N4 supply −VCC for the gates of MP1 and MP2 in order to discharge the nodes N1 and N2. Also 0 V at the gates of MN1 and MN2 clamps the node N_{VBB} to the node N1 or N2, respectively. By using this structure, Conv 2 is able to get higher pump-down speed, pumping current, and efficiency compared to Conv 1 [5]. The sequential operation of Conv 2 is described in Table 2.
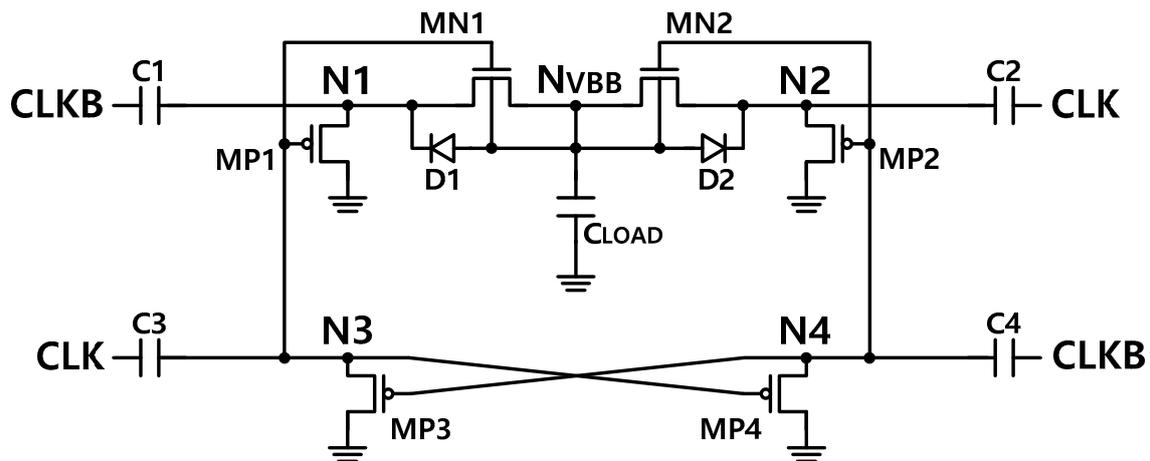
Figure 3. Conventional cross-coupled hybrid pumping circuit (Conv 2) [5].

Table 2. Sequential operation of Conv2.

Phase	CLK	MP1	MP3	MN1	V_{N1}	V_{N2}	V_{N3}	V_{N4}
1	High	Off	On	On	0	$\dfrac{\text{VCC}}{\lvert V_{tp}\rvert}$	$\dfrac{\text{VCC}}{\lvert V_{tp}\rvert}$	0
2	Low	On	Off	Off	$\dfrac{\text{VCC}}{0}$	$\lvert V_{tp}\rvert - \text{VCC}$	$\lvert V_{tp}\rvert - \text{VCC}$	$\dfrac{\text{VCC}}{0}$
3	High	Off	On	On	$-\text{VCC}$	$\dfrac{\lvert V_{tp}\rvert}{0}$	$\dfrac{\lvert V_{tp}\rvert}{0}$	$-\text{VCC}$
4	Low	On	Off	Off	0	$-\text{VCC}$	$-\text{VCC}$	0
5	High	Off	On	On	$-\text{VCC}$	0	0	$-\text{VCC}$

2.3. Conventional Cross-Coupled Hybrid Pumping Circuit Using the Auxiliary Pump (Conv 3)

Conv 2 is very useful in generating the negative voltage. However, when Conv 2 operates in sub-1-V regime, the pumping current through the transfer transistors is decreased. To overcome this problem, a cross-coupled hybrid pumping circuit using the auxiliary pump unit was introduced [7] and this circuit is referred to as Conv 3. Conv 3 is depicted in Figure 4. Conv 3 consists of six pumping capacitors, ten transistors, and two anti-phase clock signals. Two NMOS transistors, MT1 and MT2, are the transfer transistors, four PMOS transistors, MP1, MP2, MA1, and MA2, are the discharge transistors, and two PMOS transistors, MA3 and MA4, compose the auxiliary pump unit. Different from Conv 2, to obtain larger pumping current via transfer transistors, the nodes that were used to simultaneously control the gate of discharge transistor and transfer transistor are detached. The voltages at the nodes N5 and N6 are higher than the negative voltage of the other nodes. The higher voltage at node N5 or N6 turns MT1 or MT2 on, respectively. By using this scheme, Conv 3 is able to generate a larger pumping current in the transfer transistors compared to the other conventional schemes. Therefore, Conv 3 has the ability to reach −VCC faster [7]. The sequential operation of Conv 3 is described in Table 3.
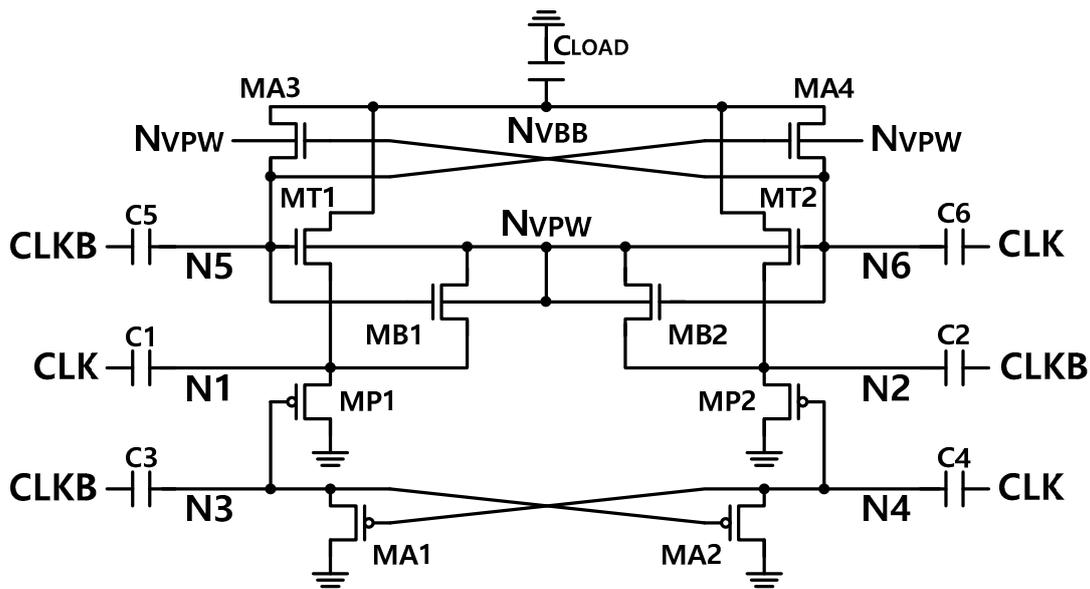
Figure 4. Conventional cross-coupled hybrid pumping circuit using an auxiliary pump unit (Conv 3) [7].

Table 3. Sequential operation of Conv3.

Phase	CLK	MA1	MP1	MT1	V_{N1}	V_{N2}	V_{N3}	V_{N4}	V_{NVPW}
1	High	Off	On	On	$\dfrac{VCC}{\lvert V_{tp}\rvert}$	0	0	$\dfrac{0}{\lvert V_{tp}\rvert}$	0
2	Low	On	Off	Off	$\lvert V_{tp}\rvert - VCC$	$\dfrac{VCC}{0}$	$\dfrac{VCC}{0}$	$\lvert V_{tp}\rvert - VCC$	$\lvert V_{tp}\rvert - VCC$
3	High	Off	On	On	$\dfrac{\lvert V_{tp}\rvert}{0}$	$-VCC$	$-VCC$	$\dfrac{\lvert V_{tp}\rvert}{0}$	$-VCC$
4	Low	On	Off	Off	$-VCC$	0	0	$-VCC$	$-VCC$
5	High	Off	On	On	0	$-VCC$	$-VCC$	0	$-VCC$

3. Proposed Cross-Coupled Hybrid Pumping Circuit

There are two main objectives in rendering the VBB generator effective. The first is that the node voltage clamping the node N_{VBB} via transfer transistors should be dropped from VCC to 0 V as quickly as possible. Then after repeated clock phasing, the voltage of the node that clamps the node N_{VBB} is able to attain the full -VCC level in a short time. That is consistent with the pump-down speed. The second is that a higher voltage level should control the gates of the transfer transistors in order to make the large pumping current via transfer transistors. These issues are addressed by the proposed circuit which is depicted in Figure 5. The proposed VBB generator consists of six pumping capacitors, eight transistors, and two anti-phase clock signals. Two NMOS transistors, MN1 and MN2, are the transfer transistors. Four PMOS transistors, MP1, MP2, MP3, and MP4, are the discharge transistors. Two PMOS transistors, MP7 and MP8, comprise an auxiliary pump unit. Two PMOS transistors, MP5 and MP6, are clamped between the nodes N3 and N5 and between nodes N4 and N6, respectively. The proposed circuit is characterized by generating more suitable voltages to control the gates of the discharge transistors and transfer transistors with lower negative voltage when discharging and higher positive voltage when transferring. To achieve this characteristic, the structure of the proposed circuit detaches the nodes to control the gates of the discharge transistors (MP1, MP2) and transfer transistors (MN1, MN2), respectively. The sequential operation is described in Table 4. Opposite polarities are preserved in the signals CLK and CLKB, MP1 and MP2, MP3 and MP4, MP5 and MP6, MP7 and MP8,

and MN1 and MN2. In phase 1, charges flow from node N3 to the ground and from node N5 via MP3 and MP5. The voltage at node N5 gets a higher voltage level A from 0 V to the charges flowing from node N3. Also, the voltage at node N6 changes from VCC to $|V_{tp}|$ because of the voltage at node N5.
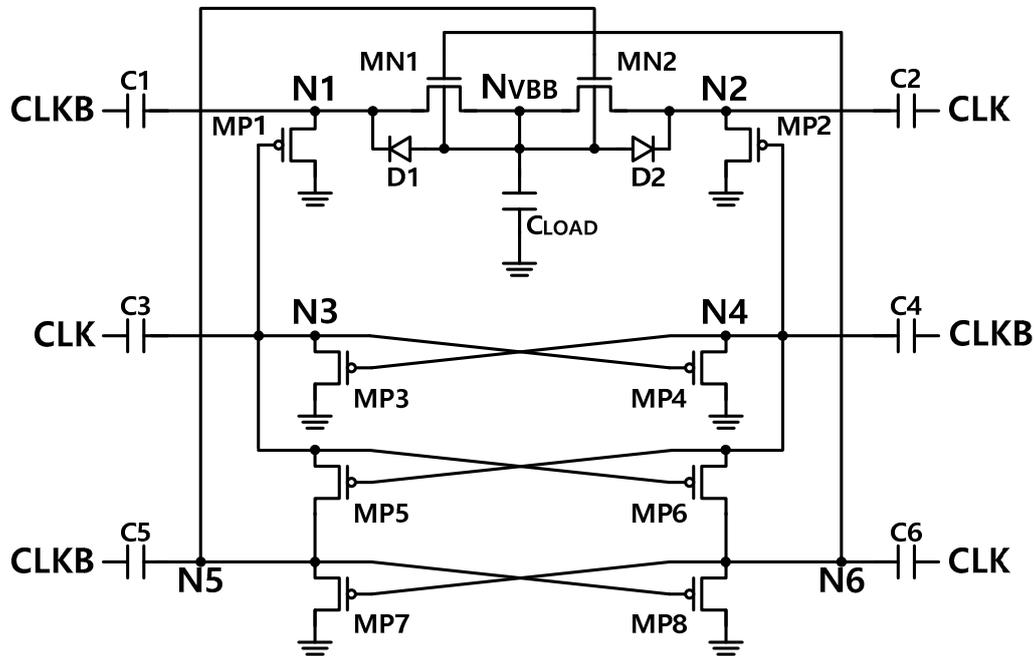

Figure 5. Proposed cross-coupled hybrid pumping circuit.

Table 4. Sequential operation of the proposed circuit.

Phase	CLK	MP1	MP3	MP5	MP7	MN1	V_{N1}	V_{N2}	V_{N3}	V_{N4}	V_{N5}	V_{N6}
1	High	Off	On	On	Off	On	0	VCC	VCC	0	0	VCC
								$|V_{tp}|$	$|V_{tp}|$		A	$|V_{tp}|$
2	Low	On	Off	Off	On	Off	VCC	$|V_{tp}|-$VCC	$|V_{tp}|-$VCC	VCC	A + VCC	$|V_{tp}|-$VCC
							0		$|V_{tp}|-$VCC + B	$-$C	A + VCC$-$B	$|V_{tp}|-$VCC + C
3	High	Off	On	On	Off	On	$-$VCC	$|V_{tp}|$	$|V_{tp}|$ +B	$-$C$-$VCC	A$-$B	$|V_{tp}|$ + C
								0	$-$C			
4	Low	On	Off	Off	On	Off	0	$-$VCC	$-$C$-$VCC	$-$C	A$-$B + VCC	$|V_{tp}|-$VCC + C
5	High	Off	On	On	Off	On	$-$VCC	0	$-$C	$-$C$-$VCC	A$-$B	$|V_{tp}|$ + C

In phase 2, when CLK is 'Low' and CLKB is 'High', the voltage at node N4 changes from VCC to voltage level $-$C that is lower than 0 V as node N4 is clamped to node N6. However, due to the voltage at node N3, MP4 also turns on, so the voltage at node N4 clamps not only to the negative voltage at node N6 but also to the ground via MP4. Due to this scheme, the voltage at node N4 is smaller than 0 V by C. There is no risk that MP2 turns on when CLKB is 'High' because the voltage at the transfer node N2 operates with the anti-phase clock with node N4. In phase 3, when CLK is 'High' and CLKB is 'Low', as the voltage at node N4 is C$-$VCC, the charges of node N2 are discharged faster than the conventional circuits that use $-$VCC to activate the discharge transistors. The voltage at node N6 rises to $|V_{tp}|$ + C from 0 V and it clamps to the ground via MP8 and also node N4 via MP6. The voltage of node N3 then turns from $|V_{tp}|$ +B to the negative voltage $-$C because it is clamped to the ground via MP3 and to the negative voltage node N5. As the function of the voltage difference between the drain and source of the transistor, the charges on node N6 are not discharged via MP8 but flow into node N4 via MP6. With repeated operations, some charges in node N4 flow into node N6 again, so that the voltage at node N6 is able to maintain the voltage level at a value greater than 0 V when CLK is 'High'. Anti-phasing clocks are applied in the symmetric branches in the proposed circuit. The resulting voltage difference between N3 and N4 and between N5 and N6 is VCC. As a function of the supply voltage VCC, the voltage levels

of A, B, and C are determined. The characteristic of this scheme aptly provides a lower negative voltage when discharging and a higher positive voltage when transferring, and the proposed circuit achieves the faster pump-down speed and the higher pumping current at lower supply voltages.

4. Experiment Results

The experiment results are shown in Figures 6–8, in which the pump-down speed, the |VBB|/VBB ratio, and the pumping current are compared among different schemes. The HSPICE simulations were performed with the Taiwan semiconductor manufacturing company (TSMC) 0.18 μm process technology. The simulation conditions are VCC = 1.2 V, C_{PUMP} = 1 nF each, C_{LOAD} = 10 nF, f_{PUMP} = 10 MHz, and $|I_{BB}|$ = 10 μA, where C_{PUMP}, C_{LOAD}, f_{PUMP}, and $|I_{BB}|$ denote the pumping capacitance, the load capacitance, the pumping frequency, and the load current, respectively.
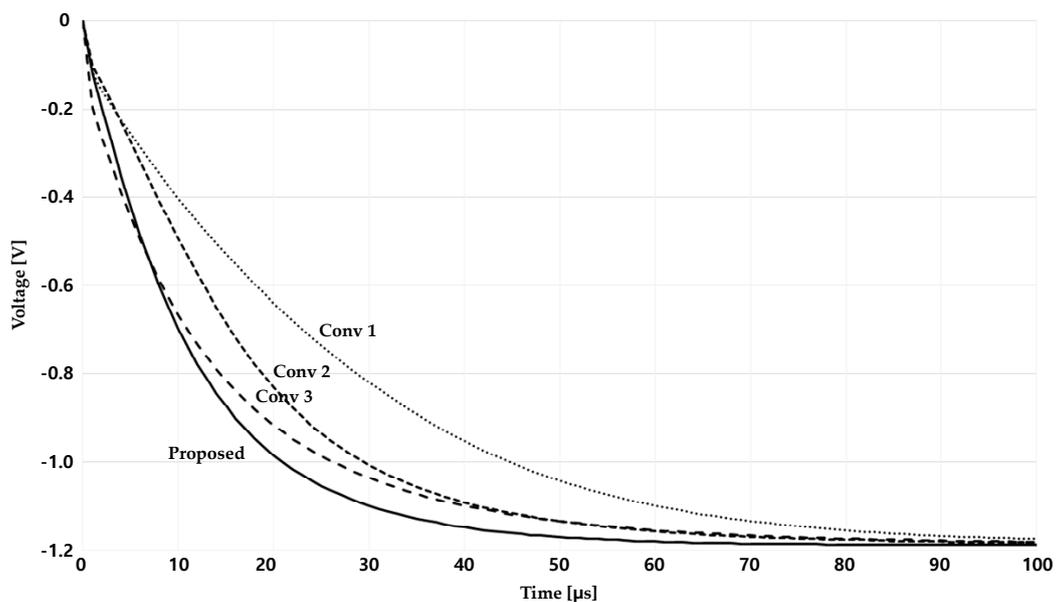
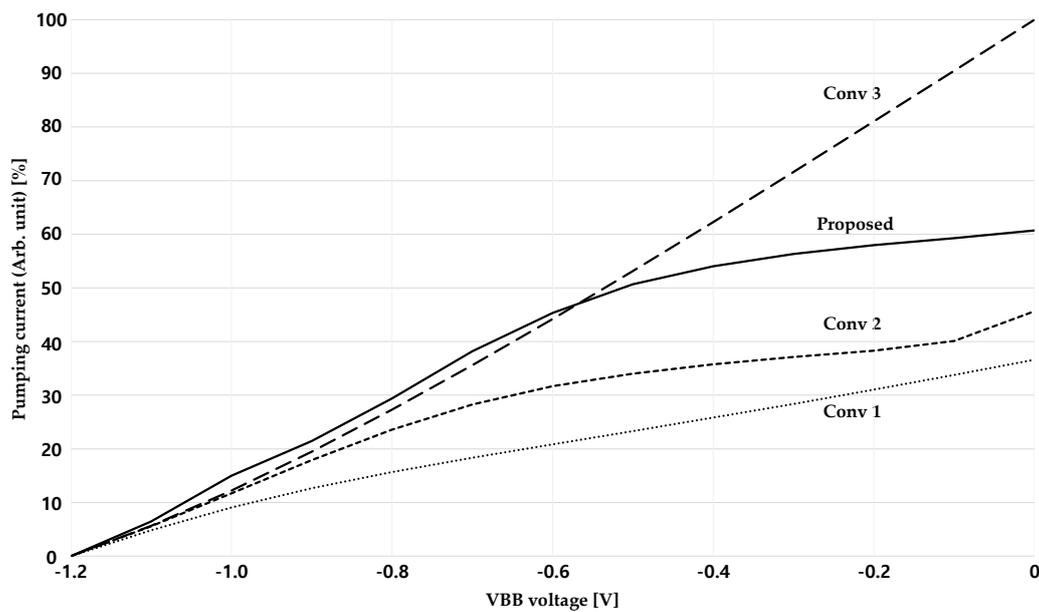**Figure 6.** Pump-down speed.
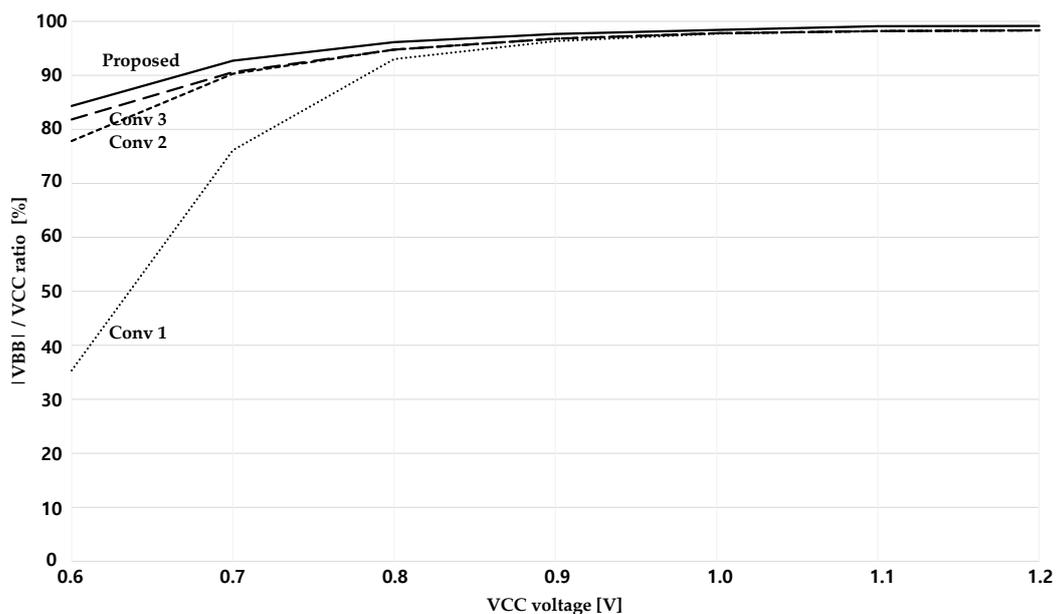
Figure 7. |VBB|/VCC ratio.

Figure 8. Pumping current.

4.1. Pump-Down Speed

Figure 6 shows the pump-down speeds among the VBB generator circuits explored. Transient simulations up to 100 μs were performed. Conv 3 shows the fastest pump-down speed initially until about 8 μs. Beyond this point, the proposed circuit shows a faster pump-down speed and reaches the target voltage of −VCC with the highest speed compared to the other conventional circuits. To attain 80% of −VCC, the pump-down speed of the proposed circuit is about 20% faster than that of Conv 3.

4.2. |VBB|/VCC

Figure 7 shows the |VBB|/VCC ratio with the supply voltage VCC varying from 0.6 V to 1.2 V. The same simulation conditions mentioned in the previous section are used. The proposed circuit shows the highest |VBB|/VCC ratio compared to other conventional circuits and this becomes pronounced as the supply voltage VCC is lowered down to 0.6 V. It reaches a ratio of 84.3% at VCC = 0.6 V which is 3% higher than that of Conv 3.

4.3. Pumping Current

Figure 8 indicates the pumping current as a function of the VBB voltage. The conditions of the simulation are the same without the load voltage in order to measure the pumping current flowing into the circuit. As the voltage at the node N_{VBB} becomes lower, the pumping current reduces as the VBB generator can transfer fewer charges to reach the target voltage. While Conv 3 shows the best pumping current at VBB = 0 V, the proposed circuit shows the highest pumping current beyond −0.6 V [3,11].

5. Conclusions

In this paper, a novel high-speed back-bias generator with a cross-coupled hybrid pumping scheme is proposed. Different from previous circuits, the new structure adds an auxiliary charge pump to obtain a higher pumping current and to be able to discharge with a greater efficiency using more suitable control voltages. This circuit exhibits the fastest pump-down speed, higher |VBB|/VCC ratio, and higher pumping current at very low voltage conditions compared to all prior VBB generator circuits. Moreover, the proposed circuit reaches a |VBB|/VCC ratio of 84.3% at the supply voltage of VCC = 0.6 V. From its capability to operate efficiently at very low voltage conditions, the proposed VBB circuit structure is quite suitable for future low-power and high-performance DRAM applications.

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