electronics

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Emulator of a Boost Converter for Educational Purposes

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Received: 13 October 2020; Accepted: 6 November 2020; Published: 9 November 2020

Abstract: Project-based learning (PBL) is proposed for the development of a Hardware-in-the-Loop (HIL) platform and the design of its digital controller for an undergraduate course on Digital Electronic Systems. The objective for students is the design of a digitally controlled HIL Boost converter, a digital pulse-width modulator (DPWM) and a current mode controller, implemented in field-programmable gate array (FPGA) devices. To this end, the different parts of the project are developed and evaluated, maximizing the use of FPGA resources in the design of the HIL and DPWM blocks, and applying design techniques that minimize the use of the digital resources used in the design of the controller. Students are equipped with a new individualized educational experience, allowing them to test their technical competence and knowledge in an environment close to the reality of the industry.

Keywords: Hardware-in-the-Loop, HIL; power converter; Boost; digital control; current control; FPGA; education; undergraduate; project-based learning, PBL

1. Introduction

Engineering curricula must incorporate contents that have jumped from scientific knowledge to emerging technologies in industry in order for the graduates to adapted to present competitive design methods [1]. To train this ability, it is necessary to equip the students with skills in tools which allow them to transfer their theoretical knowledge to the reality of the industry. In this sense, project-based learning (PBL) has been shown to be a very interesting method in the field of electronic engineering [2–6]. PBL is an educational technique through which students face close to real-world problems and challenges under the supervision of the instructor [7]. This methodology prepares students more effectively for professional work, achieving deeper learning [8].

On the other hand, the increase in the complexity of electronic systems, and the need to combine multidisciplinary concepts in a short time and a cost-effective way, have encouraged the search for new techniques for their development and testing, such as mixed signal simulators [9], simulators with analog and mixed signal extensions [10], or using two simulators at the same time—one that simulates the plant and the other the controller of that plant [11]. However, these techniques are slow and complex to develop [12]. That is why a new emulation technique has emerged as a viable and solvent alternative. This strategy is Hardware-in-the-loop (HIL) [13], which is a real-time simulation technique based on the implementation of a model in digital hardware to emulate the plant. Its use is adopted in industry and research laboratories as a low-cost and effective tool for verifying power converter controllers [14,15]. Beyond that, different electrical and non-electrical systems are emulated on which a control action is validated through the HIL concept [16]. Therefore, it can be configured to emulate

electronic systems designed for medical applications [17], mechatronics [18], smart grids [19,20], or, more specifically, power converters [11,21,22].

The implementation of these systems is carried out with different technologies, i.e., field-programmable gate arrays (FPGA), digital signal processors (DSP), complex programmable logic devices (CPLD) or microprocessors [23]. FPGA technology is preferred because it enables the selection of time-steps over a wide range [24–26] and the optimization of the processing speed and/or the occupied area [27,28]. Those characteristics are combined in a proper trade-off with the selection of the resolution of the signals involved in the emulator [12,29,30] to achieve precision [12] in consistency with the criteria for avoiding limit cycle conditions, and the specifications of steady-state error and stability margin tolerance.

From a professional point of view, this technique enables the following: (i) simulations to be carried out prior to and in parallel with the development of the plant, so that the simulated parts can be replaced by those already physically implemented as they become available; (ii) the test of the plant, based on HIL, in extreme situations, avoiding damaging the real plant; and, also, (iii) the reduction of the development cost, avoiding partial prototypes of the elements of the system and the cost of verification, as well as the breakdowns of a real system [31–34]. Meanwhile, from the academic point of view, the use of this tool allows the student to develop projects where they can put their technical knowledge into practice [35]. They can safely test their models and developments in countless situations. In this sense, many educational experiences around HIL projects can be found in the literature applied in different areas. In power systems, visualized experiences based on the use of integrated power distribution system laboratory setups are proposed in [36,37]. In [18], students have remote access to an HIL system that allows them to simulate the already configured behavior of robot manipulators in the transport area. In [38], medicine students have access to a complex closed-loop platform that emulates the interaction between the patient and the therapeutic devices. In [39,40], authors propose the use of a platform that allows the simulating of industrial equipment which is not available at universities for students to study its control. In general, in all these proposals, the user interaction with an HIL platform is carried out with a high-level programing language, with a schematic type design or graphic user interface. This makes the internal configuration of the HIL not accessible to the student.

For all of the above, the design and use of HIL in a PBL in a course on Digital Electronic Systems provides the students with an experience close to the industrial reality, which allows them to (i) build an HIL model, (ii) practice the digital electronics concepts using the hardware description language, (iii) acquire device selection criteria according to the application needs, identifying the pros and cons of implementing a design in a concurrent vs. a sequential device and adapt the circuit description in consistency with the hardware resources, and (iv) define, plan, and carry out a functional verification of synchronous digital circuits. Regarding the acquisition of skills, students acquire the ability to adapt to the environment and manage projects. So, this broadens the scope of other educational proposals based on HIL because making a low-level design of the HIL that is going to be used allows one to acquire competences not only in the field of power electronics, but also in digital electronics.

In this work, a PBL in the subject of Digital Electronic Systems is proposed. The small number of students and their diverse origin make it possible to carry out a specific pedagogy with the personalization and individualization of the teaching-learning objectives. This approach trains the students to acquire competences in digital circuit design, defining an HIL model and the corresponding digital controller without a specific HIL platform but a generic configurable concurrent digital hardware, as is the case of the FPGAs. The selected case study involves the design of a Boost HIL converter and the digital control of its input current. The HIL model and the controller are described with a non-proprietary hardware description language, i.e., a standard such as very high-speed integrated circuit hardware description language (VHDL). Then, acquired competences are applicable to a broader field of digital circuit applications. Furthermore, a collaboration among the professors of the course and the Hardware & Control Technology Laboratory (HCTLab) of the Universidad Autónoma de

Madrid (UAM) was established to verify the methodology and validate the results using the SPHIL tool developed by Sp Control Technologies™ in collaboration with HCTLab.

2. Context

The multidisciplinary Industrial Engineering program at the School of Industrial and Telecommunications Engineers at the University of Cantabria (UC) includes itineraries in electronics and automation which offer four courses in English. One of them is Digital Electronic Systems, focused on introducing students to digital hardware description and putting into practice the concepts of digital modeling and the control of power converters [41]. The updated content described here was introduced in 2018–2019. The incorporation of the HIL technique for system emulation equips the students with a more complete experience of the capabilities of the digital circuits in modeling systems and control verification in a safe and low-cost environment.

Its workload is the 6 European Credit Transfer System (ECTS), and has a weekly sequence of face-to-face activities, which includes two lecture hours, two lab hours a plus one-hour session for tutoring and follow-up activities. During the course, students work on six intermediate home-works, estimated as a two-hour workload each, and eight class-works, which take 15 min to 20 min each. With this organization, three generic competences are developed: to adapt to the digital design framework, to manage projects and to communicate and work in a foreign language. Emphasis is placed on gaining knowledge of the fundamentals and applications of digital electronics, and developing the capacity to develop analog, digital and power electronic systems. Finally, as a learning result, students can apply concepts of digital electronics to solve practical problems autonomously, manage the instrumentation of the laboratory, and critically examine the results obtained.

The number of enrolled students is usually low because students can validate the non-compulsory credits with other soft skills-oriented activities, such as volunteering or language courses. The number of students enrolled in 2017–2018 (Figure 1) was 10, the following year 8, and the last academic year (2019–2020) 8. Otherwise, the academic background of the students is diverse, since students participating in Erasmus and other interchange programs (incoming) and students from the UC coexist. Others (outgoing) use the subject to study in other universities. It is rather common that students with no previous background in power electronics follow the course. All of them attend the face-to-face sessions and participate in the continuous assessment activities. They are in the senior year with little or no internship experience in the field of the program. Therefore, the subject must be adapted to quite diverse profiles. The practical methodology oriented towards PBL permits the students to advance at different rates when necessary.

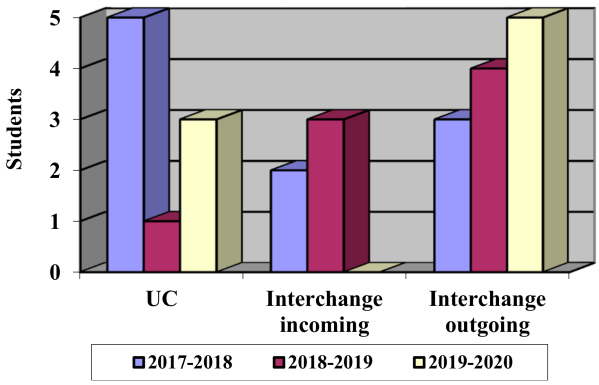


Figure 1. Number and origin of the students.

3. Teaching Organization of the Case Study

The proposed case has six practices, as described in Figure 2. The utilized software is highlighted in deep red. Students are introduced to a multi-language hardware description language (HDL) simulation environment, and they can use ModelSim, Vivado and ISE interchangeably based on their preferences. Finally, instruments allow them to verify the operation of the system in the FPGA.

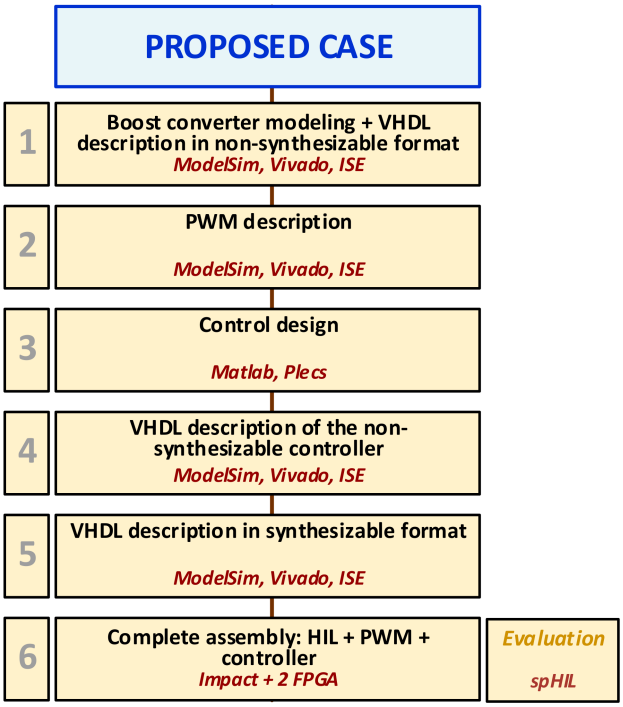


Figure 2. Summary of the proposed case.

3.1. Boost Converter Modeling

The Boost converter, shown in Figure 3, is a basic DC–DC power conversion topology. It uses an inductor, L, and a capacitor, C, as elements that store energy. In each switching period, in the first state, the on-time of switch S, energy is transferred from the source to the inductor and from the capacitor to the load. In the subsequent off-time, energy flows from both the source and the inductor through the diode, D, to the capacitor and the load, thus producing a higher voltage level across the load, v_o, than the source, v_g [42]. The Boost is modeled to simulate it together with its controller, as well as to run its real-time model with the controller already in hardware. Boost HIL replaces the real converter during the controller design stage, introducing a controller test that is easier, cheaper and safer, before the test interacting with the real circuit. The reason for using a Boost HIL is to avoid using the real converter, which uses real power, since it can pose a danger to the equipment and people, who are also inexperienced students.

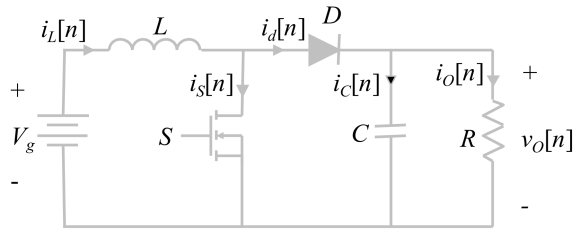


Figure 3. Boost converter.

Its model is the simplest. It uses a fixed time step to facilitate the realization of a synthesizable description [12]. Discrete equations define the state variables, inductor current, i_L, and capacitor voltage, v_o, and use the low ripple approximation of v_g and v_o and piecewise linear approximation for i_L, updating these variables in each period of numerical integration, n, [43].

In the on-time, the inductor voltage is v_g, which is

$$v_g = L\frac{di_L}{dt} \tag{1}$$

which becomes a difference equation:

$$i_L[n] = i_L[n-1] + \frac{\Delta t}{L} \cdot v_g \tag{2}$$

Similarly, the current–voltage ratio of the capacitor, i_C,

$$i_C = C\frac{dv_0}{dt} \tag{3}$$

is rewritten integrally as a discrete equation,

$$v_0[n] = v_0[n-1] + \frac{\Delta t}{C} \cdot i_C \tag{4}$$

With (2) and (4), the behavior of the converter is described according to the state of the switch and the diode. When S is open, the cases of operation in the continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM), as applicable, are emulated. Therefore, there are three states, which are described below.

S closed and D open:

$$i_L[n] = i_L[n-1] + \frac{\Delta t}{L} \cdot v_g \tag{5}$$

$$v_0[n] = v_0[n-1] - \frac{\Delta t}{C} \cdot i_0 \tag{6}$$

S open and D closed:

$$i_L[n] = i_L[n-1] + \frac{\Delta t}{L} \cdot \left(v_g - v_0\right) \tag{7}$$

$$v_0[n] = v_0[n-1] + \frac{\Delta t}{C} \cdot (i_L - i_0) \tag{8}$$

S and D open:

$$i_L[n] = 0 \tag{9}$$

$$v_0[n] = v_0[n-1] - \frac{\Delta t}{C} \cdot i_0 \tag{10}$$

Δt is the period of numerical integration, which is equal to the FPGA clock period for obtaining the maximum resolution, without using the better approximation methods that go beyond the objectives of the course, so $\Delta t/L$ and $\Delta t/C$ are constant. The variable i_C is the current through the capacitor, which is determined by the output load. The variable i_C is $-i_R$ if the diode is a closed switch. $i_R = v_0/R$ is used if a resistive load is preset.

Students are first asked to describe the Boost converter model using real-type signals in VHDL, not for synthesis, and to elaborate a test bench. This work is divided into two previous sub-works: the digital description of the L and C components and the description of the switch and diode cell. The parameters of the Boost are included in Table 1.

Table 1. Parameters used in the Boost converter.

Parameter	Value	Parameter	Value
Δt	100 ns	V_0	500 V
L	150 µH	D	0.6
C	500 µF	I_0	30 A
R_L	16.7 Ω	I_L	75 A
V_g	200 V	-	-

3.2. PWM

The pulse-width modulator (PWM) (Figure 4) is presented as the sampler of the controller output signal. The frequency response of sampled signals compared with continuous signals, and the possible generation of aliases, are reviewed. The generation of PWM results from the comparison of the modulating signals, resulting from the control action, v^*_c, that is acquired at the beginning of each switching period to obtain the PWM signal, avoiding the vertical crossing effect [44].

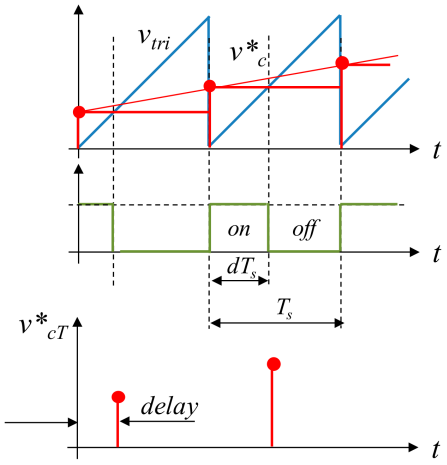


Figure 4. PWM modulator with uniform sampling.

The resolution of the PWM depends on the number of clock cycles in the switching period and the type of carrier. Students are introduced to techniques for increasing the resolution of the PWM block and how to avoid limit cycle oscillations [45].

Students are asked to describe a synthesizable pulse-width modulator block in VHDL. They have two options to generate the carrier signal [46]: triangular signal or sawtooth. A specific task of the PWM block, independent of the general case described in this work, is defined as a lab practice, allowing students to further study this key issue by working with different switching frequencies and resolutions.

The effect of PWM modulation at a low frequency is visualized on the oscilloscope. The reading frequency of the sinusoidal signal stored in the memory can be adjusted in the address counter, which allows for introducing disturbances into the duty cycle value at different frequencies, and this feature is also useful to obtain the frequency response of the Boost HIL.

3.3. Control Design

The technical objective of the project is to control the input current to the converter. The control of the input current to the converter is chosen so that the controller can be solved with a simple proportional–integral (PI) action. The design of the control is carried out using linear control techniques. The plant is derived in the digital domain with the aforementioned low-ripple voltage approach [47,48].

Consequently, the current i_L is piecewise linearly approximated. The small-signal natural and forced responses, as observed in Figure 5, are superimposed and, later, the disturbance is extracted by subtracting the perturbed current from the unperturbed one, i_L, describing the result, $\tilde{i}_L$, in the z domain using uniform sampling.

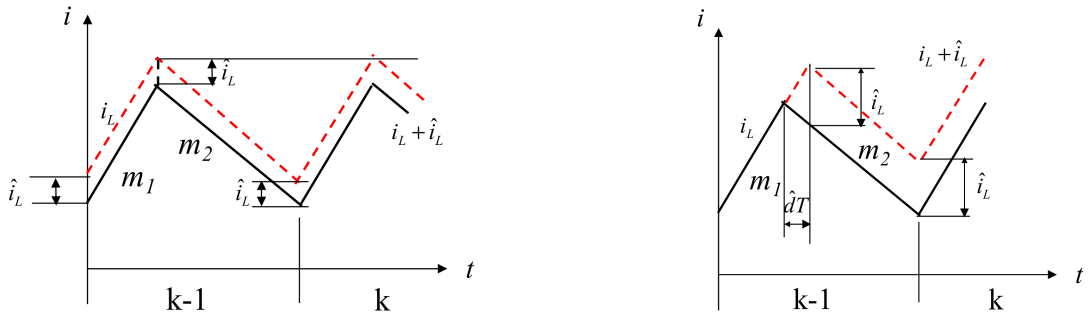


Figure 5. Simplified digital modeling of the Boost converter. (**a**) Natural response and (**b**) forced response.

Using this method, it results in a second order system,

$$\begin{bmatrix} \tilde{v}[n] \\ \tilde{i}[n] \end{bmatrix} = \begin{bmatrix} 1-\frac{T}{RC} & \frac{(1-D)T}{C} \\ -\frac{(1-D)T}{L} & 1 \end{bmatrix} \begin{bmatrix} \tilde{v}[n-1] \\ \tilde{i}[n-1] \end{bmatrix} + \begin{bmatrix} -\frac{IT}{C} \\ \frac{VT}{L} \end{bmatrix} \left[\tilde{d}[n-1]\right] \tag{11}$$

from which the transfer function of the plant is obtained

$$G_{ic}(z) = \frac{\tilde{i}}{\tilde{d}} = \frac{VT}{L} \frac{z^{-1} + z^{-2}\left(\frac{2T}{RC} - 1\right)}{1 - z^{-1}\left(2 - \frac{T}{RC}\right) + z^{-2}\left(1 + \frac{(1-D)^2T^2}{LC} - \frac{T}{RC}\right)} \tag{12}$$

where z^{-1} represents the delay of a switching period. If in the case of sufficiently high frequency disturbances, v_o constant is assumed, the system order is reduced and the analysis is simplified.

$$\tilde{i}[n] = \tilde{i}[n-1] + (M_1 + M_2)\tilde{d}[n-1]T \tag{13}$$

The plant being approximated to

$$\frac{\tilde{i}}{\tilde{d}} = \frac{V}{L} T \frac{z^{-1}}{1 - z^{-1}} \tag{14}$$

The structure of the current control applied to the Boost HIL is shown in Figure 6. The inductor current, i_L, is compared with a reference signal, i_{ref}. The generated error signal, $\varepsilon[n]$, is the input to the control block, $G_c(z)$, which in this case is a PI controller, whose output is the input to the digital PWM (DPWM) block to generate the on and off signal for the switch S.

In the third practice, the design a PI controller for the input current of the converter is proposed, specifying a sampling frequency f_s = 20 kHz, a crossover frequency f_c = 2 kHz and a phase margin PM > 50°.

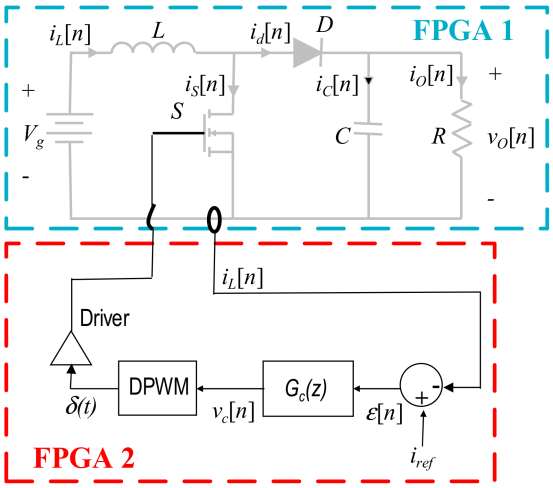


Figure 6. Schematic of the closed loop system.

3.4. VHDL Description of Non-Synthesizable Controller

Students rely on simulations with a numerical computing software to verify the design of the digital controller. The transfer function in the discrete domain has the following format:

$$G_c\left(z^{-1}\right) = \frac{B_0 + B_1 z^{-1}}{1 + A_1 z^{-1}} \tag{15}$$

where A_1, B_0 y B_1 are system gains.

This function is described based on the structure of a finite impulse response (FIR) filter according to Figure 7.

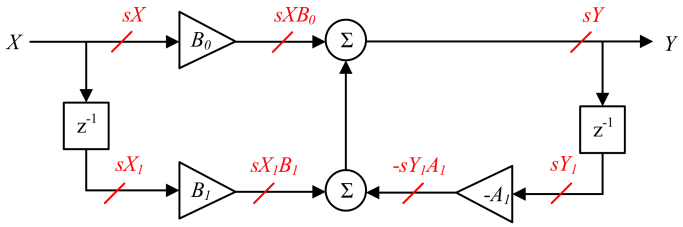


Figure 7. Materialization of the controller based on FIR filter structure.

The signals (*sX*, *sY*, etc.) involved in the digital controller have been highlighted in red. The controller output signal in VHDL code is obtained from

$$sY <= sXB_0 + sX_1B_1 - sY_1A_1 \tag{16}$$

In the fourth practice, the preparation of the VHDL description of the digital controller and the PWM of the Boost converter with real-type signals is proposed. The objective is to verify the controller interacting with the Boost HIL by preparing a first version of the test bench for the whole system.

3.5. VHDL Description in Synthesizable Format

Here, students are guided in the transformation of their VHDL description, in real format, of the regulator and Boost, to a synthesizable format, with the aim of becoming familiar with the scaling and quantization concepts and effects. To accomplish this task, they can use different formats and integers, std_logic_vector and sfixed, after receiving a lesson on fixed point number format. In this

task, students check the operation of the regulator they have designed before verifying its behavior in an FPGA and with a commercial HIL in the next task.

3.6. Complete Assembly (Hardware-in-the-Loop + PWM + Controller)

The design of the system is completed with closed-loop control of the plant. The proposed scheme to carry out this practice is to first use a single FPGA for the whole system, and then later two separate FPGAs for the whole system, as shown in Figure 6, for a more complete verification. The objective is to synthesize the control code and verify its operation by interacting with HIL. In parallel, the design is evaluated using the SPHIL module [49], in collaboration with the HCTLab of the UAM, in an FPGA. This tool includes a switched Boost model, adjusted using a very intuitive graphical interface to measure four different parameters (v_g, i_L, v_C and v_0). The other FPGA contains the synthesized code of the PI control and PWM designed by the student. In this practice, it is only necessary to read an input signal, i_L, and, for its configuration, a previous template is provided.

In this part, students use a commercial HIL model to evaluate their proposal, and not the one they had developed. This task makes the students test their regulator in hardware, to reinforce their learning with results in the laboratory where they measure the resulting hardware.

3.7. Evaluation

Finally, marks are given at the end of the course according to the following general criteria:

- no satisfactory solution—fail;
- simulation of the basic performance—C;
- implementation in FPGA and functional verification—B;
- verification of the circuit performance using HIL technique—A.

This score represents 50% of the final mark. The follow-up done in the classroom represents 20% and the other 30% corresponds to the exercises done in the classroom.

4. Results Obtained

This section shows the results of the practical case study. Two FPGA have been used to carry out the final verification stage: a Nexys 4DDR (XC7A100T-1CSG324C) and an Arty-Z7 (XC7Z010-1CLG400C). The oscilloscope used is the MSO-X 3104A model from Agilent Technologies.

The operation of the HIL emulator has been verified by applying different duty cycle values. Figure 8 shows the resulting output voltage and i_L in a steady state when using the parameters in Table 1 on the emulator.

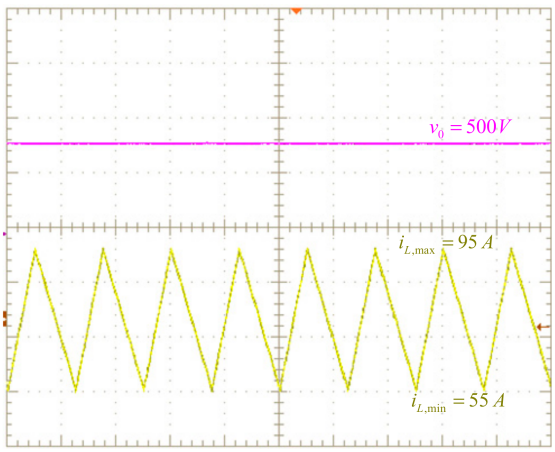


Figure 8. Output voltage and inductor current in the emulator with $d = 0.6$. i_L, in yellow (15 A/div), v_0, in magenta (15 V/div), and time (40 µs/div).

Figure 9 shows the results obtained when analyzing the behavior of the controller designed in MATLAB®. The control is then described in VHDL in real format, together with the PWM and the Boost converter, simulating its behavior with ModelSim®. In Figure 10, the results obtained in the simulation are shown, and their values coincide with those obtained in Figure 8.

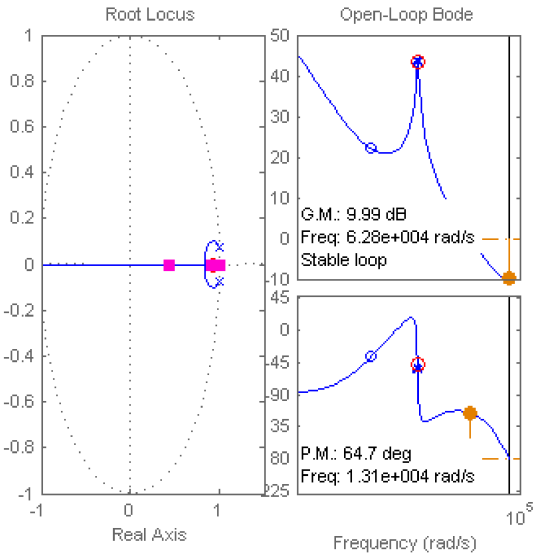


Figure 9. Behavior characterization of the control loop with the PI controller designed in Matlab.

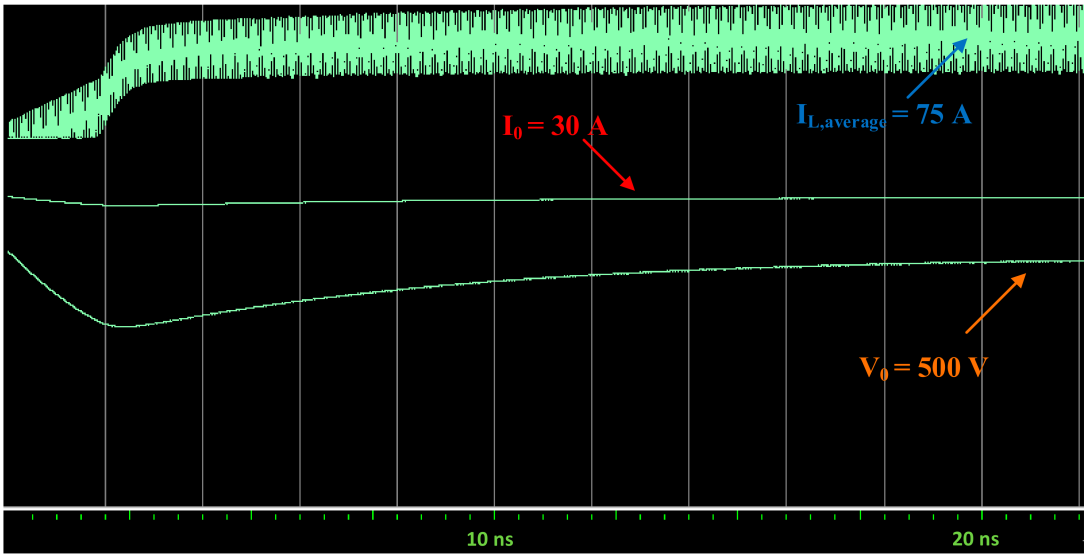


Figure 10. Simulation results obtained in ModelSim with the implemented circuit and the test bench.

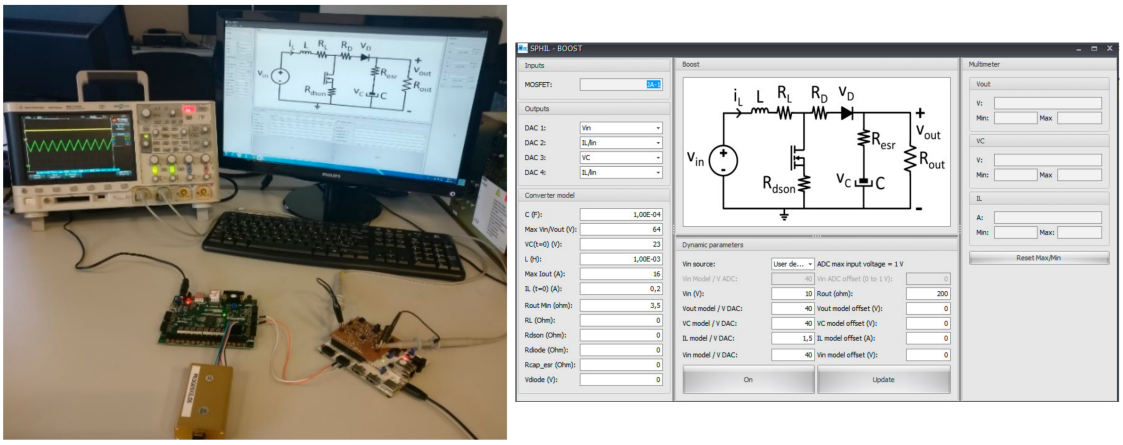
When converting the code from the real format to another synthesizable one, the float32 format may initially be more attractive to students due to its simplicity when it comes to being used on the circuit. However, this requires a higher number of hardware resources in the FPGA, and its use may compromise the temporary restrictions of the design. To illustrate this effect, a multiplication of two numbers in the float32 format and two numbers in 32-bit integer is implemented in class using the ISE® program. The operations are implemented and shown in Table 2, where the multiplication operation works 2.7 times faster in int32 than in float32, and it adds 19 times faster, despite having less hardware resources in general.

Table 2. Parameters used in the Boost converter.

Operation	DSP48E	LUT	Timing
float32 * *float32*	3	135	52.435 ns
float32 + *float32*	2	195	88.970 ns
int32 * *int32*	4	231	19.315 ns
int32 + *int32*	0	186	4.658 ns

* is multiplication, + is addition and DSP48E and LUT are digital signal processing logic and look up table elements, respectively.

Finally, the response of the digitally controlled HIL Boost converter is evaluated via the SPHIL tool in an Arty Z7-20 FPGA, as shown in Figure 11a, to emulate the Boost HIL, and a Nexys 4 FPGA to emulate a controller and the DPWM. A graphical interface allows the SPHIL user to configure the parameters of the Boost converter as shown in Figure 11b. With those hardware tests, students can evaluate the performance of their regulators, which they had already simulated in a closed loop, and are now working on hardware with a commercial HIL model that makes Boost. This offers extra motivation for students who feels that their work is recognized, because it has real utility and encourages competitiveness among them by checking which design is more robust out of them all.



(**a**) (**b**)

Figure 11. Boost converter emulator to verify designs proposed by students. (**a**) Laboratory mount configuration and (**b**) SPHIL graphical user interface.

The power converter model and control has been chosen to combine a practical exercise of digital circuit design, considering different sources of specifications for the HIL and the controller. This approach presents a deep insight into the operation of switching power converters, and their digital controllers with specific characteristics, different from the analog counterpart. So, the case study puts in practice concepts of power electronics and digital electronics that are hard to assimilate without encountering a practical design, such as the digitalization effects of sampling, quantization, resolution and additional delays. Moreover, the learning benefits are clear since the contents of digital circuit design and power electronics are combined in one course, going from theory to the experimental verification of the result.

5. Conclusions

A Digital Electronic Systems course focused on PBL is proposed to level students with different backgrounds. The project is based on the development of an HIL platform and the design of its digital controller, and concepts of digital modeling, the control of power converters and techniques of digital hardware description are applied. In general, this proposal allows students to acquire competences

in the field of power electronics and digital electronics at the same time. Specifically, it confronts students with the design trade-off between the limitation of hardware resources and static and dynamic performance, and allows them to experience the effects of inconsistent designs, such as the appearance of a response with a limited cycle, and the effects of aliases or delays that reduce or eliminate the phase margin. At the same time, the dual utility of a hardware description standard, initially as a specification validation tool and later as a circuit definition language, reinforces the acquisition of abilities to solve effective digital design specifications. Finally, the results of applying this teaching project have been validated with a proven commercial tool designed in a different environment from that in which teaching is carried out, which allows students to obtain an enhanced learning experience.

Author Contributions: P.L. carried out a postdoctorate at the HTCLab of the UAM where she studied Hardware-in-the-Loop techniques under the tutelage of Á.d.C., P.L. developed the practices of this work. F.J.A. and C.B. teach Digital Electronic Systems course in the UC and they put into practice the planned work with students. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: The authors thank the company Sp Control Technologies for the assignment of their SPHIL product developed together with the HCTLab research group of UAM.

Conflicts of Interest: The authors declare no conflict of interest.

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