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A Novel Zero Dead-Time PWM Method to Improve the Current Distortion of a Three-Level NPC Inverter

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Abstract: This paper proposes a novel pulse width modulation (PWM) for a three-level neutral point clamped (NPC) voltage source inverter (VSI). When the conventional PWM method is used in three-level NPC VSI, dead time is required to prevent a short circuit caused by the operation of complementary devices on the upper and lower arms. However, current distortion is increased because of the dead time and it can also cause a voltage unbalance in the dc-link. To solve this problem, we propose a zero dead-time width modulation (ZDPWM) which does not require dead time used in complementary operation. The proposed technique applies the offset voltage to the space vector pulse width modulation (SVPWM) reference voltage for the same modulation index (MI) as the conventional SVPWM, but any complementary switching operation needs dead time. In addition, the proposed method is divided into four operation sections using the reference voltage and phase current to operate switching devices which flow the current depending on the section. This ZDPWM method is simply implemented by carrier and reference voltage that reduce the current distortion, because complementary operation that needs dead time is not implemented. However, the operation section is delayed due to the sampling delay that occurs during the experiment. Therefore, in this paper, we conduct a modeling of sampling delay to improve the delay of operation section. To verify the principle and feasibility of the proposed ZDPWM method, a simulation and experiment are implemented.

Keywords: three-level NPC VSI; zero dead-time PWM; sampling delay; current distortion

1. Introduction

In high power applications such as medium voltage motor drives, solar cells, vehicles, and most recently, wind generation system, etc., multilevel topologies introduced in [1] have been widely applied to reduce harmonic in the grid current, to downsize the physical filter size, and to mitigate the switching losses of the used devices as compared with the conventional two-level pulse width modulation (PWM) inverter. These multilevel topologies allow the output voltage to be closer to the sinusoidal wave by increasing the number of voltage levels, and reducing the harmonic distortion, as reported in the literature [2–4]. The major multilevel topologies that have been studied are neutral point clamped (NPC) [5,6], active net point clamped (ANPC) [7–9], flying capacitor (FC) [10–12], and cascaded multilevel inverter (CMLI) [13,14]. The ANPC application has a high cost since it has a relatively large number of switching devices. The capacitor used in FC requires precharging, and the high number of flying capacitors required with increasing output levels reduces system reliability. The disadvantages of CMLI are the complexity of synchronization and the unbalanced power losses between power modules. Among these topologies, the three-level neutral point clamped (NPC) voltage source inverter

(VSI) is the most popular topology as compared with other three-level topologies because it has some advantages such as simple operating sequence, low voltage stress, and low switching losses [15,16]. Figure 1 illustrates a three-level NPC VSI topology.

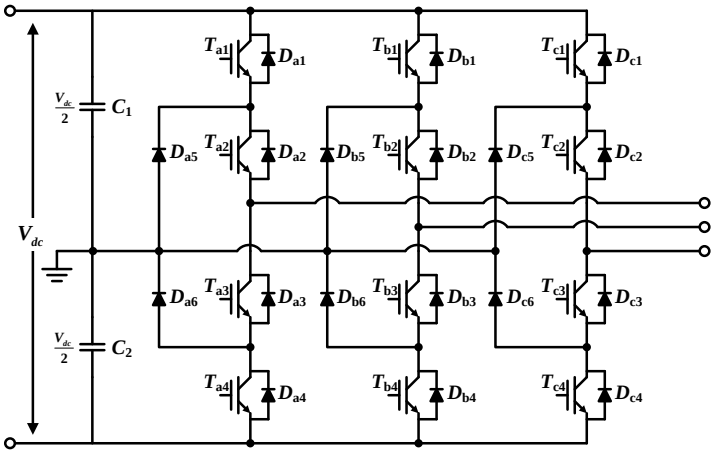


Figure 1. Configuration of the three-level neutral point clamped (NPC) voltage source inverter (VSI).

Each leg consists of four switching devices which are connected in series, two diodes, and a neutral point of dc-link as shown in Figure 1.

The performance including the efficiency and total harmonic distortion (THD) of the three-level NPC VSI is affected by the PWM method such as sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), and discontinuous pulse width modulation (DPWM), etc.; the available output voltage area is determined depending on the PWM method [17–20]. The previously explained PWM techniques all require dead time when transitioning from positive to zero, or reverse, switching transition conditions. In this transition time, the switching device, T_{x1}, is turned off and the switching device, T_{x3}, is turned on, in parallel. During the transition time, the dead time is applied to prevent a short circuit caused by the on/off delay of the switching devices.

However, the dead time in the complementary switching method causes distortion in the output voltage, and therefore increases the THD in the phase current. For this reason, dead-time compensation methods are widely studied to reduce the THD in phase current [21–24]. In [21], the authors proposed a method to improve the harmonic components caused by dead time by applying the offset voltage which consisted of the reference voltage and distorted output voltage in an inverter. Selective harmonic elimination (SHE) modulation is also one of the ways to solve harmonic component, considering dead-time effect [25]. However, since this method is based on the PWM which operates complementarily, these methods have the characteristic of turning on the switching device even when there is no current flowing into the switching devices.

Another research integrated the sixth harmonic of the synchronous d-axis proportional-integral (PI) current regulator [22]. This method imposes high computational burden and is difficult to realize, because of the detection of harmonics by integrated operation with integral controller. A previous study used a parameter adjustment mechanism for adaptive dead-time compensation [23]. Because this method utilized the dc-bus voltage and three-phase voltage, it was difficult to achieve an accurate effect if an imbalance of three-phase voltage and dc-bus voltage existed. In [26], dead-time compensation was performed with a dead-time correction state machine. This method was based on the error from measured three-phase voltage and current, and sensitiveness existed from the disturbance, which was a disadvantage.

In the case of the previous studies, there are limitations to the compensation of current disturbance due to dead time, because of the modulation or complicated control configuration and mechanism, and based on various infarction signals.

In this paper, to solve these limitations, the zero dead-time width modulation (ZDPWM) method is proposed which does not need the dead-time, and therefore there improve the distortion of output current. A short circuit which is caused by the on/off delay of switching devices does not appear when the complementary switching operation is not used. Thus, in this paper, we describe the ZDPWM method that operates without dead time, and how this PWM is implemented by comparing the carrier and reference voltage. We also suggest an improved method that can solve the sampling delay of a microcontroller unit (MCU) that is seen in the experiment.

This paper is organized as follows: In Section 2, we describe the basic structure and theory of the existing three-level NPC topology; in Section 3, we describe the analysis of the proposed ZDPWM method and how to implement the proposed technique; in Section 4, we describe the impact of sampling delay on the proposed ZDPWM method and the technique to improve this; in Section 5, we describe the simulation and experimental results for validation of the proposed control; and in Section 6, we provide the conclusions.

2. Configuration of the Three-level Neutral Point Clamped (NPC) Inverter and Operation Principle

In this section, first, we describe the basic configuration and operating principles of NPC topology and the effects of dead time before describing the proposed techniques.

The three-level NPC inverter, as shown in Figure 1, is connected to the neutral point, the neutral point clamp diode, and the dc-link capacitor, each leg consists of four switches, and two neutral point clamp diodes. Since the two neutral point clamp diodes are connected to the neutral point of the dc-link, unlike the two-level inverter, an output state of "zero" is possible.

Table 1 shows the switching state of the three-level NPC inverter according to the output voltage. Switching states can be divided into three states depending on the output voltage. Figure 2 shows the flow of current with switching status in a three-level NPC inverter. The state, in Figure 2a, outputs a voltage of "positive" with current flowing under load from the top capacitor and switches T_{x1} and T_{x2} on one leg. T_{x1} and T_{x3}, T_{x2} and T_{x4} perform reciprocal actions, therefore, T_{x3} and T_{x4} are off. The state, in Figure 2b, is that the current is flowing from the neutral point to the load, the voltage output is "zero", with switches T_{x2} and T_{x3} on and switches T_{x1} and T_{x4} off. The state, in Figure 2c, is that the current is flowing from the lower capacitor to the load, the voltage output is "negative", with switches T_{x3} and T_{x4} on and switches T_{x1} and T_{x2} off.

Table 1. Switching state of three-level NPC inverter depending on output voltage.

State	T_{x1}	T_{x2}	T_{x3}	T_{x4}
Positive	1	1	0	0
Zero	0	1	1	0
Negative	0	0	1	1

These three-level NPC inverters can be designed to have a lower voltage on each switch than conventional two-level inverters because one leg consists of four switches. In addition, the level of voltage is higher than that of a two-level inverter, therefore, the THD is lower. All elements are switched to the fundamental frequency, which gives the inverter a high efficiency advantage [27].

The three-level NPC is generally adapting SVPWM, the same as the two-level inverters [28]. With SVPWM, the three-level NPC inverter consists of a total of 27 switching states and 19 voltage vectors, as shown in Figure 3.

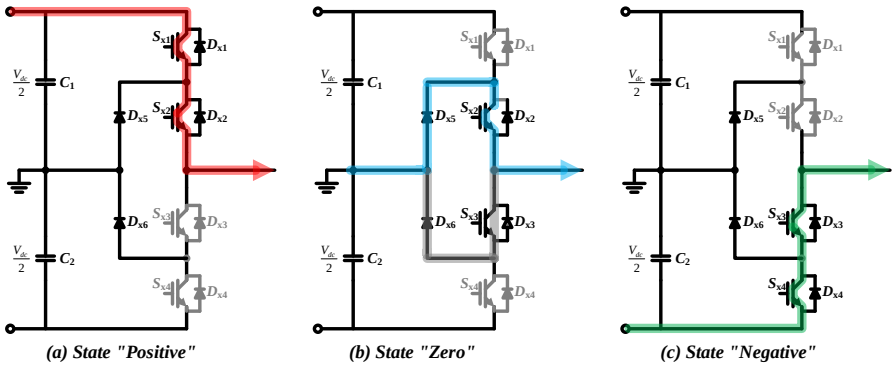


Figure 2. Current flow of three-level NPC inverter depending on the switching state.

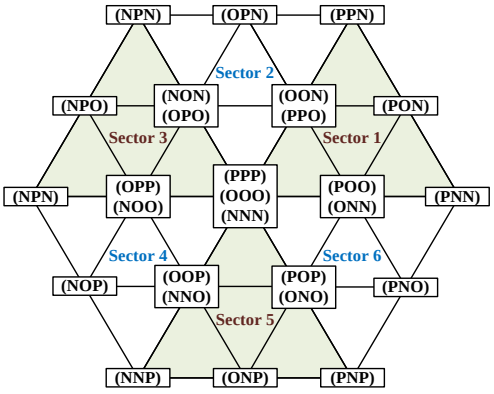


Figure 3. Vector diagram of three-level NPC inverter.

At this time, vectors requiring dead time are divided into three forms, as shown in Figure 4, depending on the state of the load. First, a unit vector, representing 120 degrees phase displacement, is as shown in Equation (1), in order to express the phase voltage of the load as:

$$a = e^{j2\pi/3} = -\frac{1}{2} + j\sqrt{3/2} \tag{1}$$

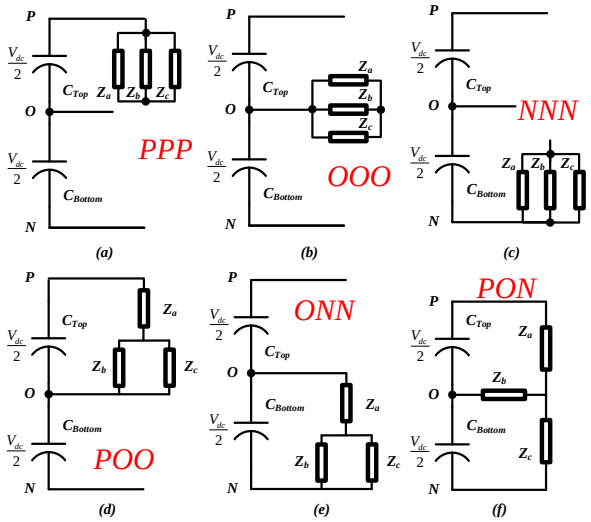


Figure 4. Voltage vector depending on the switching state: (**a**) PPP; (**b**) OOO; (**c**) NNN; (**d**) POO; (**e**) ONN; (**f**) PON.

The space vector of the phase voltage of the load can be expressed as shown in Equation (2):

$$V = \frac{2}{3}(v_{a0} + av_{b0} + a^2 v_{c0}) \tag{2}$$

With equation (2), the voltage vector of the zero vector in Figure 4a–c can be expressed as (3):

$$\begin{aligned} V_{(PPP)} &= \tfrac{2}{3}\left(\tfrac{V_{dc}}{2} + a\tfrac{V_{dc}}{2} + a^2\tfrac{V_{dc}}{2}\right) = 0 \\ V_{(OOO)} &= \tfrac{2}{3}\left(0 + a + a^2\right) = 0 \\ V_{(NNN)} &= \tfrac{2}{3}\left(-\tfrac{V_{dc}}{2} - a\tfrac{V_{dc}}{2} - a^2\tfrac{V_{dc}}{2}\right) = 0 \end{aligned} \tag{3}$$

Figure 4d,e shows a small vector. When switching states are (POO) and (ONN), voltage vectors can be expressed in the following ways:

$$\begin{aligned} V_{(POO)} &= \tfrac{2}{3}\left(\tfrac{V_{dc}}{2} + a0 + a^2 0\right) = \tfrac{V_{dc}}{3} \\ V_{(oNN)} &= \tfrac{2}{3}\left(0 - a\tfrac{V_{dc}}{2} - a^2\tfrac{V_{dc}}{2}\right) = \tfrac{V_{dc}}{3} \end{aligned} \tag{4}$$

In addition, Figure 4f shows the medium vector, and if the switching state is (PON), the dc-link neutral point is connected to the load stage, which affects the voltage variation of the neutral point. In the above state, the voltage vector may be shown as follows:

$$V_{(PON)} = \frac{2}{3}\left(\frac{V_{dc}}{2} + a0 - a^2\frac{V_{dc}}{2}\right) = \frac{V_{dc}}{3}(1 - a^2) = \frac{V_{dc}}{\sqrt{3}}e^{j\pi/6} \tag{5}$$

In order to make the above load conditions, the three-level NPC inverter must perform a complementary operation of four insulated gate bipolar transistor (IGBT) and two reverse parallel diodes, as described earlier.

Figure 5 shows the characteristics of power switching devices that use dead time, when performing complementary operation. The upper side represents switching signals, and the bottom side represents collector-emitter voltage and output current. As shown in Figure 5, the transition between the on/off states may cause a short circuit, due to the time difference between rising time and falling time, and therefore dead time is applied to the on/off signals to prevent such short circuit accidents. However, due to the effect of dead time, an error occurs between the commanded voltage and the actual voltage. These voltage errors vary with the inverter current direction.

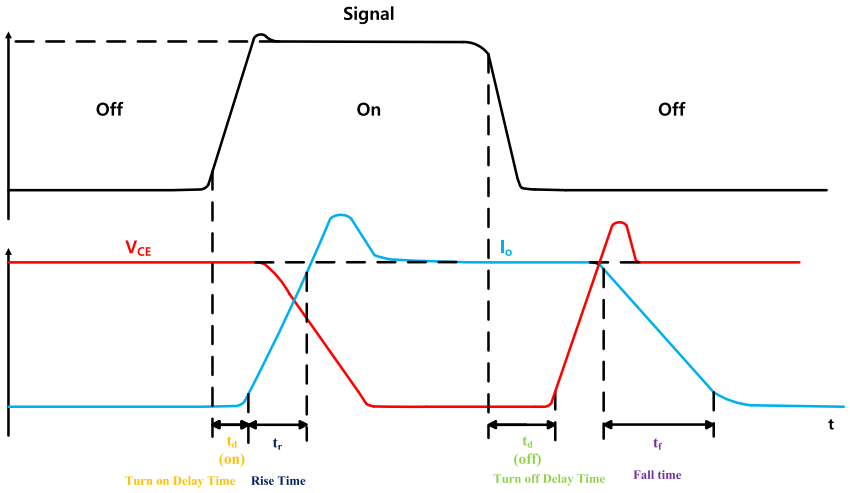


Figure 5. Turn-on/off characteristics of a switching power device.

Figure 6 shows the switching state and output voltage during dead time. Switch T_{x2} is always on, and T_{x4} is always off. When the direction of the current is $i_o > 0$, applying the dead time by t_{dead} to switch T_{x1} causes an error between the command switching and the actual switching, resulting in an error voltage equal to V_{error} in the output voltage. Similarly, when the direction of the current is $i_o < 0$, applying dead time to T_{x3} produces a voltage error as much as V_{error} at the output voltage. The error voltage generated by such dead time causes distortion of the output current, higher distortion of the electric wave, and lower stability of the system, due to the distorted output current [29].

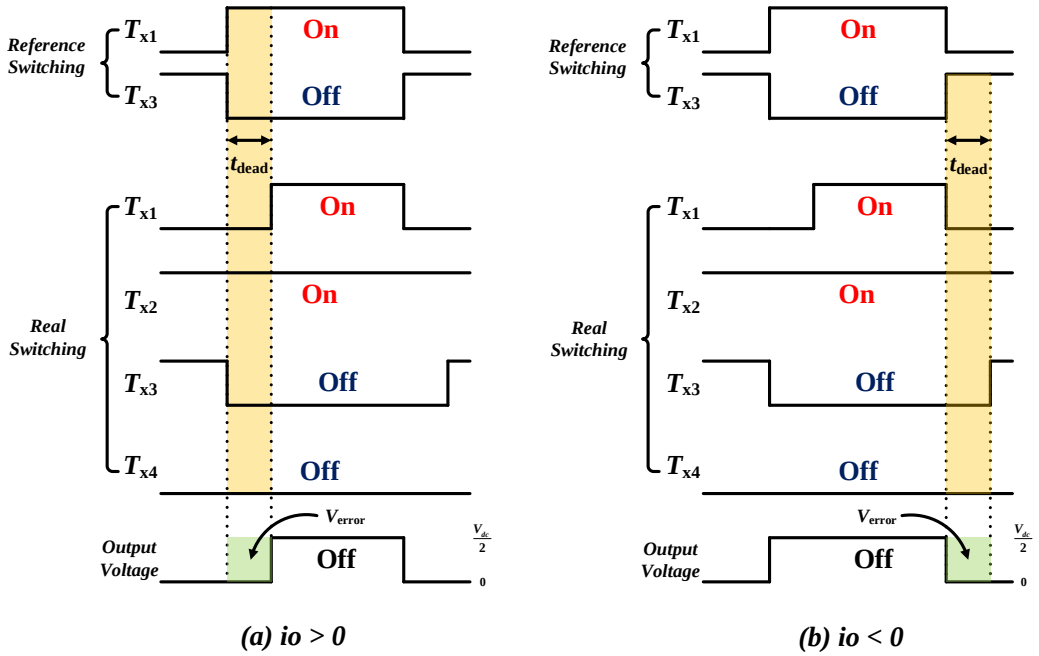


Figure 6. Switching state and output voltage during dead time.

3. Proposed Zero Dead-Time PWM Method

In this section, we describe the proposed zero dead-time PWM (ZDPWM) which totally removes dead-time utilization for PWM generation, in order to improve the previously explained current distortion caused by dead time in a three-level NPC inverter.

Figure 7 shows the switching mode according to the reference voltage and phase current. The proposed method focuses on turning on the switching devices which are flowing the current, and is divided into four operation areas depending on the direction of the reference voltage and phase current as shown in Figure 7b–e. The reference voltage and phase current conditions in each section are as follows:

$$\begin{aligned} &In\ Secion\ 1,\ v_{x\_ref}\&i_{x\_out} > 0 \\ &In\ Secion\ 2,\ v_{x\_ref} < 0,\ i_{x\_out} > 0 \\ &In\ Secion\ 3,\ v_{x\_ref}\&i_{x\_out} < 0 \\ &In\ Secion\ 4,\ v_{x\_ref} > 0,\ i_{x\_out} < 0 \end{aligned} \tag{6}$$

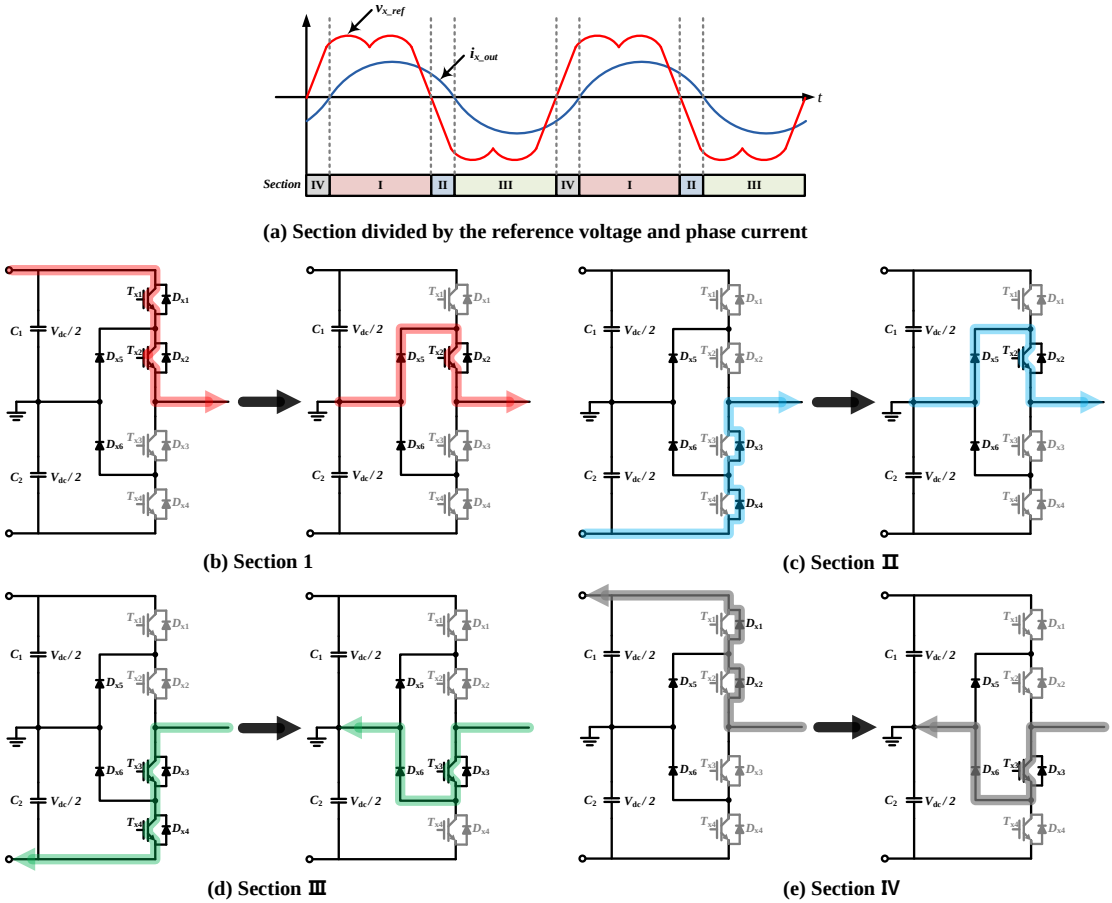


Figure 7. Switching state and current path according to each section divided by the reference voltage and phase current.

First, Figure 7b illustrates when the direction of the current is in the "+" direction. In section I, the switch T_{x3}, which is affected by dead time, does not turn on when switching from "positive" to "zero" state. Therefore, because it does not operate the more than three switching devices, there is no dead-time interval without implementing the complementary operation. Figure 7c illustrates when the direction of the current is in the "+" direction, as in case of Figure 7b. In Section II, switch T_{x3}, which is affected by dead time, does not turn on when switching from the "negative" to "zero" state. Therefore, the complementary operation is also not performed in Section II. Figure 7d shows when the direction of the current is in the "−" direction. In Section III, the switch T_{x2}, which is affected by dead time does not turn on when switching from the "negative" to "zero" state. Thus, because it does not operate the more than three switching devices, there is also no implementation of the complementary operation. Figure 7e illustrates when the direction of the current is in the "+" direction, as in case of the Figure 7d. In Section IV, the switch T_{x2} does not turn on when switching from the "positive" to "zero" state. Therefore, the complementary operation is also not implemented in Section IV. As a result, the switching states can remove dead time from any of the operation modes as there is no short circuit fault resulted from turn on/off delay between the switching transient [30].

Figure 8 shows the switching signal and reference voltage waveforms of phase A of the proposed ZDPWM method used in the three-level NPC VSI. Depending on the direction of the output current, two offset voltages $V_{a\_offsetx}$ are generated, and the magnitude of the offset voltage is determined by the maximum modulation index (MI), as shown in Figure 8 and Equation (7) as:

$$\begin{aligned} &if\ i_{x\_out} > 0,\ then\ V_{a\_offset} = V_{a\_offset1} = +1.1547\ (modulation\ index) \\ &if\ i_{x\_out} < 0,\ then\ V_{a\_offset} = V_{a\_offset2} = -1.1547\ (modulation\ index) \end{aligned} \quad (7)$$

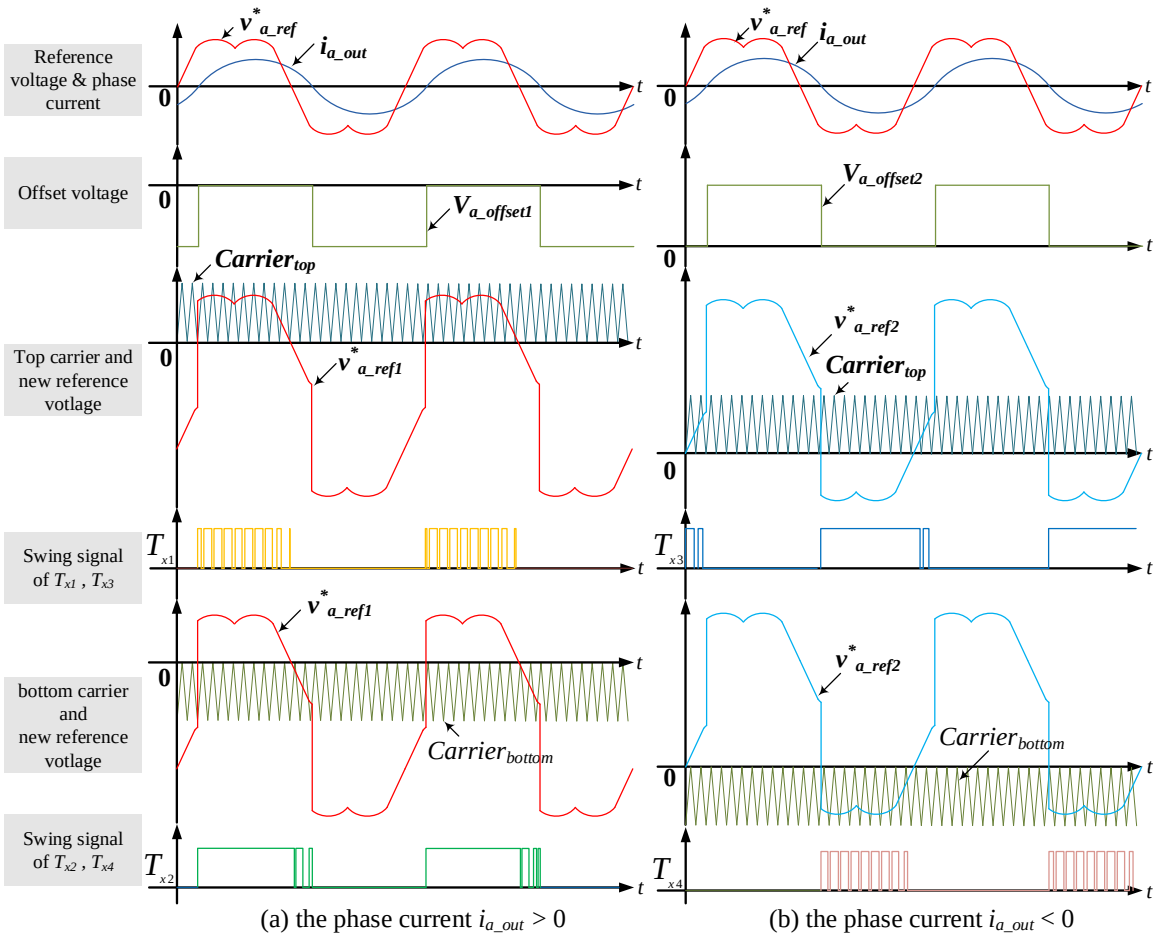


Figure 8. The switching signal and reference voltage waveforms of the proposed zero dead-time width modulation (ZDPWM) method.

The proposed technique is based on the SVPWM method; the maximum MI value of SVPWM is 1.1547. When the SVPWM generates a voltage reference from the output of the PI current controller, the offset value is designated as the maximum MI value, as described in Equation (7), in order to use the same maximum capable output voltage as the maximum voltage of SVPWM.

Two new reference voltages are generated by adding two offset voltage to the reference voltage, as shown in Figure 8. On the one hand, when $V^*_{a\_ref1}$, which is generated by merging with the "−" offset voltage, is greater than the upper carrier $Carrier_{top}$, the switching signal is generated by switch T_{x1}, and when $V^*_{a\_ref1}$ is greater than the lower carrier $Carrier_{bottom}$, the switching signal is generated by switch T_{x2}.

On the other hand, when $V^*_{a\_ref2}$, which is generated by merging with the "+" offset voltage, is less than the upper carrier $Carrier_{top}$, the switching signal is generated by switch T_{x3}, and when $V^*_{a\_ref2}$ is less than the lower carrier $Carrier_{bottom}$, the switching signal is generated by switch T_{x4}. The switching condition are expressed as follows:

$$\begin{aligned} &1)\ if\ v^*_{ref1} > Carrier_{Top},\ then\ T_{x1} = 1 \quad 2)\ if\ v^*_{ref1} > Carrier_{Bottom},\ then\ T_{x2} = 1 \\ &\qquad\qquad else\ T_{x1} = 0 \qquad\qquad\qquad\qquad\qquad\quad else\ T_{x2} = 0 \\ &3)\ if\ v^*_{ref2} < Carrier_{Top},\ then\ T_{x3} = 1 \quad 4)\ if\ v^*_{ref2} < Carrier_{Bottom},\ then\ T_{x4} = 1 \\ &\qquad\qquad else\ T_{x3} = 0 \qquad\qquad\qquad\qquad\qquad\quad else\ T_{x4} = 0 \end{aligned} \tag{8}$$

Therefore, in the proposed ZDPWM method, since each switching signal is compared only in each area, switches T_{x1} and T_{x3}, and switches T_{x2} and T_{x4} do not perform the complementary operation to each other, unlike conventional SPWM, SVPWM method.

Figure 9 also shows that, when using the proposed ZDPWM method, there is no need for dead time at the transition of each section. As shown in Figure 9, unlike conventional techniques, a switch can be seen to perform switching operations in each area, in contrast to conventional complementary operation. The switching state in the proposed ZDPWM technique can be defined as in Table 2.

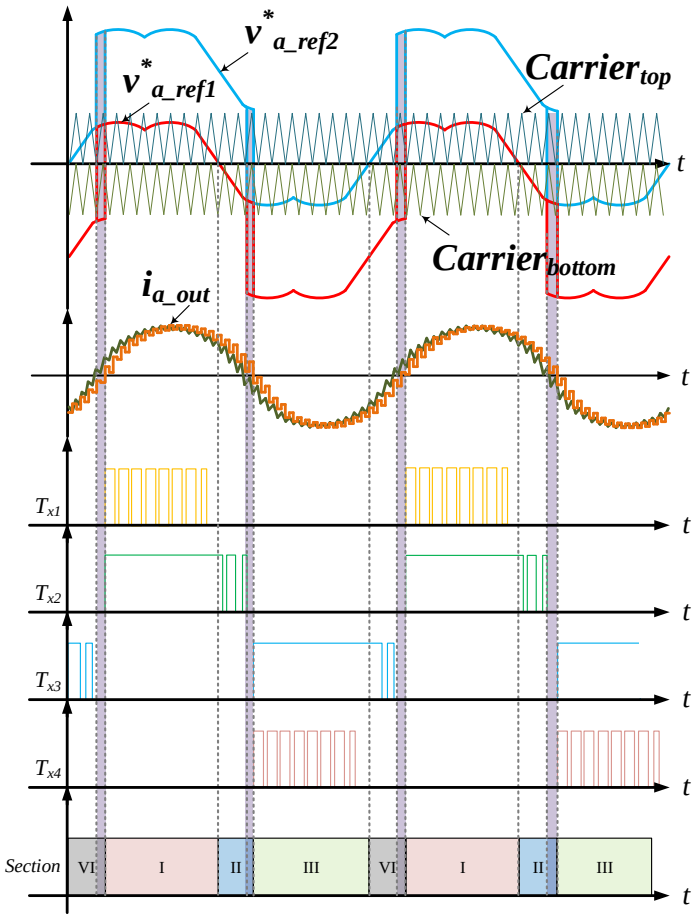


Figure 9. The switching signal and reference voltage whole waveforms of the proposed ZDPWM method.

Table 2. Switching state of the proposed ZDPWM depending on the section.

		Section I		**Section II**		**Section III**		**Section IV**	
State	Reference Voltage	Positive		Negative		Negative		Positive	
	Phase current	Positive		Positive		Negative		Negative	
	Phase Voltage	Positive	Zero	Negative	Zero	Negative	Zero	Positive	Zero
	Switch T_{x1}	On	Off	Off	Off	Off	Off	Off	Off
	Switch T_{x2}	On	On	Off	On	Off	Off	Off	Off
	Switch T_{x3}	Off	Off	On	Off	On	On	Off	On
	Switch T_{x4}	Off	Off	On	Off	On	Off	Off	Off

Figure 10 illustrates the determination of short-circuit accidents at the transition of a three-level NPC inverter using the proposed ZDPWM technique. Figure 10a shows the switching state of the four switches when transitioning from Section I to Section II. In Section I, T_{x1} and T_{x2} are determined by the top carrier, the bottom carrier, and the first reference voltage $v^*_{a\_ref1}$, and T_{x3} and T_{x4} are determined

by the second reference voltage $v^*_{a\_ref2}$. Due to this, transition from Section I to section II is not affected by short circuit accidents.

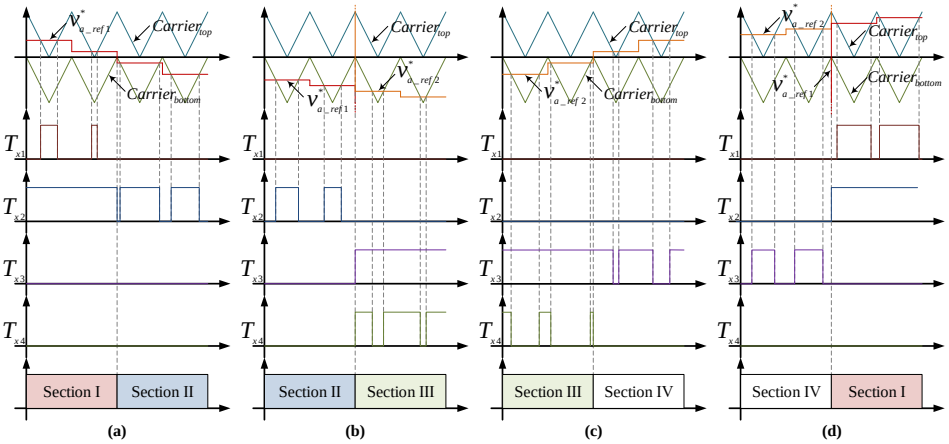


Figure 10. Switching state of proposed ZDPWM when transition of section: (**a**) from I to II; (**b**) from II to III; (**c**) from III to IV; (**d**) from IV to I.

Figure 10b shows the switching state when transitioning from Section II to Section III. Because switch T_{x1} was off when transitioning from Section I to Section II, it does not affect the state in Figure 10b. Switch T_{x2} is off before transitioning from Section II to Section III, and switches T_{x3} and T_{x4} are on at the transitioning from Section II to Section III. Due to this, transition from section II to section III is also not affected by short circuit accidents, because the three switches do not simultaneously change the state.

Figure 10c shows the switching state when transitioning from Section III to Section IV. Switches T_{x1} and T_{x2} are off state, switches T_{x3} are determined by the top carrier, bottom carrier, and second reference voltage $v^*_{a\_ref2}$, and switch T_{x4} are switched off when transitioning from Section III to Section IV. Therefore, no short circuit accident is occurred because the three switches do not change the state simultaneously.

Figure 10d shows the switching state when transitioning from Section IV to Section I. Three switches are turned on when the section is changed, but no short circuit accident occurs because switches T_{x1} and T_{x2} do not change at the same time.

Figure 11 shows a control block diagram of the proposed ZDPWM technique based on previous illustration. As shown on the figure, it can be easily implemented based on the SVPWM technique.

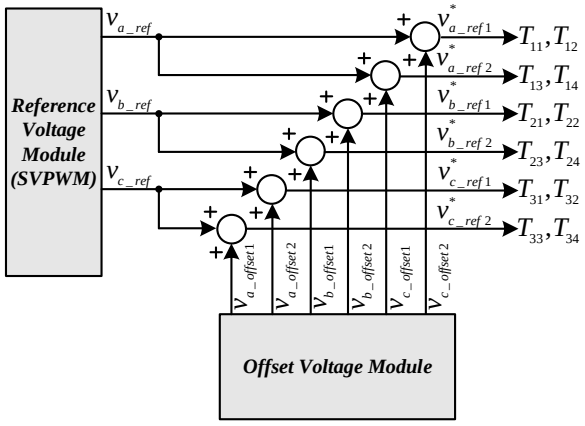


Figure 11. Control block diagram of proposed ZDPWM method.

However, since this method determines the offset of reference voltage according to the polarity of the phase current, unexpected distortion may occur if the delay occurs in the analog-to-digital

converter (ADC) modules that senses the phase current. Therefore, in this paper, simple phase delay modeling was performed, and it was applied to the proposed ZDPWM method.

4. Phase Delay Modeling and Compensation Method

In this section we describe the problems that can arise when the proposed ZDPWM technique is actually implemented and how to optimize it.

Figure 12 shows the delay in sampling data caused by the ADC module in MCU. Since the sampling period of ADC modules is determined using the interrupt of the PWM modules in MCU, the initiation of the ADC for real-time data sampling is associated with the switching period, as shown in Figure 12. The ADC modules which sense the current needs more than a certain amount of time to converter analog-to-digital data. Therefore, the phase current data are not immediately converted at the beginning of the sampling, and the data sampled at the previous time is used at the start of the next sampling. The sampled phase current is calculated as the lagging current relative to the real current and, consequently, the current controller or voltage controller of the inverter is operated through these sampled current data.

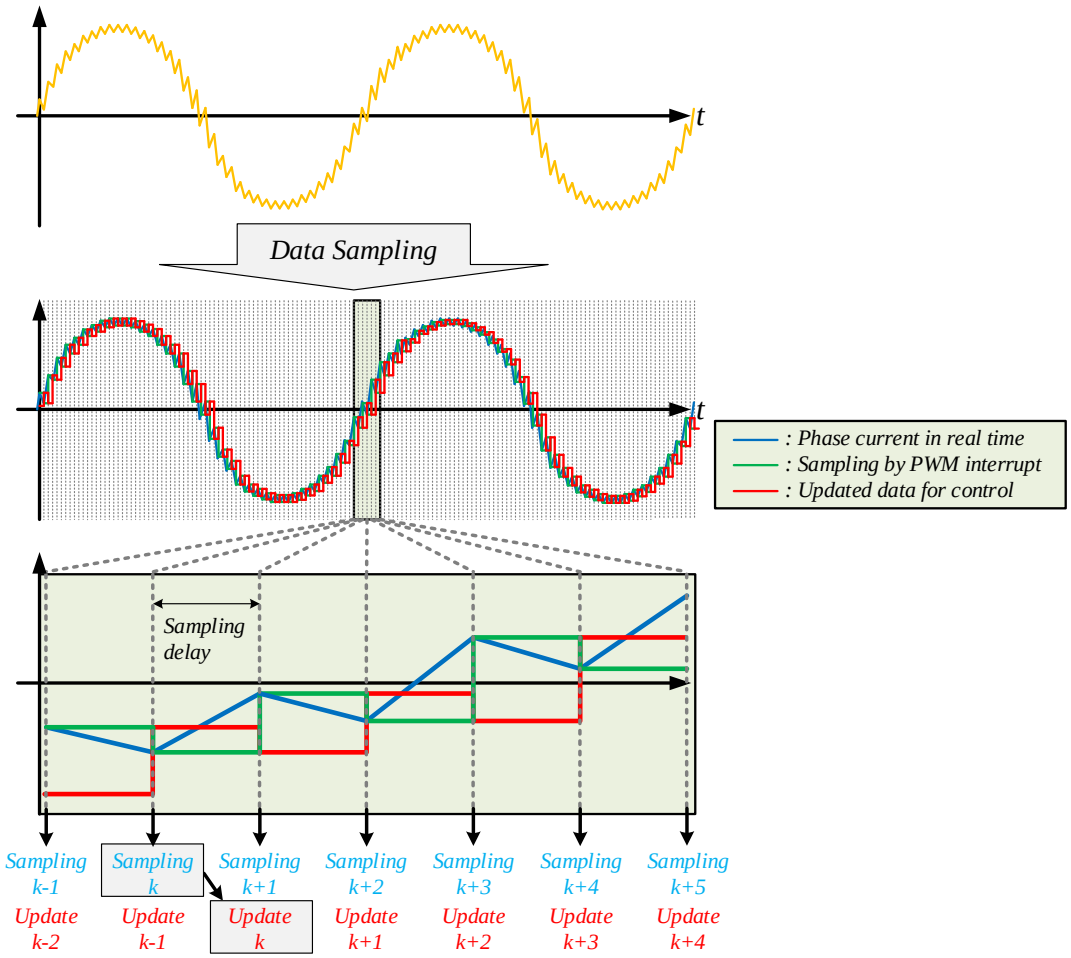


Figure 12. Sampling delay caused by analog-to-digital converter (ADC) module in a microcontroller unit (MCU).

When the conventional PWM is used, it does not significantly affect switching operation even if it is sensed as a lagging current, because the delayed phase is compensated by using the d-axis current control. However, in the case of the proposed ZDPWM, because the phase of voltage and current are shifted by the sampling delay, it causes a delayed transition of the operation section. This delay of section transition delays the recognition of the zero-crossing of the phase current and causes distortion

of the phase current. This delay of section transition also cannot be improved by only the d-axis control used in the conventional SPWM, SVPWM method. Therefore, the sampling delay should be improved to have the same phase with real current for the ideal operation of the proposed ZDPWM method.

The sampling delay t_{delay} can be calculated by Equation (9) as:

$$t_{delay} = \frac{1}{f_{sw}} \tag{9}$$

where f_{sw} is the switching frequency of the inverter. The relation formula both the delay angle of phase current, which is output AC phase, and the sampling delay are calculated through proportional trigonometric equation as follows:

$$2\pi : \frac{1}{f_{ref}} = \theta_{delay} : t_{delay} \tag{10}$$

In Equation (10), f_{ref} is the frequency of the reference voltage. In this paper, we propose the sampling delay compensation method through phase angle of d-q transformation using the delay angle which is calculated from the Equation (11) as:

$$\theta_{delay} = \frac{2\pi f_{ref}}{f_{sw}} \tag{11}$$

The delayed phase current through sampling can be defined as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I_{peak}\cos(\theta - \theta_{delay}) \\ I_{peak}\cos(\theta - 2\pi/3 - \theta_{delay}) \\ I_{peak}\cos(\theta + 2\pi/3 - \theta_{delay}) \end{bmatrix} \tag{12}$$

Equation (12) can be expressed as a d-q axis current using the d-q transformation as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} T(0)R(\theta - \theta_{delay}) = \begin{bmatrix} I_q^e \\ I_d^e \end{bmatrix} = \begin{bmatrix} I_{peak}\cos(0) \\ I_{peak}\sin(0) \end{bmatrix} \left(T(0) = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}, R(\theta) = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \right) \tag{13}$$

In general, the phase angle which is used in d-q transformation is obtained by phase locked loop (PLL). $T(0)$ and $R(\theta)$ are transfer matrix of the Park transformation and Clark Transformation. As shown in the Equation (13), finally, the current of d and q axis does not affect the sampling delay of the ADC modules.

Therefore, to prevent the phase delay caused by the sampling delay, as shown in Equation (14), the delayed phase angle obtained by Equation (11) is compensated when performing the reverse d-q transformation as:

$$\begin{bmatrix} I_q^e \\ I_d^e \end{bmatrix} R^{-1}(\{\theta - \theta_{delay}\} + \theta_{delay})T^{-1}(0) = \begin{bmatrix} I_{peak}\cos(\theta) \\ I_{peak}\cos(\theta - 2\pi/3) \\ I_{peak}\cos(\theta + 2\pi/3) \end{bmatrix} \tag{14}$$

Figure 13 shows a flowchart to compensate for the phase angle delay of the phase current. When sensing the current, as shown in Figure 13, the phase angle of the current is delayed by the sampling delay. This delayed current is converted to a synchronous reference frame via d-q transformation, and harmonics within this value are removed by digital filters such as low pass filter. Then, the values of these converted synchronous reference frame are converted to a stationary reference frame again using the compensated phase angle shown in the Equation (14) via reverse d-q transformation. Therefore, the proposed ZDPWM method can use the phase current, which is not delayed, to calculate the offset voltage. The phase angle used in this time is compensated as much as it is delayed.

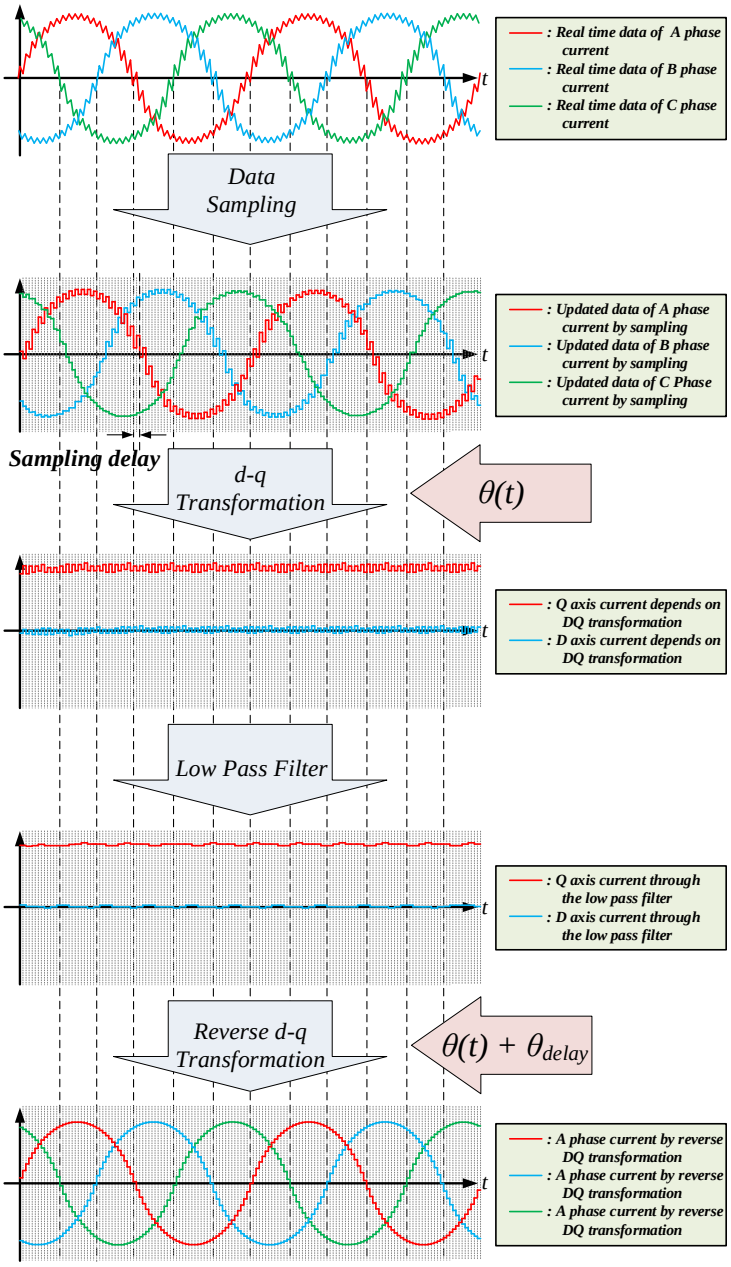


Figure 13. Flowchart of the compensating of the delayed phase angle of the phase current.

5. Simulation and Experimental Results

In order to verify the principle and feasibility of the proposed ZDPWM method, a simulation was developed using the PSIM software program. The simulation schematic in which the three-level NPC VSI back-to-back system is illustrated in Figure 14. The systems parameters of the simulation are shown in Table 3.

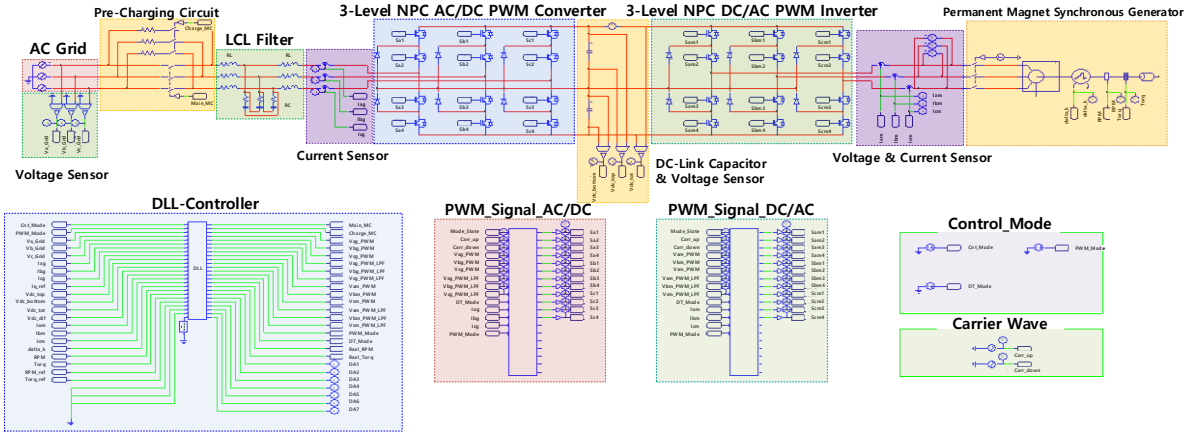


Figure 14. Three-level NPC VSI back-to-back schematic used in simulation.

Table 3. Simulation parameters.

Parameter		Conventional PWM Method		Proposed PWM Method	
		Value	Unit	Value	Unit
Dead time		5	(μs)	0	(μs)
Input voltage		380	(Vrms)	380	(Vrms)
Grid frequency		60	(Hz)	60	(Hz)
Switching frequency		10	(kHz)	10	(kHz)
DC-link capacitance		6000	(μF)	6000	(μF)
DC-link voltage		650	(Vdc)	650	(Vdc)
LCL filter	Grid side filter inductance	700	(μH)	700	(μH)
	Filter capacitance	10	(μF)	10	(μF)
	Converter side filter inductance	1000	(μH)	1000	(μH)
PMSG	Maximum speed	190	(rpm)	190	(rpm)
	Resistance	0.466	(ohm)	0.466	(ohm)
	Inductance	12.975	(mH)	12.975	(mH)
	Pole	24	(pole)	24	(pole)
	Maximum torque	670	(Nm)	670	(Nm)

Figure 15 shows the results of a permanent magnet synchronous motor (PMSG) torque control simulation using a conventional SVPWM with dead time. When the control starts, the grid side inverter operates as a converter to perform voltage control. After reaching the normal state, the torque command is applied to the load side inverter at 0 → 670 (Nm) → −670 (Nm) → 670 (Nm). From the top, it shows dc-link voltage, torque, grid side measured current, grid side reference voltages, and current and reference voltages to motor load. In order to figure out the dead-time effect, grid side current, LCL filter current, and motor current are shown on Figure 16. As previously explained, dead time is applied to prevent a short circuit accident, but it causes current distortion. This distortion appears in the form of low-order harmonics when performing fast Fourier transform (FFT) analysis, as shown in Figure 17.

Figure 18 shows the simulation results when applying the proposed ZDPWM in the same conditions without dead time as the previous SVPWM. The applied load is the same as the previous condition 0 → 670 (Nm) → −670 (Nm) → 670 (Nm). As shown in Figure 19, the proposed ZDPWM does not use dead time, and current distortion cannot be seen caused by dead-time effect of the current in the grid side, the LCL filter, and the load motor. Thus, the FFT analysis, as shown in Figure 20, indicate that the low-order harmonics produced by dead time are significantly reduced as compared with SVPWM.

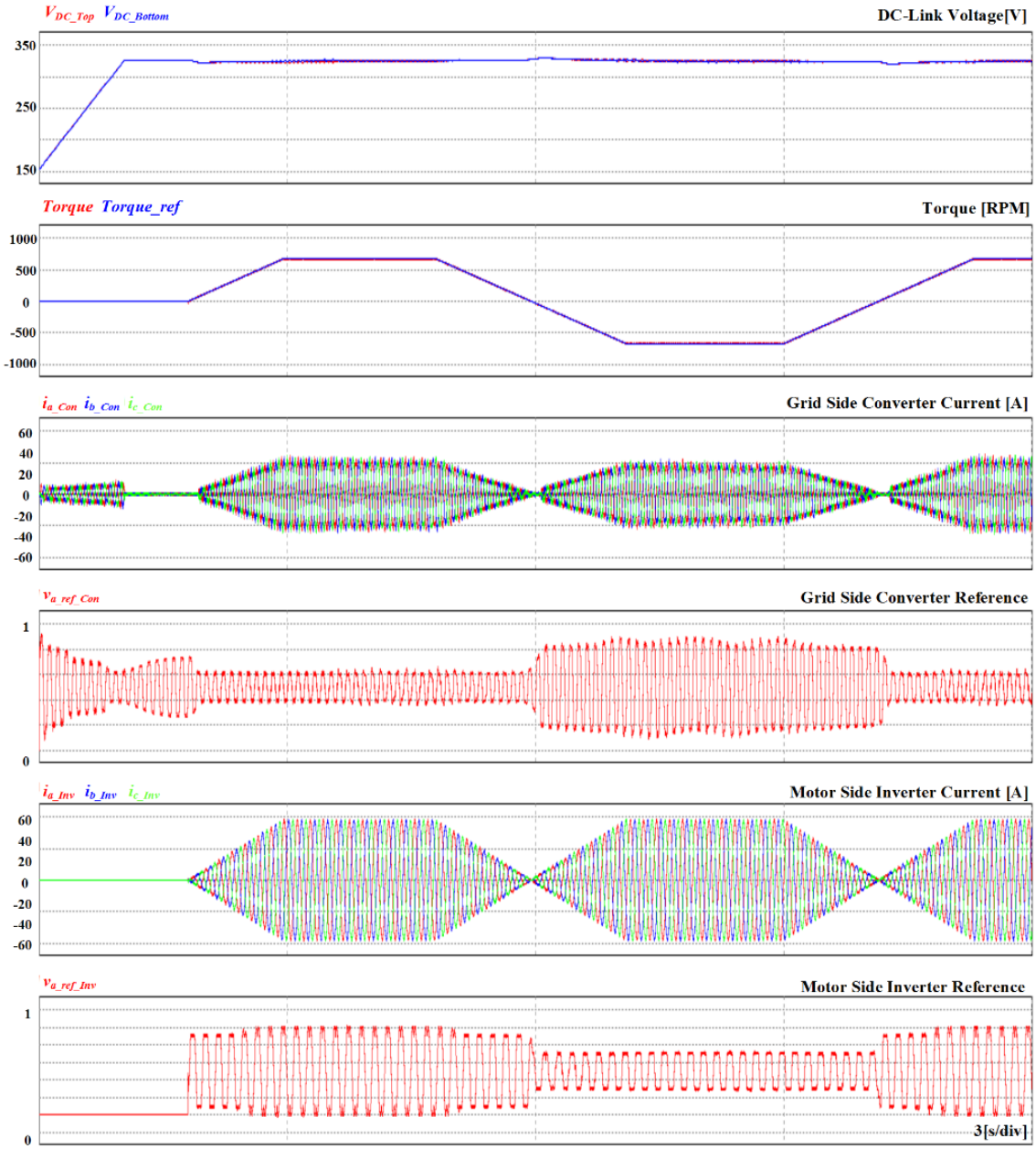


Figure 15. Simulation results of PMSG torque control using the conventional space vector pulse width modulation (SVPWM) with dead time.

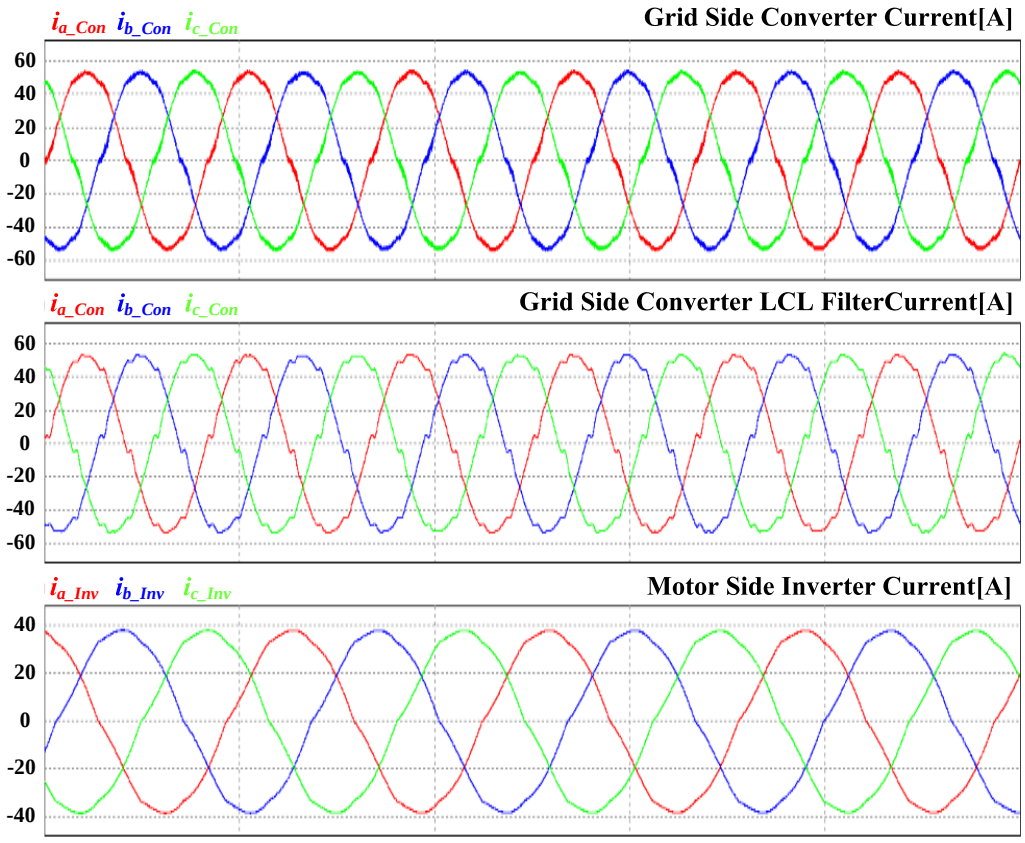


Figure 16. Simulation results of grid side current, LCL filter current, and three-phase motor current using the conventional SVPWM with dead time.

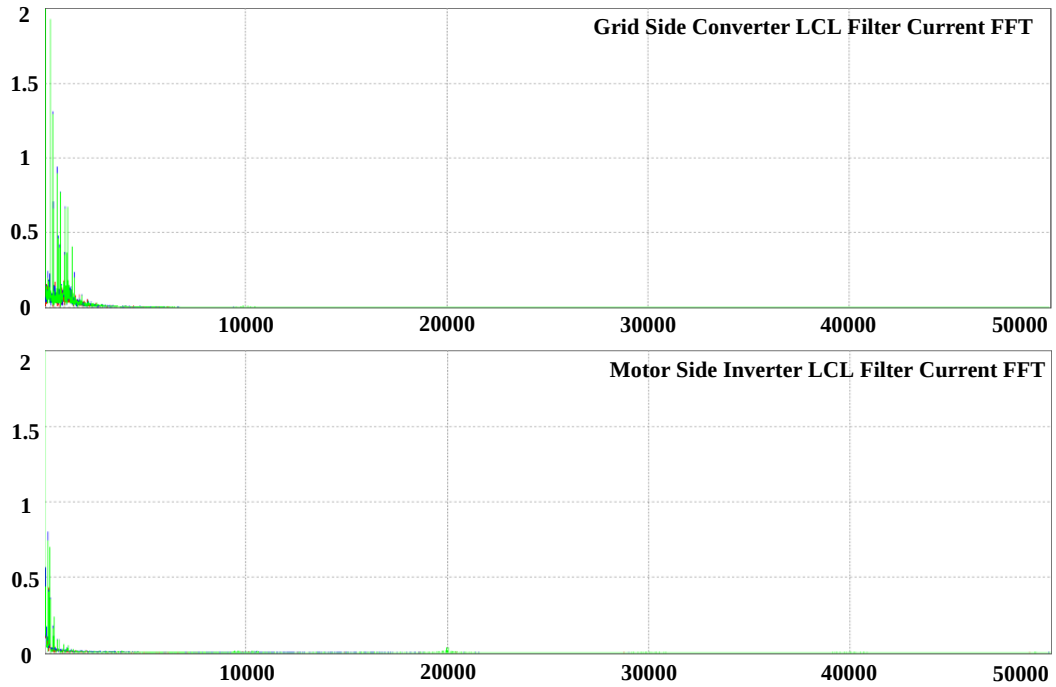


Figure 17. Fast Fourier transform (FFT) analysis results of grid side LCL filter current and motor side current using the conventional SVPWM with the dead time.

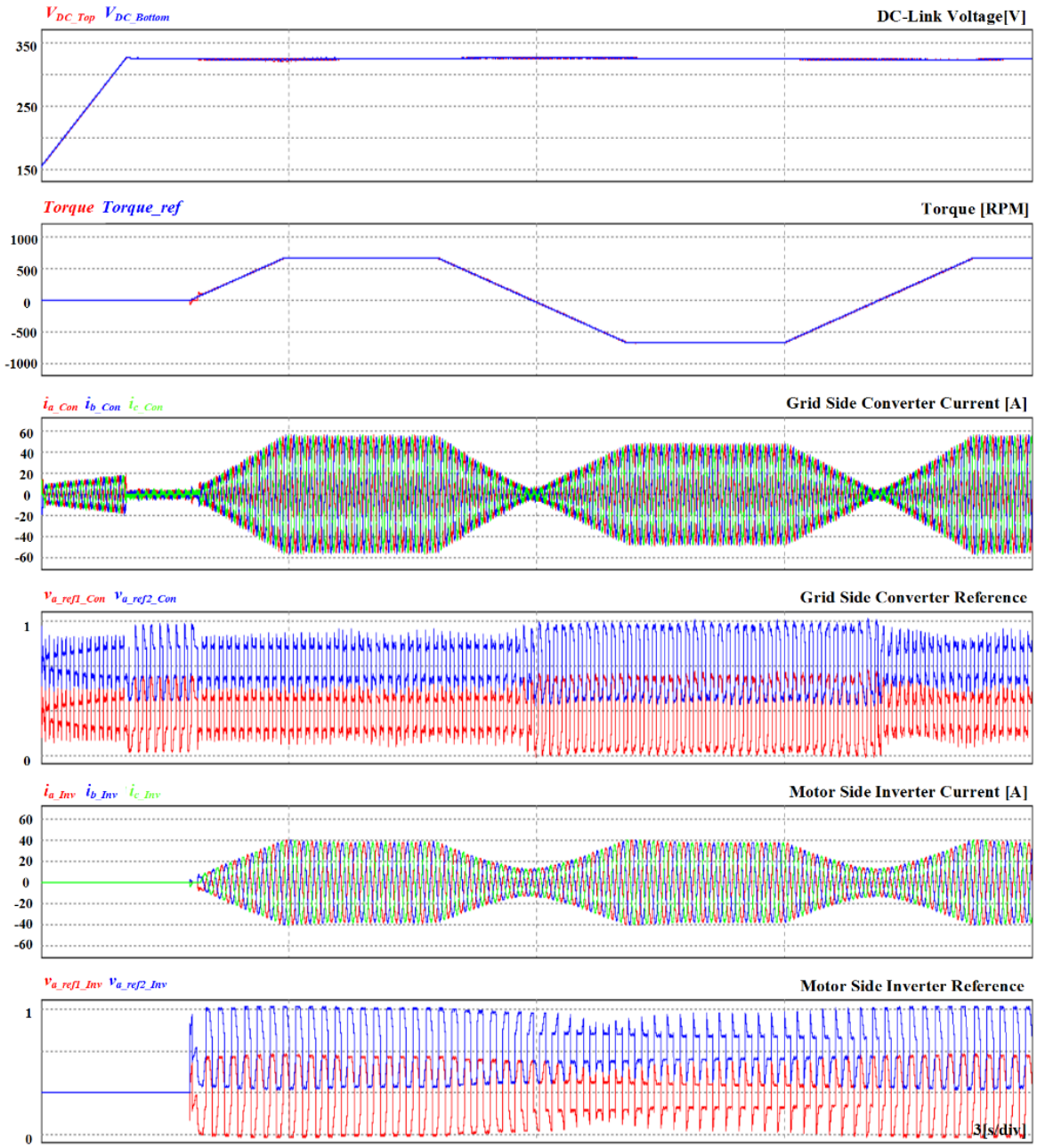


Figure 18. Simulation results of PMSG torque control using the conventional using the proposed ZDPWM method.

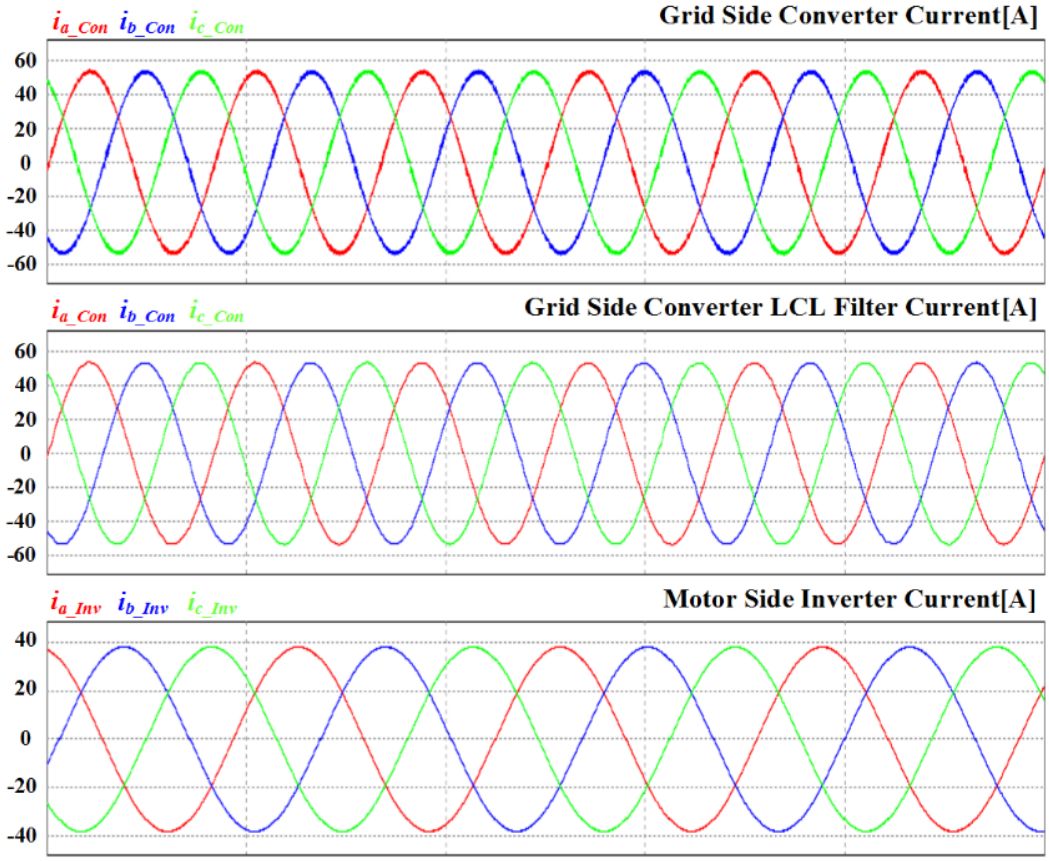


Figure 19. Simulation results of grid side current, LCL filter current and three-phase motor current using the proposed ZDPWM method.

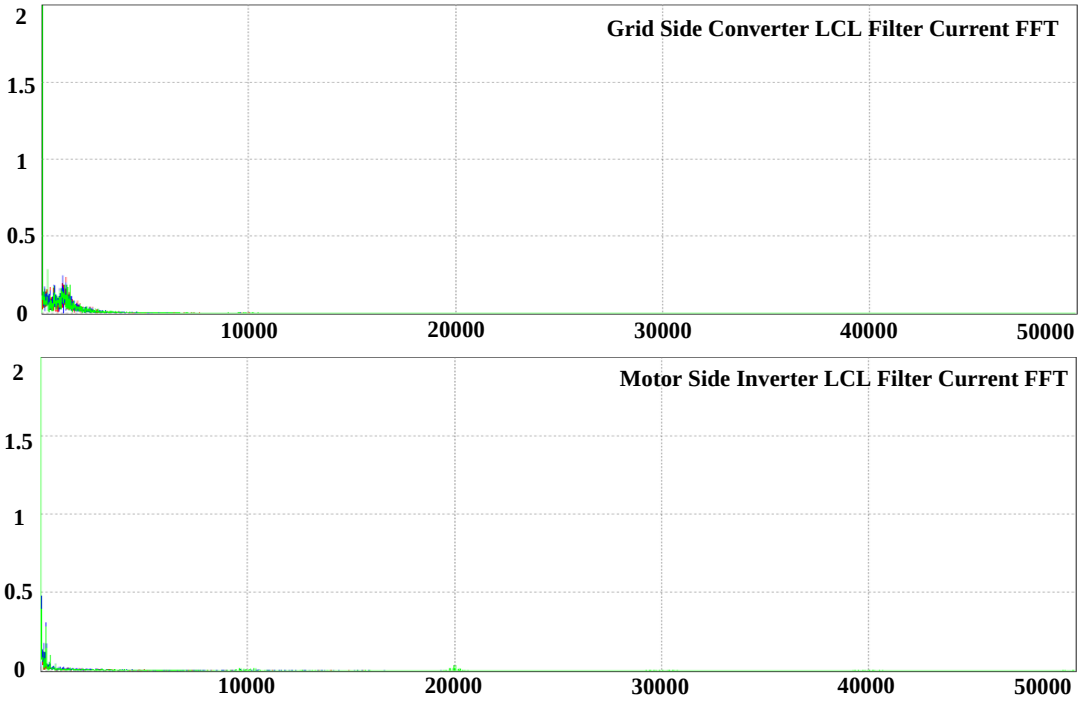


Figure 20. FFT analysis results of grid side LCL filter current and motor side current using the proposed ZDPWM method.

Figure 21 shows the comparison simulation result of the conventional SVPWM and proposed ZDPWM method. As previously mentioned, when using the conventional SVPWM method, dead time increases the distortion in the phase current, which causes an increase in the THD. However, the proposed ZDPWM method does not require dead time because it does not perform a complementary operation, as shown in Figure 21, and therefore it reduces the distortion in the phase current. Consequently, when using the conventional SVPWM method with dead time, the THD of the current is about 2.4%, but the THD of the current is about 1.2% when using the proposed method.

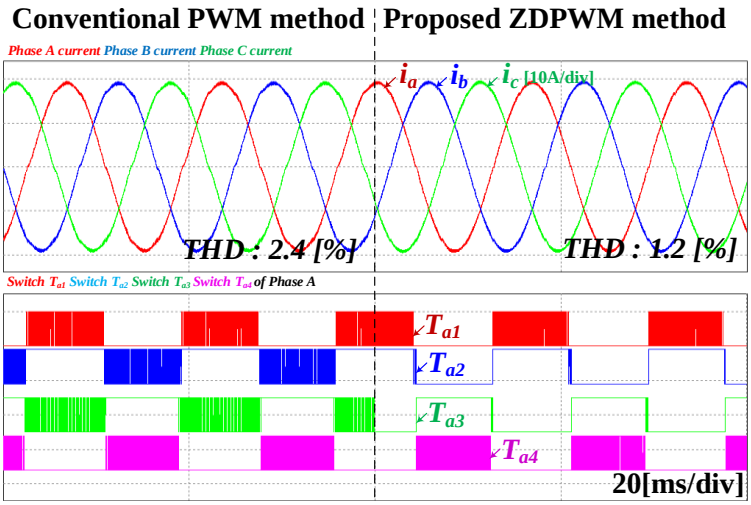
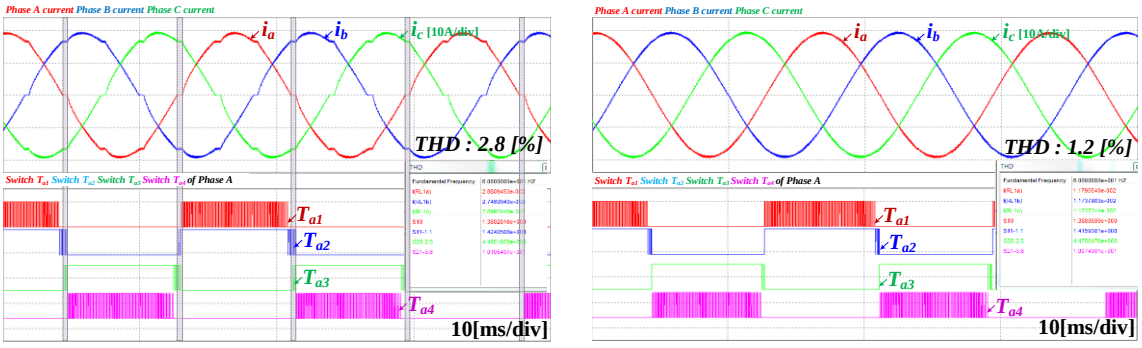


Figure 21. Simulation results of the conventional SVPWM method and proposed ZDPWM method with delay compensation applied in three-level NPC VSI (20 ms/div).

Figure 22 also shows the simulation waveforms before and after applying proposed ZDPWM with sampling delay compensation. We can see that the proposed ZDPWM method is more distorted by the sampling delay of the phase current at the section where it is transmitted, as shown in Figure 22a. At this time, the THD of current is about 2.8% and is higher than the conventional SVPWM method. Figure 22b shows that by compensating the delay, the distortion caused by the delay is reduced.



(**a**) (**b**)

Figure 22. Simulation results of the proposed ZDPWM method applied in three-level NPC VSI: (**a**) Without delay compensation (10 ms/div); (**b**) With delay compensation (10 ms/div).

In this case, the compensated phase angle, which is calculated by using the Equation (11), is shown in Figure 23. Therefore, although the phase of the sensed current is delayed more than the real current, the phase current used in the proposed ZDPWM method has the same phase as the real current because delay is compensated during the reverse d-q transformation.

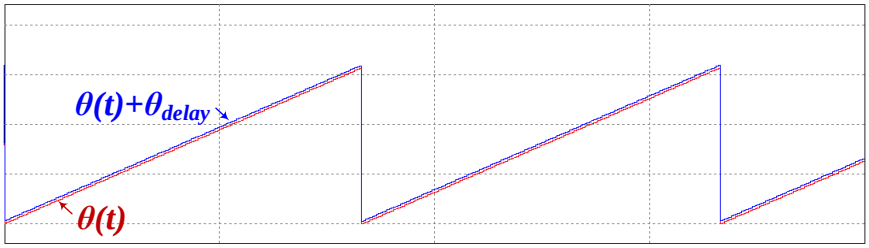


Figure 23. Simulation results of the real phase angle and compensated phase angle.

Simulation results of three methods are summarized as Table 4. The THD characteristics of the conventional SVPWM, proposed ZDPWM without delay compensation and proposed ZDPWM with delay compensation are 2.4%, 2.8%, 1.2% respectively. As a result, proposed ZDPWM with delay compensation is the best method to improve current distortion of a three-level NPC inverter.

Table 4. Comparison of the THD characteristics of the conventional SVPWM and proposed methods.

Control Method	THD (%)
Conventional SVPWM (5μs dead time)	2.4
Proposed ZDPWM without sampling delay compensation (no dead time)	2.8
Proposed ZDPWM with sampling delay compensation (no dead time)	1.2

In addition, in the NPC topology, in this paper, voltage unbalancing occurs in the dc-link due to load condition, difference in charging/discharging status according to current direction, etc. Therefore, as illustrated in [31,32], voltage balancing in dc-link is generally achieved by applying offset voltage to the PWM output from SVPWM, PSPWM, or LSPWM. In this paper, we also applied offset voltage to compensate dc-link unbalancing at the output end of ZDPWM, and conducted simulation by applying offset voltage the same as the conventional SVPWM.

Figures 24 and 25 show the simulation results applying SVPWM and the proposed ZDPWM in a three-level inverter, respectively. As shown in the figure, all applications in this paper perform voltage balance control, and therefore the dc-link voltage imbalance in the upper/lower capacitors does not occur.

An experiment was performed to verify the feasibility of the proposed ZDPWM method applied in a three-level NPC VSI. The configurations of the experimental system and power stacks are as follows in Figures 26 and 27.

The controller is implemented on TMS320F28346 and that of a floating point microcontroller unit at 300 MHz rate frequency. The switching and sampling frequency is 10 kHz. The power is supplied to the three-level NPC inverter through the three-level NPC PWM converter.

Figure 28a shows the output phase current waveforms of each phase when the conventional SVPWM method is used in a three-level NPC VSI. In this experiment, the dead time was 5 us. As shown in Figure 28, we can see that dead time causes the distortion of the output current and, in particular, large distortion of the current, at zero crossing points. Figure 28b shows the phase A output current and reference voltage waveform, and the switching signal according to the reference voltage is generated, as shown in Figure 28c. As a result, it can be seen that the THD of the output current has deteriorated to about 2.5% due to the dead time.

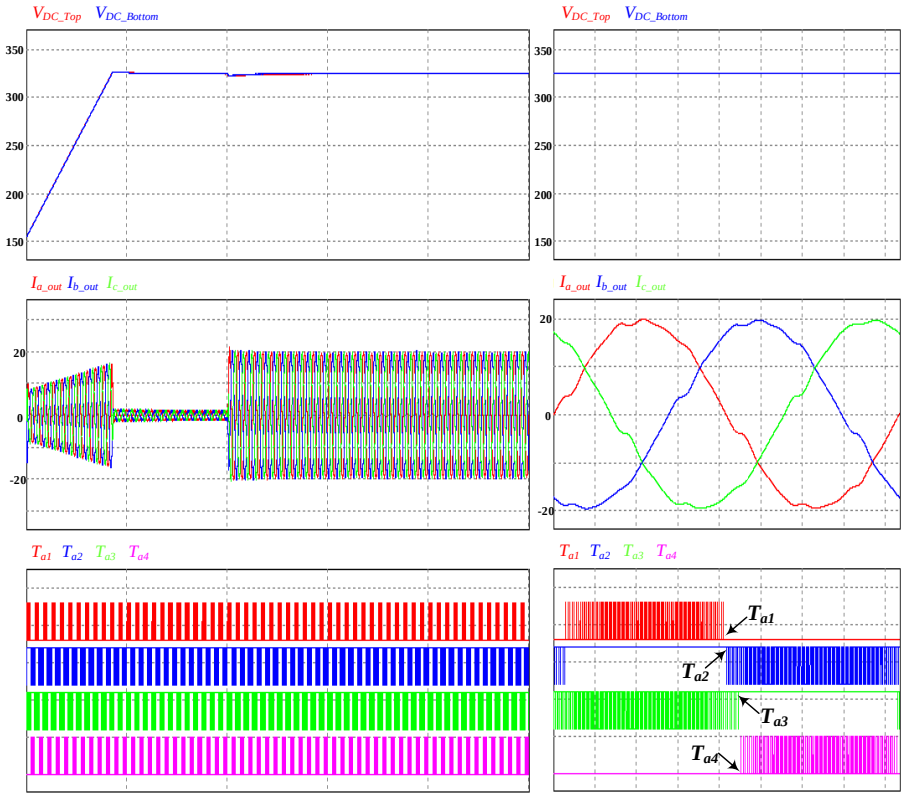


Figure 24. Simulation results using the dc-link balancing control applied in the SVPWM method.

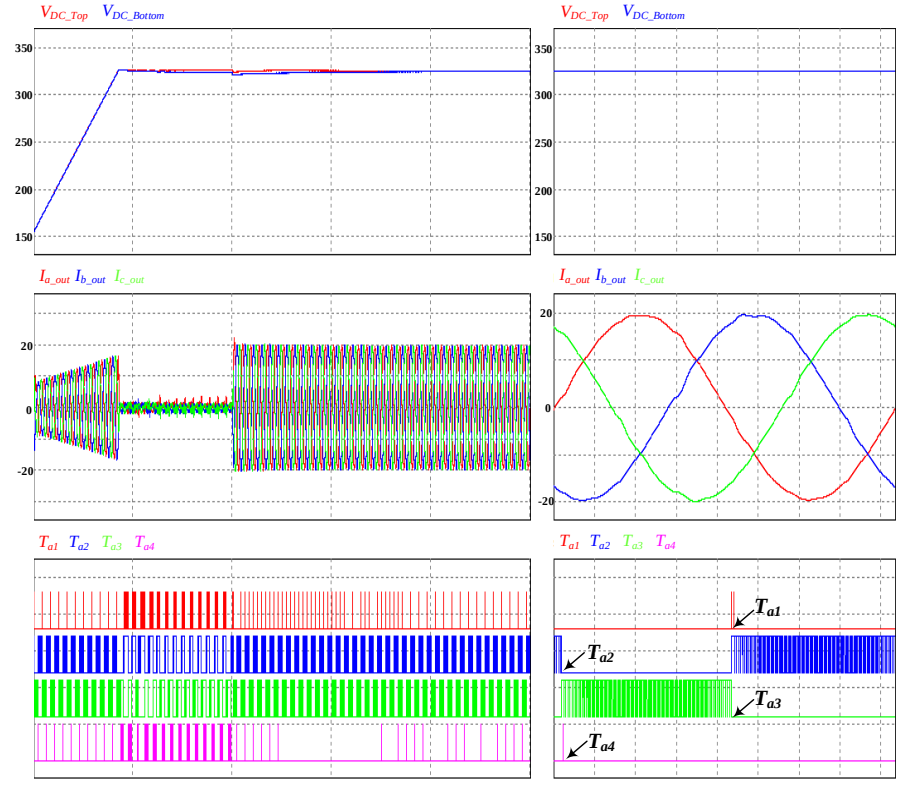


Figure 25. Simulation results using the dc-link balancing control applied in the proposed ZDPWM method.

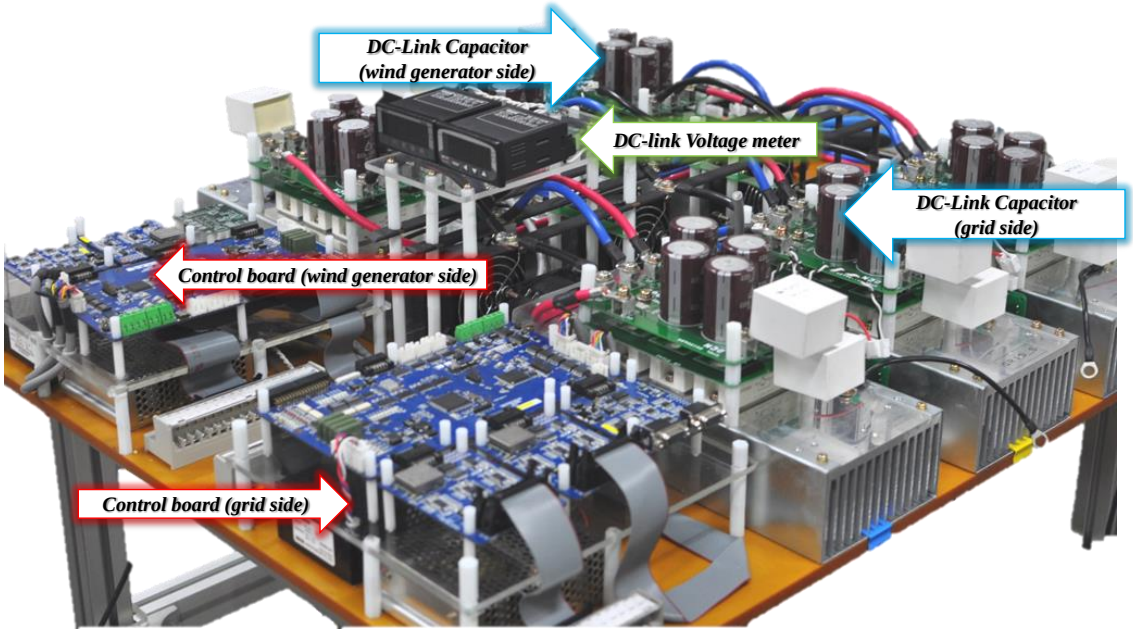
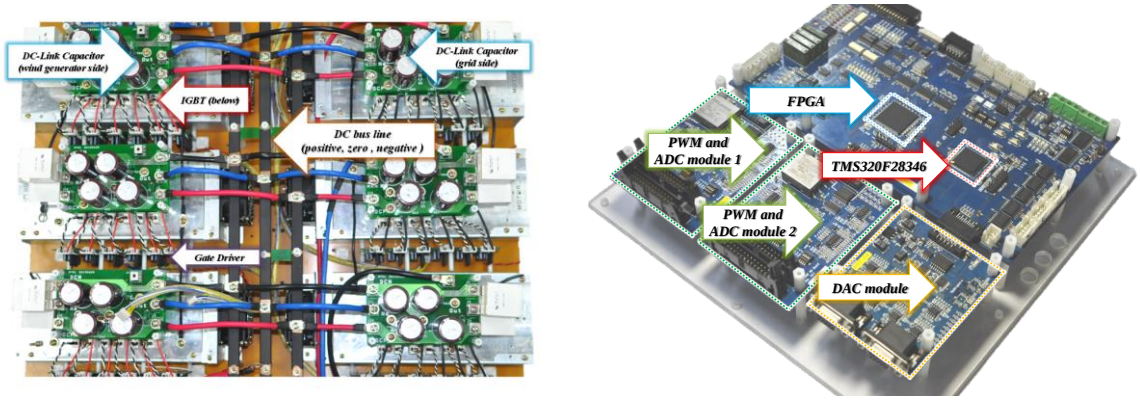


Figure 26. Configuration of the experimental system.



(**a**) (**b**)

Figure 27. Configuration of the experimental setup: (**a**) The dc-link, switching devices, and gate driver; (**b**) The control board.

Figure 29a shows the output phase current waveforms of each phase when the proposed ZDPWM method with delay compensation is used in a three-level NPC VSI. In this experiment, the dead time was not applied. Figure 29b shows the phase A output current and reference voltage waveform. Figure 29c shows the switching signal generated by two reference voltage which are adding the offset voltage to reference voltage. In the conventional SVPWM method, each switching signal is generated by applying the dead time in order to perform the complementary operation and prevent the short circuit, but in the proposed ZDPWM method, it is possible to verify that the switches T_{a1} and T_{a3}, and the switches T_{a2} and T_{a4} do not perform the complementary operation, as shown Figure 29d. As a result, we can see that the THD of the output current is about 1.2% better than the conventional SVPWM method by about 1.3%.

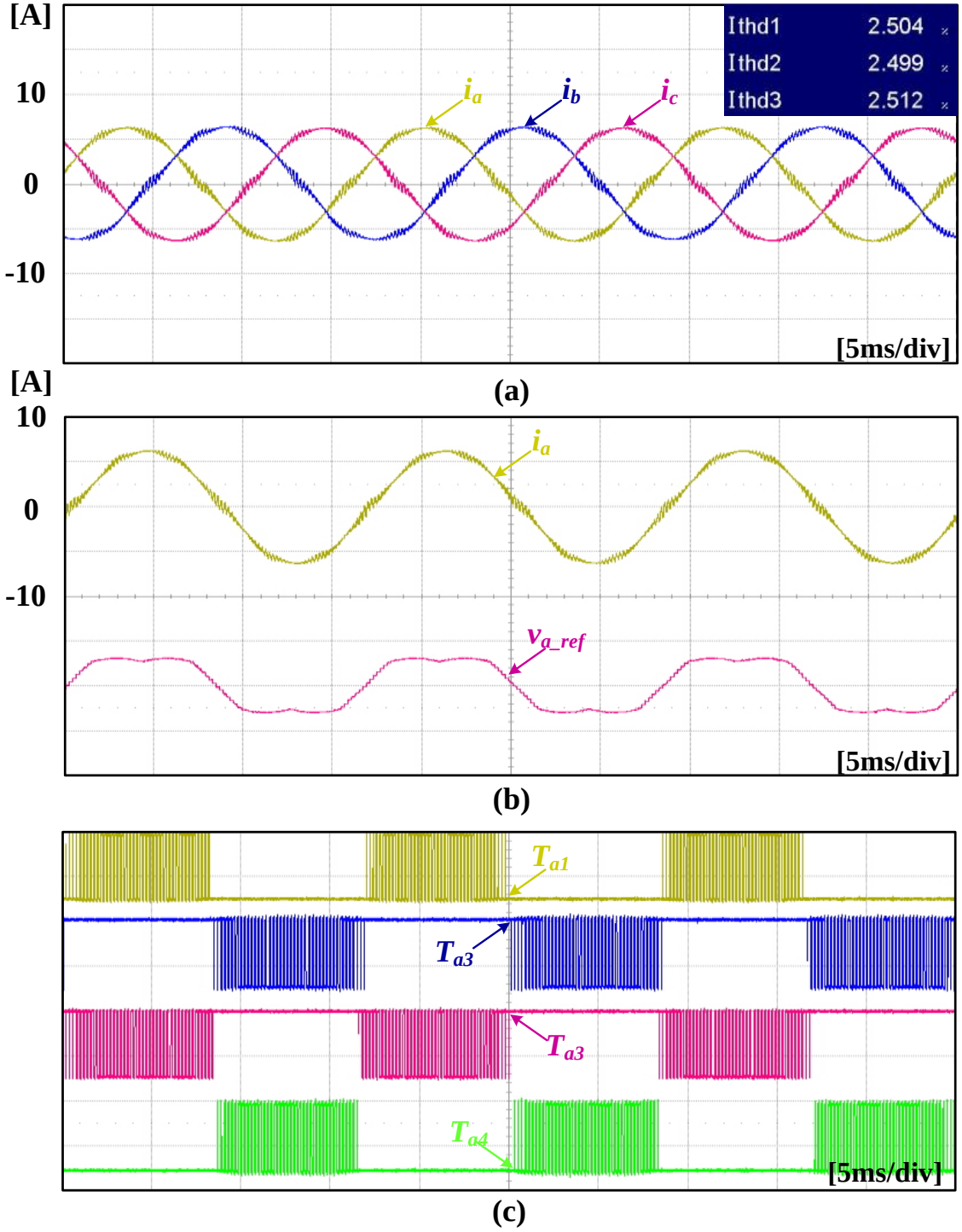


Figure 28. Waveforms of the experimental results using the conventional SVPWM method: (**a**) Each phase current; (**b**) Reference voltage; (**c**) Switching signal of the one leg switching devices.

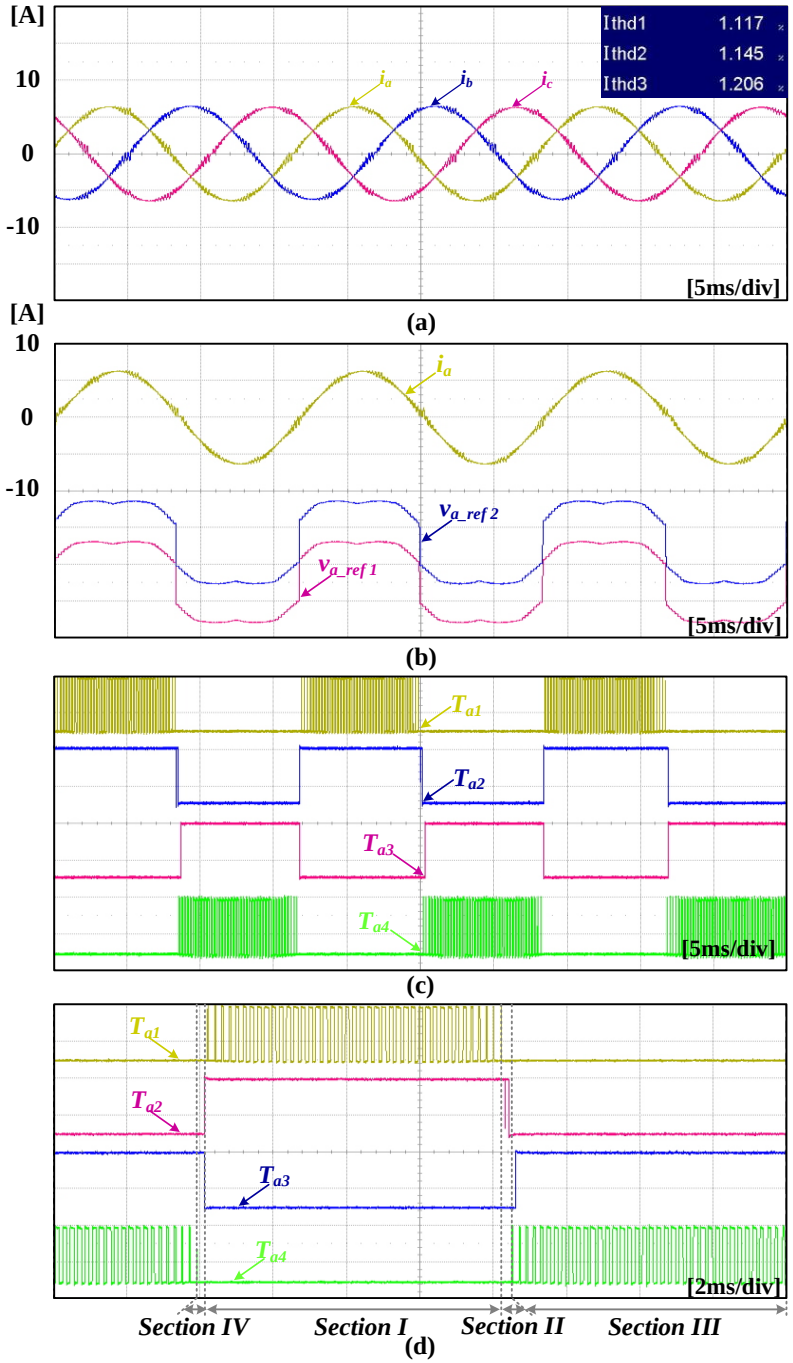


Figure 29. Waveforms of the experimental results using the proposed ZDPWM method with compensation method: (**a**) Each phase current; (**b**) Reference voltage; (**c**) Switching signal (5 ms/div); (**d**) Switching signal (2 ms/div).

6. Conclusions

In this paper, we have proposed the ZDPWM method with compensation of the sampling delay in three-level NPC VSI. It can reduce the current distortion caused by the dead time and it is easy to implement.

We discovered that complementary switching operation of the NPC VSI was the reason dead time was needed and we described how to operate the NPC VSI without dead time. In addition, the sampling delay modeling was described to compensate the delay of the phase current.

In this paper, a simulation and an experiment were performed and presented to verify the proposed ZDPWM method as well as their feasibility. From them, the proposed method resulted in better performance of lower current harmonic distortion.

From the simulation result, the current regulated by conventional SVPWM has a THD of about 2.4%, the current regulated by proposed ZDPWM without sampling delay compensation has a THD of about 2.8%, and the current regulated by proposed ZDPWM with sampling delay compensation has a THD of about 1.2%. Additionally, in experimental result shows that the current regulated by proposed ZDPWM without sampling delay compensation has a THD of about 2.5% and the current regulated by proposed ZDPWM with sampling delay compensation has a THD of about 1.2%, similar to the simulation result. These results indicate that THD can be significantly reduced by the proposed method. As a result, the proposed ZDPWM is a good PWM strategy for three-level NPC VSI systems.

Author Contributions: J.-W.K. and S.-W.H. conceived and designed the experiment; J.-W.K. and S.-W.H. performed the experiment; J.-W.K. and Y.K. analyzed the theory; J.-W.K. wrote the manuscript; H.L. reviewed the manuscript and search state-of-the art literature; J.-H.L. participated in research plan development and revised the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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