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A Novel General Purpose Combined DFVF/VCII Based Biomedical Amplifier

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Abstract: We here present a 0.15 µm CMOS high input impedance and low noise AC coupled flipped voltage follower-based amplifier for high integration level in integrated circuits in a wide range of sensing applications. With such a circuit, it is possible to achieve a high level of integration, thanks to the absence of passive resistors, and also to implement a very high input impedance without capacitive feedback thanks to bootstrap operation, thus offering a very low high-pass cutoff frequency. Simulated results with a proven and well modeled standard technology show a whole circuit input-referred noise of 5.4 µVrms. The bias voltage is ±0.6 V with a total power consumption of the single amplifier of 20 µW. The very low circuit complexity allows a very low estimated reduced area occupation giving, as a general example, the possibility of integrating an array of up to thousands of channels for biomedical applications. Detailed simulation results, PVT analysis and comparison tables are also presented in the paper.

Keywords: CMOS technology; High input Impedance; DFVF; VCII

1. Introduction

The acquisition and recording of low-frequency and low-amplitude signals for photonics, automotive, biomedical and structural applications is of fundamental importance in current electronic systems: as an example, the acquisition of very noisy signals is at the foundation of understanding brain functions [1–10]. Bioelectric signal sensing, in particular, is a challenging feature in both daily healthcare and prevention.

A general electrical biosignal is characterized by very low amplitude and also by the fact that is buried in noise. As widely reported in the literature, neuro signals have a very low electrical amplitude, up to 1 mV_{pp}, and their frequency ranges between 0.5 Hz and 10 kHz. They can be classified into two groups: local-field potentials (LFPs) and action potentials (APs). The first group is characterized by very slow signals, where the frequency is in the range ~ (0.5 Hz–1 kHz), while in the second group, the neuro signals present a rapid amplitude variation forming a series of spikes; therefore, the frequency is higher and falls in the range ~ (0.3 Hz–10 kHz). Moreover, these signals are characterized by an amplitude that is inversely proportional to the frequency, causing faster signals, such as AP to have an even smaller amplitude; therefore, proper amplification is required. With respect to heart signal monitoring, all the information for electrocardiography (ECG) is located in the ~ (0.05 Hz–100 Hz) range, while the voltage amplitude, considering conventional wet cloth electrodes, is below 0.5 V [11]. A challenging aspect of designing a general-purpose amplifier, however, is that there are applications where, instead, a large bandwidth may be of importance, as presented in [12,13]. A compromise is therefore necessary for the overall performance of the circuit.

In the literature, many electronic circuits and systems have been proposed in order to interface with and sense very low voltage signals from dedicated or general-purpose electrodes [14–20], even for

portable application [21], where the energy consumption is much more critical and energy harvesting techniques can be employed to remove the battery dependence or at least to increase the lifetime [22–26]. As a rule, the performances of these interfacing circuits, including, in most cases, buffers or amplifiers as a first stage, are limited by the DC gain, DC offset, noise, Common Mode Rejection Ratio (CMRR), and input impedance. Also, dimensions and power consumption are important features, especially in very low voltage, very low power applications, and also the limiting of heat dissipation. Finally, the on-chip area occupation, in addition to the features listed above, is often a fundamental requirement. Due to all the aforementioned aspects, electronic recording circuits and systems require a very low noise first interfacing stage that in most cases is formed by a high-impedance input voltage amplifier. Several architectures implementing such circuits have been proposed in the literature [27–33], but there is a continuous demand for novel and improved-performance topologies in order to achieve an ultra-large-scale integrated solution. In particular, in the biomedical acquisition system literature, different electronic interfaces have been proposed, in order to minimize the interference voltage contribution, usually by achieving a very high input impedance and high CMRR values. Most of these solutions are centered on the analysis of the frontend amplifier, which has to perform a differential reading with appropriate noise rejection; hence, its performance affects the overall behavior of the whole system.

In this work, in order to overcome the mentioned specifications tradeoff in terms of noise, power consumption, gain and space occupancy we propose a low complexity mixed operation mode (voltage/current) amplifier using two different circuit architectures. In particular, we combine a Differential Flipped Voltage Follower (DFVF) stage with a Second-Generation Voltage Conveyor (VCII) acting as transimpedance amplifier.

The proposed circuit was simulated in LTspice using a standard CMOS technology with very accurate 0.15 um foundry models, comparing the performance with state-of-the-art circuits. The proposed circuit has an input-referred noise of 5.4 μVrms. The supply voltage is ±0.6 V, with a total power consumption of the single amplifier of 20 μW.

This paper is organized as follows. In Section 2, a brief recall of DFVF and VCII are given while in Section 3 we describe in detail the proposed architecture and the design constraint of the proposed integrable circuit blocks. Simulation results are outlined in Section 4. Finally, Section 5 reports the conclusions of the paper.

2. Flipped Voltage Follower and Second-Generation Voltage Conveyor Short Overview

2.1. The Flipped Voltage Follower

The Flipped Voltage Follower (FVF) is basically a high input impedance low complexity high precision buffer. The FVF is also characterized by very low output impedance, requiring a very low static power dissipation.

The basic FVF circuit is reported in Figure 1a [34–41]. The applied signal V_{in} is buffered to the source of transistor M_1. In this case, a high value of input impedance, especially at low frequency, is given by the gate of transistor M_1, while a low output impedance is achieved due to the negative feedback loop implemented by the transistor M_2. Concerning the bias condition, the current flowing through M_1 is constant and fixed by the current generator I_B. The circuit load current is given by varying the current through M_2. Two different phases can be distinguished during normal operating conditions. The first phase is for the applied rising edge of V_{in}. In this case, the current is injected to the load; the transistor M_1 current is fixed to I_B while the M_2 current in is reduced, with the load current now being equal to $I_L = I_B - I_D(M_2)$. A maximum load current equal to I_B is delivered to the load when M_2 is switched off. In the second phase, the input signal falling edge is considered. In this case the current is taken from the load but, the current through M_1 being constant, this means that the M_2 current increases, and this is possible thanks to the negative feedback loop that increases the A node voltage increasing the gate applied voltage of M_2. In this last case, the total current of M_2 is given by I_L

+ I_B not being limited by I_B, but rather only being limited by the supply voltage. The output impedance is always low for both phases while the input impedance remains the same (gate terminal impedance).

The presented conventional FVF has a major drawback: it can deliver a sink load current greater than the bias current, but is limited in terms of delivering a maximum load current of I_B. For this reason, distortion phenomena may occur in normal operation when large input signals are applied, or extremely low operation voltages required. To overcome this limitation, improved topologies have been presented in the literature. For example, Figure 1b shows a modified FVF architecture that is able to deliver a load current larger than the applied bias. In this topology, the M_1 current is not fixed by a constant current source as in Figure 1a; in this way, it can provide a load current in both phases that is greater than its bias current. The only limitation of this modified architecture is that during the second phase, when high input signals are applied, the feedback loop does not work properly anymore, and the buffer functionality is performed by the simple common drain transistor M_1. In this last case, the FVF output impedance becomes $1/g_{m1}$, which is different from the first phase output impedance because the feedback is very low.

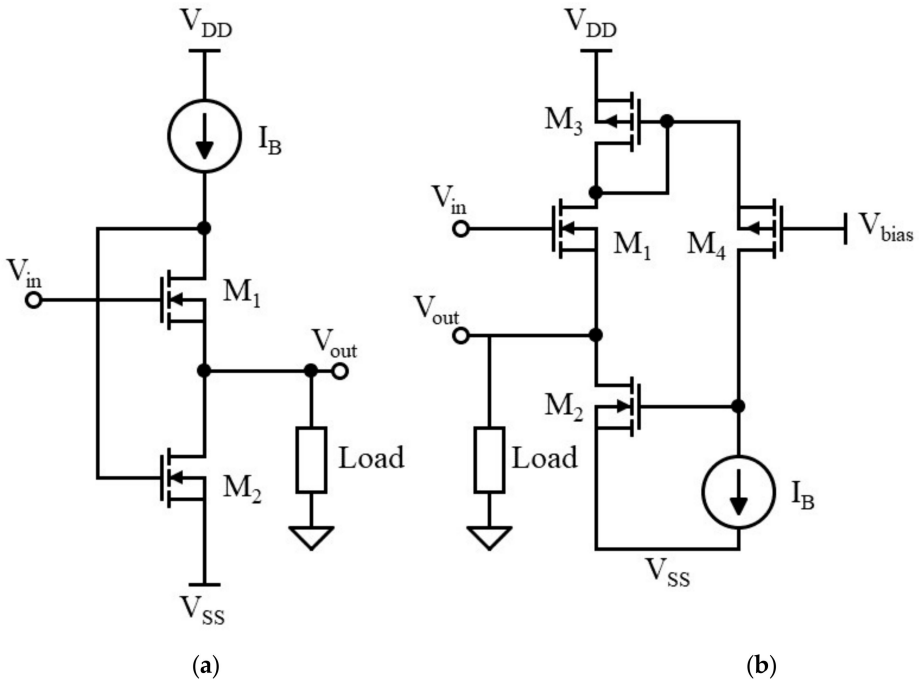


Figure 1. FVF structures: (**a**) standard NMOS FVF, (**b**) class AB FVF.

2.2. The Second-Generation Voltage Conveyor

Recently, current-mode signal processing and, in particular, the basic building block, namely the second-generation current conveyor (CCII), have been used instead of the Op-Amp in many integrated applications [42–44]. With respect to the classical Op-Amp, the CCII device is simpler and superior due to both the low complexity of the transistor level structure and, more importantly, its open-loop configuration. In fact, thanks to the absence of negative feedback, the frequency compensation is not needed, resulting in a further simplified circuit design and also high-frequency operation with the same performance as the Op-Amp. More recently, in 2001, a novel block identified as second-generation voltage conveyor (VCII) [45–48] was introduced, resulting in the dual of CCII. In Figure 2a a diagram of the VCII is provided, showing the three main signal terminals, while in Figure 2b, the internal structure is depicted. In detail, the internal architecture is formed by a current buffer between Y and X nodes and a voltage buffer between X and Z terminals.

Different from the CCII, the Y node of a VCII is a very low impedance current input port, while the X node is a very high impedance output current node. Finally, the Z node is a low impedance voltage output port.

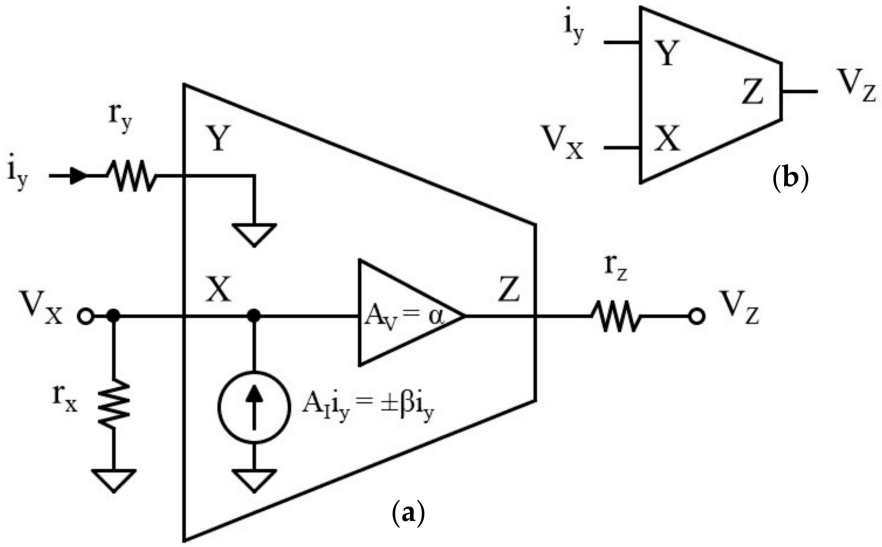


Figure 2. (**a**) Internal block structure of the VCII; (**b**) VCII device symbol.

The constitutional relationships between port voltages and currents can be expressed as follows:

$$\beta = \frac{i_y}{i_x} \approx \pm\frac{\beta_0}{1+\frac{s}{\omega_\beta}}, \alpha = \frac{v_x}{v_z} \approx \frac{\alpha_0}{1+\frac{s}{\omega_\alpha}} \tag{1}$$

where β_0 and α_0 are DC values (ideally equal to unity) of the current gain between Y and X terminals and voltage gain between X and Z terminals, while ω_β and ω_α are the so-called −3 dB frequency of current and voltage transfer characteristic, respectively. Two types of VCII, namely VCII+ and VCII−, are identified by β (also, β must be as close as possible to 1). In the ideal representation, α is also unitary.

In Figure 3 the transistor level implementation of the VCII utilized in this work (VCII+) is reported: the Y, X, and Z terminals are reported, also showing both the voltage and current architecture buffers.

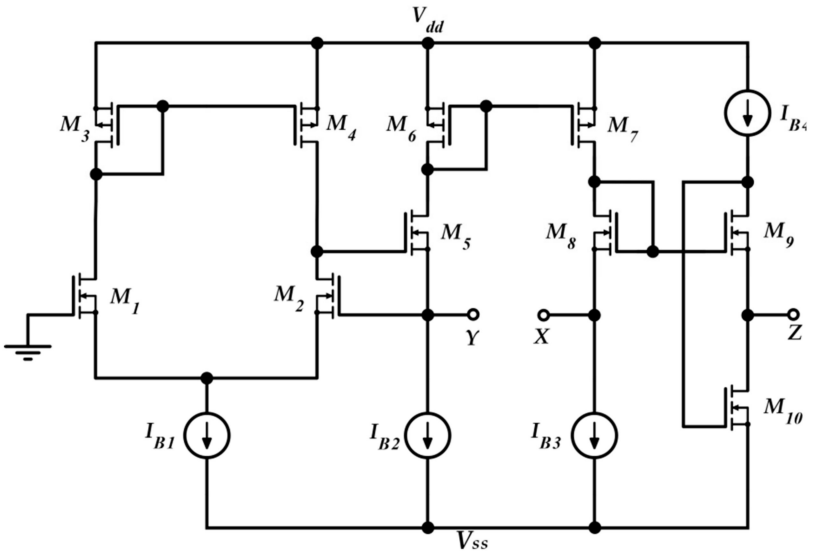


Figure 3. Transistor level implementation of the VCII+ used in this work.

3. The Proposed Combined Architecture

In this section, the design strategy and architecture of the proposed amplifier is presented. The system is composed of two main blocks, which are a Differential Flipped Voltage Follower (DFVF) and a VCII, as reported in Figure 4. The first is identified by transistors M_1, M_2, and M_3 and represents the differential voltage input stage of the circuit. It is a non-linear, Class-AB transconductance amplifier, since the quiescent current is I_{bias}, different from zero, but the maximum output current is larger than the biasing current. Considering the scheme depicted in Figure 4 and neglecting the channel length modulation, it is possible to compute the drain current I_d, M_1 of the transistor M_1 as follows:

$$I_{d,M1} = \frac{1}{2}\mu_P C_{ox,P}\left(\frac{W}{L}\right)_{M1}\left(V_{sg,M1} - V_{th,M1}\right)^2 \quad (2)$$

where μ_P and $C_{ox,P}$ are the charge-carrier effective mobility and the gate oxide capacitance per unit area of the PMOS transistor, respectively.

On the other hand, the voltage at the shared node **A** between all the three transistors is equal to:

$$V_A = V_{DD} - V_{sd,M3} = V_{DD} - \left(V_{s,M3} - V_{d,M3}\right) = V_{DD} - \left[V_{s,M3} - \left(V_{g,M3} + V_{sd,M2}\right)\right] \quad (3)$$

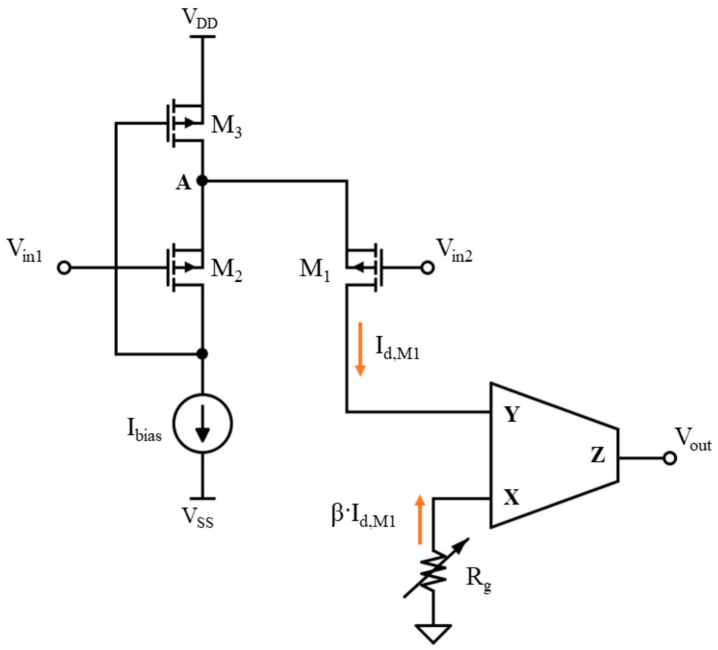


Figure 4. Mixed circuit and block scheme of the proposed DFVF-VCII-based amplifier.

Since the voltage $V_{g,M3}$ at the gate of M_3 is equal to the drain voltage $V_{d,M2}$ of M_2, and the source voltage $V_{s,M3}$ corresponds to the supply voltage V_{DD}, Equation (3) can be expressed as follows:

$$V_A = V_{DD} - (V_{s,M3} - V_{s,M2}) = V_{DD} - \left[V_{s,M3} - \left(V_{in1} + V_{th,M2}\right)\right] = V_{in1} + V_{th,M2} \quad (4)$$

Moreover, the voltage V_A can also be expressed as

$$V_A = V_{in2} + V_{sg,M1} \quad (5)$$

Therefore, by substituting Equation (5) in Equation (4), a new expression of the source-gate voltage of M_1 can be formulated:

$$V_{sg,M1} = V_{in1} + V_{th,M2} - V_{in2} \quad (6)$$

Finally, by recalling Equation (2) and by considering the expression of $V_{sg,M1}$ as shown in Equation (6), the final relation between the input voltages V_{in1} and V_{in2} follows, as well as the output current of the DFVF input stage:

$$I_{d,M1} = \frac{1}{2}\mu_P C_{ox,P}\left(\frac{W}{L}\right)_{M1=M2}(V_{in1} - V_{in2})^2 \tag{7}$$

Equation (7) demonstrates that the output current of the DFVF input stage is quadratically proportional to the difference between V_{in1} and V_{in2}. This quadratic dependence can be linearized, so the output current can be considered to be linearly proportional to the differential input voltage when the latter is very small, as in the case of neural signals. By changing the W/L ratio of the transistor M_1, the transconductance gain of the differential input stage can be modified.

The DFVF is followed by a VCII in transimpedance configuration. Recalling Equation (1), the current $I_{d,M1}$ at the node Y of the voltage conveyor is mirrored at the node X, multiplied by the β coefficient, and is converted to a voltage V_X by means of the resistor R_g, as follows:

$$V_X = -R_g \cdot \beta I_{d,M1} \tag{8}$$

Since the voltage at the X node of the VCII is replicated at the Z node, multiplied by the α factor, the output voltage expression of the proposed neural amplifier can be expressed as:

$$V_Z = V_{out} = -\alpha\beta \cdot R_g \cdot I_{d,M1} = -\frac{1}{2}\alpha\beta R_g \mu_P C_{ox,P}\left(\frac{W}{L}\right)_{M1}(V_{in1} - V_{in2})^2 \tag{9}$$

where the resistor R_g acts as gain tuner of the output voltage.

By observing Equation (8), it can be stated that the proposed scheme acts as a tunable inverting differential voltage amplifier without the use of any feedback network, where the gain can be adjusted by changing the value of the resistor R_g

To achieve full-chip integrability of the proposed scheme, R_g is substituted by a simple voltage-controlled resistor [49], whose schematic level implementation is depicted in Figure 5a.

This structure acts as a variable resistor, controlled by a voltage Vctrl, as described in the following equation:

$$R_g = \frac{L_{M4=M5}}{2\mu_P C_{ox,P} W_{M4=M5}(V_{ctrl} - V_{th})} \tag{10}$$

The actual resistance vs. control voltage relationship referred to transistor sizes reported in Table 1 is shown in Figure 5b.

Therefore, Equation (9) can be rewritten by substituting Equation (10) into the R_g term:

$$V_{out} = -\frac{1}{4}\alpha\beta\left(\frac{L}{W}\right)_{M4}\left(\frac{W}{L}\right)_{M1}\frac{(V_{in1} - V_{in2})^2}{V_{ctrl} - V_{th}} \tag{11}$$

where the voltage gain decreases as the control voltage V_{ctrl} increases. From Equation (11), it can be seen that the terms μ_P and $C_{ox,P}$ disappear from the input–output relation, since both the voltage-controlled resistors and the input DFVF stage are implemented by means of a PMOS transistor. As a consequence, the constitutive relation of the proposed neural amplifier is not dependent on the technology parameters.

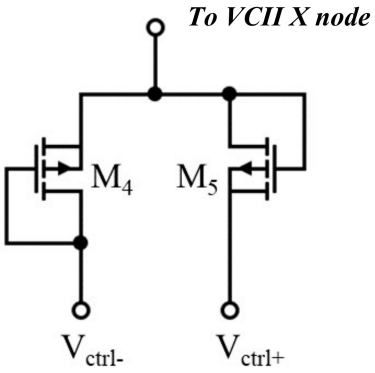
Finally, if the transistors M_4 and M_5 are made with the same geometric dimensions as M_1 and M_2, Equation (11) can be simplified as follows:

$$V_{out} = -\frac{1}{4}\frac{(V_{in1} - V_{in2})^2}{V_{ctrl} - V_{th}}. \tag{12}$$

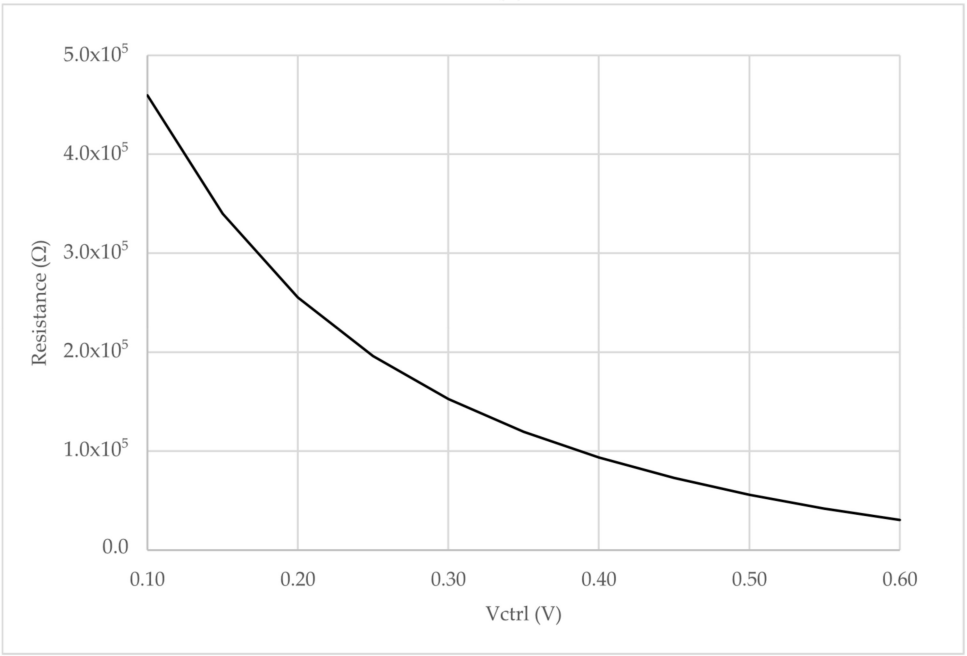
with α and β being coefficients usually equal to unity, for a standard designed VCII.

In Figure 6, the final transistor-level implementation of the proposed neural amplifier is presented. Here, the differential input stage is AC coupled by means of capacitors C_1 and C_2, which can be very small, since the input impedance of the scheme is high. Transistors M_{26} and M_{27} are utilized to bias the DFVF input. The V_B voltage is chosen so to maintain them in sub threshold conditions. The Y branch of the VCII is implemented by means of an AB-Class, super common-gate cell, which helps to lower the impedance at the Y node. The AB-Class biasing is performed by means of transistors M_5-M_6, where the V_A voltage establishes the biasing current of the Y and X branches.

Since the current at X terminal has to flow into the node (it is equal to the Y current), the circuit behaves as an inverting amplifier.



(**a**)



(**b**)

Figure 5. Implemented PMOS voltage-controlled shunt resistor Rg for neural amplifier gain tuning (**a**) circuit; (**b**) resistance vs. control voltage relationship.

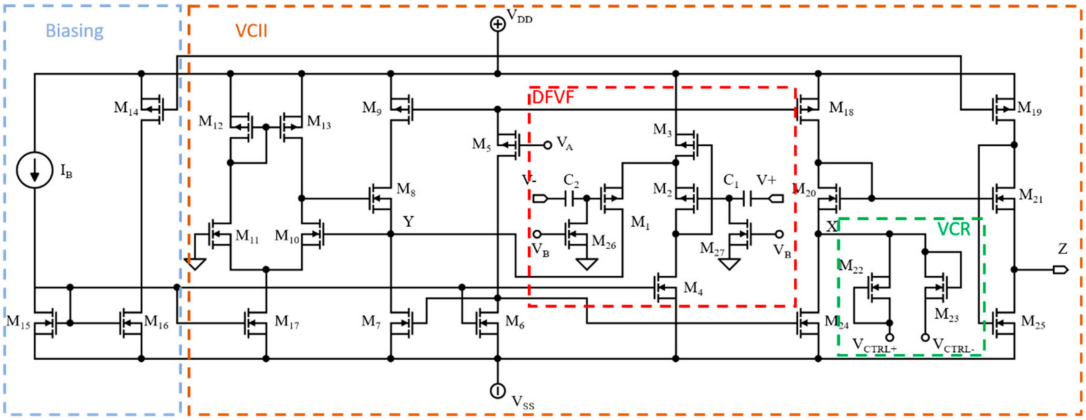


Figure 6. The complete transistor-level architecture of the proposed neural amplifier. The four main blocks have been highlighted: (**1**) Biasing current mirror (**2**) VCII complete block, (**3**) DFVF standalone block, (**4**) Voltage Controlled Resistor (VCR).

Table 1. Transistor aspect ratios and main parameter values.

Transistor	Dimensions (W, L)
$M_{1,2}$	5.55 µm, 0.3 µm
M_3	1.05 µm, 0.3 µm
$M_{4–6–15–16–17}$	1.8 µm, 1.5 µm
$M_{5–9–18}$	11.85 µm, 0.3 µm
M_8	60 µm, 0.15 µm
$M_{10–11}$	55.95 µm, 0.15 µm
$M_{12–13}$	1.95 µm, 0.15 µm
M_{14}	7.95 µm, 1.5 µm
$M_{7–24}$	3.6 µm, 1.5 µm
M_{19}	16.05 µm, 1.5 µm
$M_{20–21}$	70.05 µm, 0.3 µm
$M_{22–23}$	55.05 µm, 18 µm
M_{25}	1.8 µm, 45.9 µm
Parameter	**Value**
I_B	2 µA
V_A	−290 mV
C_1, C_2	1 pF
V_B	50 mV

4. Simulation Results and Comparisons

Simulations were performed using the LFoundry 150 nm low V_{th} CMOS process. Supply voltage was set to ±0.6 V. Transistor dimensions, as well as main biasing parameters, are reported in Table 1. The overall power consumption was evaluated as 20 µW. To minimize the dependence of the output voltage on the process parameters, the active resistor was implemented through a PMOS pair, while their aspect ratio was tuned in order to achieve the largest gain span possible with the control voltage ranging from 0.1 V to 0.6 V. In this regard, the minimum value is given by the technology threshold voltage, while the upper one is fixed by the supply voltage.

Figure 7 shows the drain current of M_1 when a differential signal is applied to the DFVF inputs.

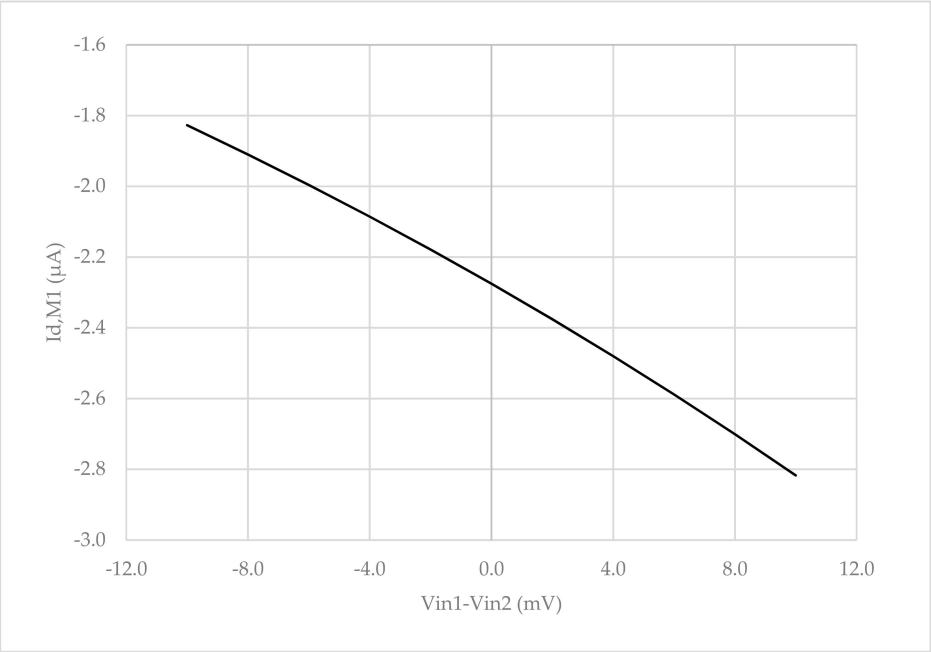


Figure 7. DFVF differential input voltage vs. output current relationship.

As can be seen, the current follows the differential input variation, with a 2.3 µA DC value fixed by the biasing mirror M_{15}–M_4. As stated before, although the relationship between the differential input voltage and the M_1 drain current is non-linear (Equation (7)), it can be linearized in applications where input amplitudes are sufficiently low. AC performances of the amplifier at various gain levels are shown in Figure 8. For this simulation, a 1 pF load capacitor was connected at the output of the amplifier.

As long as the control voltage remains greater than the threshold voltage of the PMOS equivalent resistor pair, it is possible to set the gain of the amplifier from 32 dB to 0 dB. The value of C_1 and C_2 was set to 1 pF resulting in a lower cutoff frequency of approximately 100 mHz.

The input–output relationship of the amplifier was derived by applying a differential voltage ranging from −5 mV to 5 mV to the input DFVF and monitoring the Z terminal of the VCII. Figure 9 acknowledges a good linearity when very small input signal applications are considered, even under conditions of high gain.

Referring to Figure 6, the X and Y branches and the DFVF stage were biased with the same current so as to make sure that, for common-mode inputs, the current flowing into the gain resistor is equal to zero, and so is the voltage at the output. Input-referred noise performances are shown in Figure 10. The total noise over a bandwidth that goes from 100 mHz to 10 kHz is equal to 5.4 μV_{RMS}. To achieve a low noise figure, due to the mixed current and voltage mode behavior of the proposed amplifier, both the current and voltage noise contribution have to be addressed. In particular, to reduce current noise at each terminal, it is possible to reduce the W/L ratio of M_7, M_{24} and M_{25}. To reduce the noise voltage of the circuit, it is instead possible to design M_{20} and M_{21} with a high W/L ratio.

Noise efficiency factor (NEF) was also evaluated over the same bandwidth at room temperature on the basis of the following equations:

$$NEF = v_{ni,RMS}\sqrt{\frac{2I_{TOT}}{V_T 4K_B T\pi BW}} \tag{13}$$

where I_{TOT} is the total current consumption of the amplifier, $v_{ni,rms}$ is the total RMS voltage noise referred to the input, V_T is the thermal voltage expressed in [K], K_B is the Boltzmann's constant and BW the total bandwidth with reference to the noise. The resulting NEF is equal to 8.3.

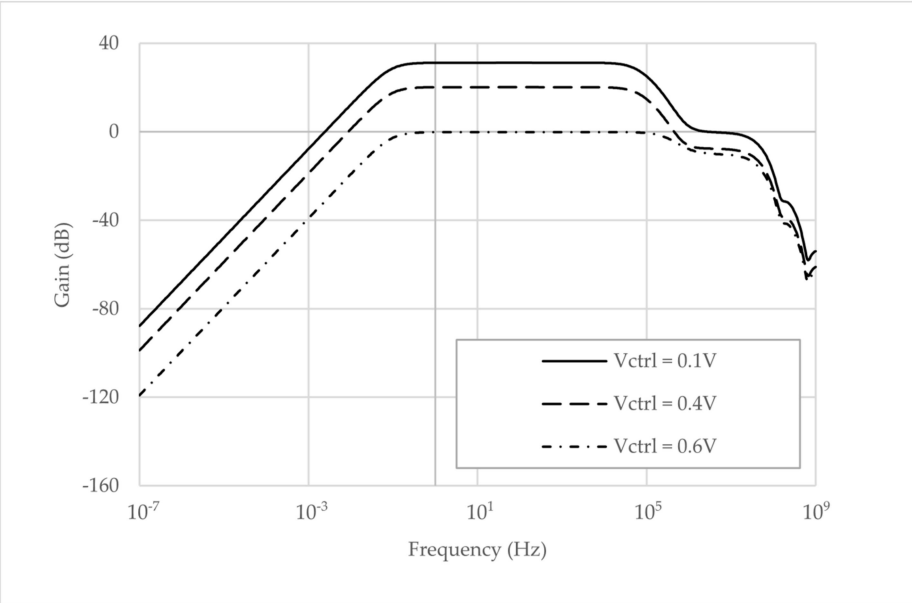


Figure 8. AC performances of the amplifier at various gain levels.

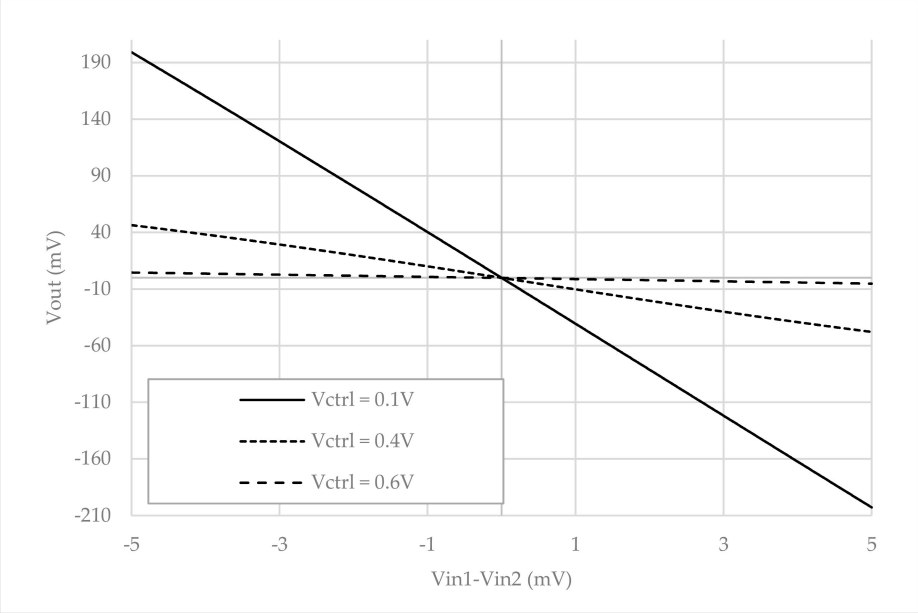


Figure 9. DC performances of the amplifier at various gain levels.

Since the actual sensing elements can be placed far from the processing circuitry, an investigation on the influence of the line impedance [50] over the output voltage was performed. Figure 11 shows the input impedance of the amplifier. Variations induced in the output voltage when a series resistor is introduced between the signal generator and the amplifier itself are overall negligible, due to the extremely high input impedance of the proposed topology (3.2 GΩ @ 10 kHz).

To evaluate the spectral distortion introduced by the proposed circuit, a differential sinusoidal input with a 100 μV peak amplitude and a frequency of 10 kHz was applied to the input terminals. The total harmonic distortion of the output voltage was equal to 1.1% (−39.8 dB) when considering 10 harmonics and with the amplifier gain set to its maximum value (32 dB).

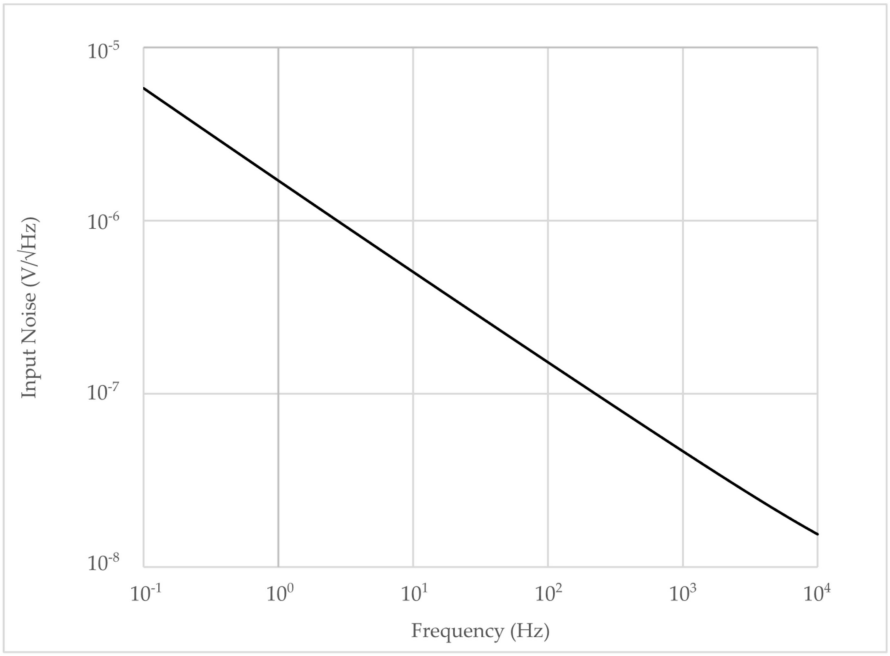


Figure 10. Input-referred noise performance of the amplifier.

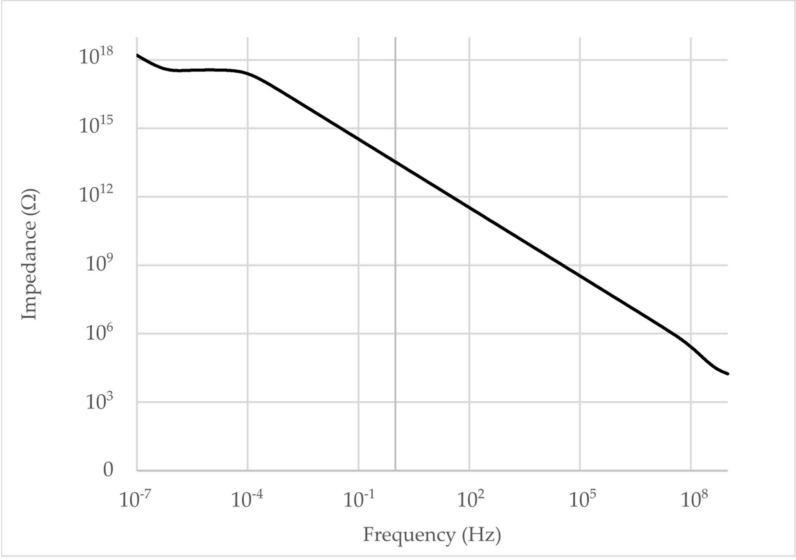


Figure 11. Input impedance of the proposed amplifier.

To conclude the analysis, the robustness of the amplifier performance with respect to randomly imposed PVT conditions was investigated. For this simulation, a Monte Carlo analysis was conducted over 100 iterations of an AC simulation, while monitoring the output voltage, and the two cutoff frequencies. The gain of the amplifier was set to 20 dB (V_{ctrl} = 0.4 V). Figure 12a–c shows the probability distributions for the gain, the lower cutoff frequency and the upper cutoff frequency, respectively.

A comparison between the main features of the proposed architecture and the most recent available literature [51–53] is given in Table 2, showing the proposed topology points of strength.

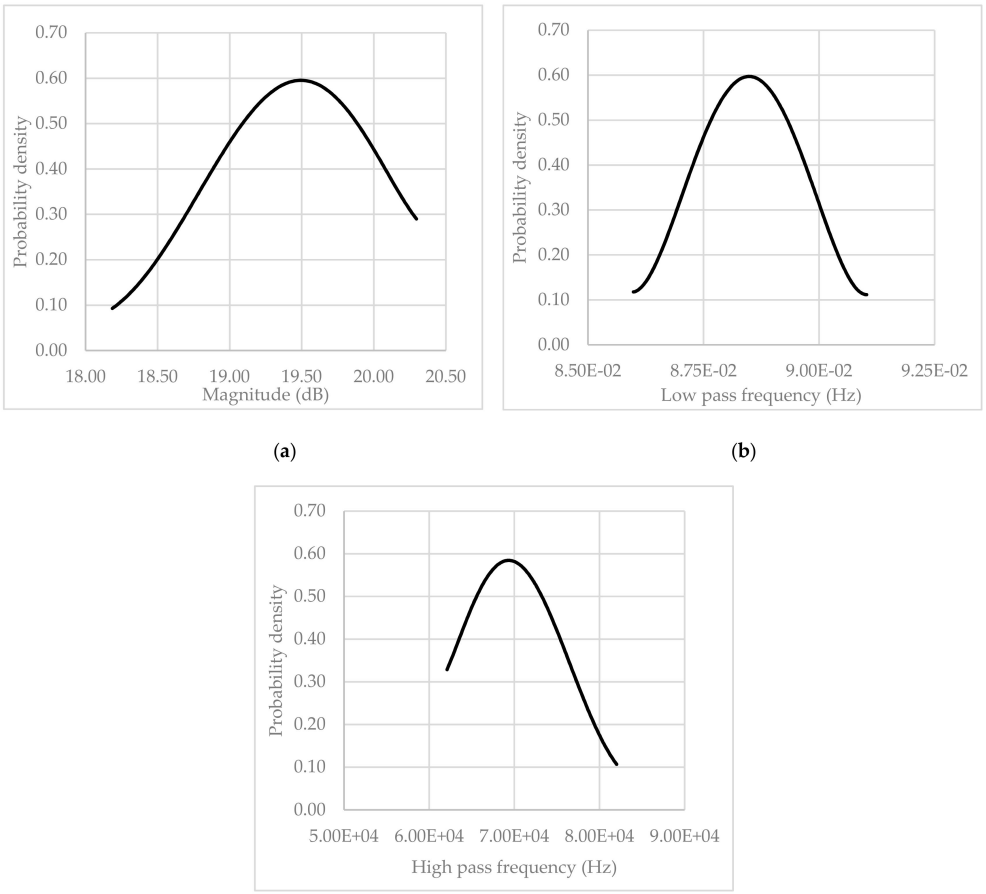


Figure 12. Statistical distribution of (**a**) the output voltage, (**b**) the lower cutoff frequency, (**c**) the higher cutoff frequency, evaluated under random PVT conditions.

Table 2. Comparison table.

Parameter	This work	2016 [50]	2018 [51]	2019 [53]	2019 [54]	2018 [55]
CMOS Technology	LFoundry 150 nm	180 nm	180 nm	180 nm	180 nm	500 nm
Supply voltage	±0.6 V	1.2 V	1 V	1.2 V	1.2 V	3.3 V
Static power consumption	20 µW	0.9 µW	0.25 µW	8.1 µW	2.48/5.46 µW (AP/LFP)	28.05 µW
Amplifier Gain (dB)	0~33 (continuous Tuning)	30/50	25.6	26/32/35.6 (Selectable)	40/20 (AP/LFP)	49.5 (Untunable)
f_{HPF} (Hz)	10^{-5}	6.3	4	0.025/0.25/0.5/1.5/32/65/125/260		13
f_{LPF} (kHz)	174~3980	0.175	10	1/11.4/125	100/1000 (LFP/AP)	9.8
Zin	3.2 GΩ *(@10 kHz)*	20 MΩ	200 MΩ @100 Hz	-	-	-
Zout	1.2 kΩ *(@10 kHz)*	-	-	-	-	-
THD @frequency reference	1.02% (−39.8 dB) @Vin = 2mVpp, Vctrl = 0 V, 10 kHz)	0.4%@1mVpp 10 Hz	-	-	-	1% @ 0.7 mVpp, 10 kHz
Noise Voltage (input referred)	5.4 μV_{RMS} (0.1 Hz ~ 10 kHz)	2.6 µVRMS (0.5 Hz ~ 400 Hz)	3.32 μV_{RMS} (250 Hz ~ 10 kHz)	6.75 μV_{RMS} (0.5~11.4 k, 40 dB)	AP: 3.44 (0.25 k~10 k) LFP: 6.88 (0.025~600)	1.88 μV_{RMS} (0.03 Hz~11 kHz)
NEF	8.3	6.6	1.07	7.29	NA	2.3

5. Conclusions

We have presented a mixed DFVF/VCII circuital topology for implementing optimized high-efficiency integrated amplifiers to be used in several applications such as biomedical systems. The interfacing amplifier was designed with a 150 nm CMOS technology showing, at simulation level, very low input-referred noise and high input impedance, together with very low sensitivity towards the amplifier input line impedance. Moreover, the proposed architecture showed no need for any capacitive feedback for the input bootstrap operation, in any case offering very low high-pass cutoff frequency.

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