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Design of a Voltage to Time Converter with High Conversion Gain for Reliable and Secure Autonomous Vehicles

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Abstract: Automation of vehicles requires a secure, reliable, and real-time on-chip system. These systems also require very high-speed and compact on-chip analog to digital converters (ADC). The conventional ADC cannot fulfill this requirement. In this paper, we proposed a Darlington pair- and source biasing-based high speed, secure, and reliable voltage to time converter (VTC). It is a compact, high-speed design and gives high conversion gain. The source biasing also helps to increase the input voltage range. The conversion gain of the proposed circuit is 101.43ns/v, which is 52 times greater than the gain achieved by state-of-the-art design. It also shows less effect of process variation and bias temperature instability.

Keywords: automation of vehicles; internet of things; voltage to time converter; speed; reliability NBTI; PBTI; ADC; life-time

1. Introduction

The secure and reliable autonomous vehicle is a new research area for the future transportation system. The rapid automation design comes from digital electronics [1]. The block diagram of the autonomous vehicle is shown in Figure 1. It is consists of many input sensors and output control signals. This type of system requires object detection and a decision-based controller. These controllers process huge data using the parallel processors, and the CNN-based accelerator can solve it. These do the dot product using an array of restive or other memories. Hence, it also uses a number of high-speed analog to digital converters because the digital design has been the main driving force for the emerging nanoscale CMOS technology-based VLSI design. CMOS process technology helps in improving the speed and the device fabrication density. The on-chip analog to digital converter (ADC) is needed for digital circuit design. Device dimensions decrease with each new technology node to increase the performance and to reduce the area overhead. However, scaled device dimensions cause the introduction of leakage current sources such as subthreshold and gate leakage currents. These leakage current sources increase the power dissipation [2,3]. Furthermore, the scaled device dimensions cause an increase in the gate electric field intensity, which adds more electric-field stress. The conversion gain and reliability of ADC degrade under electrical field stress at elevated temperatures [4]. Hence, the primary goal of this work is to develop a compact, reliable, low power and high conversion gain-based voltage to time converter (VTC) for an ADC.

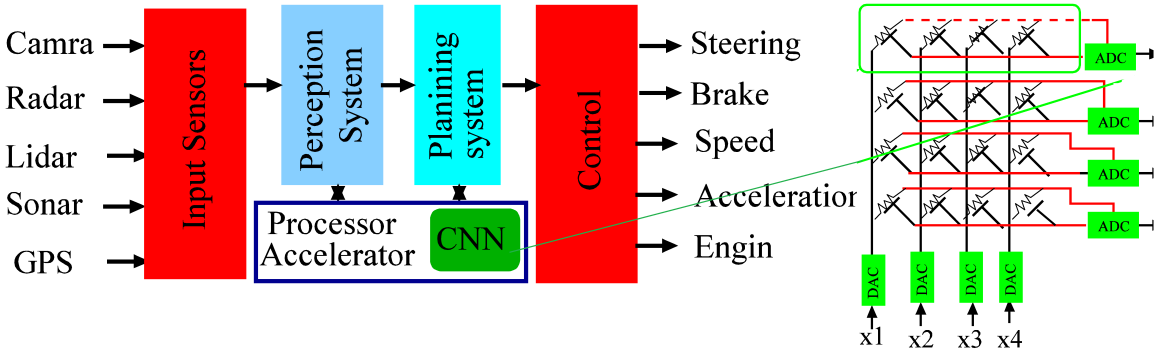

Figure 1. Vehicle automation system and use of convolution network-based accelerator using analog to digital converter (ADC).

The conventional flash type ADC is mostly used for high-speed design, but this ADC also increases the area penalty [5]. Moden State-of-the-art design such as Opamp-free noise shaping successive-approximation register (SAR) ADCs are small in size but they are very slow [6]. CNN requires fast and compact ADC to design real-time systems. High-speed ADCs are mostly designed using the differential amplifier. Differential amplifier-based ADCs are sensitive to the process variations; hence, these ADC are unstable. The differential amplifier is an analog circuit which means it requires symmetric transistor. We also know a tiny noise voltage can degrade the analog circuits. Hence, their fabrication is difficult with the digital ICs such as with the SRAM and microprocessors, etc. [7]. Another design issue in these ADCs is their reliability, which is degraded by negative and positive bias temperature instability (NBTI and PBTI) which are commonly found in nanoscale technology. BTI (NBTI and PBTI) is caused by the presence of dangling hydrogen bonds at the dielectric and semiconductor interface in semiconductor devices such as MOSFET and FinFET, etc. [8,9]. The weak dangling bonds are broken under high electric stress and at increasing temperature due to their low binding energy and the trapping of hydrogen atoms into the gate oxide [8]. The number of PMOS transistors is more in conventional ADC design, which further reduces the reliability [4].

VTC is used to converter voltage to time. Further, VTC is used to design the ADC. The resolution of VTC-based ADC depends on the conversion gain hence it is an important parameter for VTC. Several types of time-dependent ADCs have been reportedly used for high-speed applications, but these have fewer conversion gains [10–12]. The design principle of these ADCs is based on generating delay by charging and discharging of capacitors. The most challenging issues in these designs are a small range of delays and poor sensitivity towards the change in the input voltage. In most designs, a reference voltage is used for comparison with the actual capacitor voltage [10,13]. The reference voltage generation on-chip is also difficult. It requires efficient and stable on-chip hardware. Recently, the bootstrapping principle has been utilized for charging and discharging of the capacitors and proposed a VTC-based ADC [12]. But fabricating a capacitor on-chip requires a large area. In addition, bootstrapping also produces instability in VTC design due to the bootstrap capacitor. Therefore, it cannot be used in ADC [10,12]. Another VTC has been designed based on the basic principle of the currently starved inverter [11]. This design produces a much shorter delay for VTC, and its resolution is not sufficient for the ADCs. Hence, we propose a Darlington pair-based high conversion gain VTC circuit for ADCs. It uses less number of PMOS transistors, which results in improved circuit reliability.

The rest of the paper is organized in the following manner: Section 2 provides a full description of the proposed VTC. Simulation results and analysis are included in Section 3. Section 4 concludes the paper.

2. Proposed VTC

The block diagram of the proposed VTC shown in Figure 2a consists of a Voltage to delay, a delay smoothing circuit and an asynchronous digital counter. An inverter designs the delay smoothing circuit. The asynchronous counter is showing one applicability of the proposed circuit. The VTC generates the delay which enables the counter for a period which is counted by the counter to produce the final digital output. In this work, we propose a delay generator and controlling circuits. The circuit diagram of the proposed VTC is shown in Figure 3. The objective of the proposed VTC is to increase the rise or fall time delay of the delay generator circuit and increase the conductivity of the controlling circuit. Such objectives are achieved through increasing the threshold voltage of the pull-down circuitry of an inverter (delay generator circuit). The high conversion gain is achieved through increasing the conductivity of the controlling circuit which also helps to improve the delay sensitivity window. The controlling circuit has a smart function of converting the voltage to time as well as increasing the sensitivity toward the change in input voltage. It gives a large change in output delay due to a small change in the input voltage. The source biasing voltage of the proposed VTC V_{bb} helps to increase the conductivity of the controlling circuit and it also helps to increase the linear region.

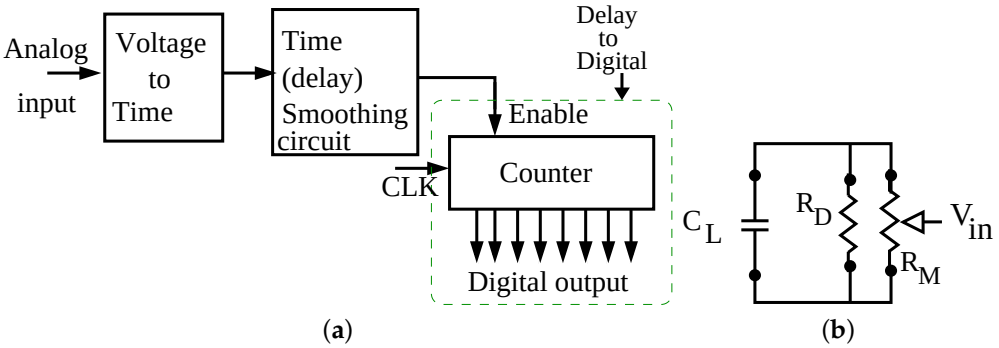

Figure 2. (**a**) Proposed voltage to time converter (VTC)-based ADC (**b**) Fundamental Model.

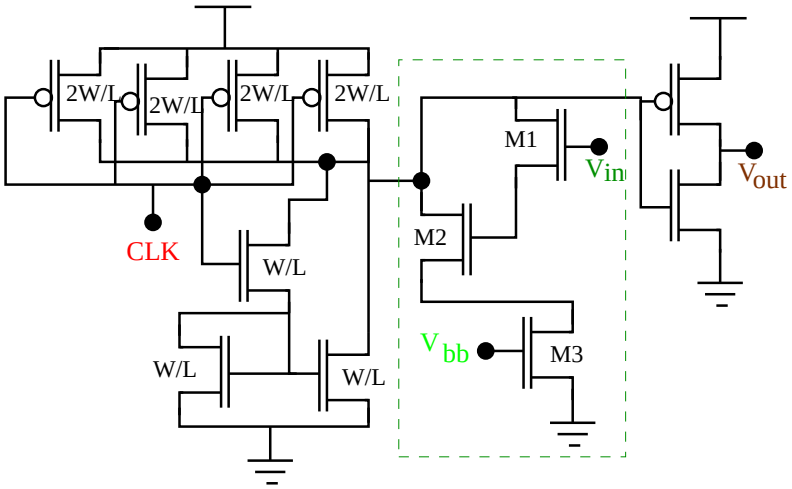

Figure 3. Circuit diagram of the proposed VTC.

Darlington pair-based pull-down network named as super MOS (S-MOS) has been used for the inverter in order to increase the conductance and the threshold voltage of the MOSFET. In S-MOS, a combination of two MOS works as a single MOSFET with two times threshold voltage. This method can be used to generate N times of threshold voltage for the different applications. Now we will do the different circuit electric analysis of the proposed circuit. In order to calculate the modified threshold voltage (V_{TH}), the output is assumed to be high since this transition is important, and input

is increased from 0 to V_{DD}. At this time, we assume all the transistors are in saturation mode for the simplified calculation.

Hence,

$$\frac{K_P}{2}(V_M - V_{DD} - V_{TP})^2 = \frac{K_N 1}{2}(V_M - V_{TN1} - V_{TN1})^2 \tag{1}$$

Hence, the threshold voltage (V_M) of the new circuit is given by:

$$V_M = \frac{2V_{TN} + (V_{DD} + V_{TP})\sqrt{K_P/K_N}}{1 + \sqrt{K_P/K_N}} \tag{2}$$

To calculate the change in output delay as a function of input voltage, the first parameter to be determined the fall time because we are manipulating this time for the VTC design. Calculating this parameter requires the development of an equivalent discharging model which is shown in Figure 2b. R_D and R_M are parallel connected and denote the driver circuit resistance and the controlling circuit resistance, respectively.

$$\tau_{HL} = 0.69(R_D + R_M)C_L \times K_f \tag{3}$$

where C_L is the load capacitance and K_f is the graph fitting parameter which is used to reduce the gap between level 1 and level 54 MOSFET models.

$$R_D = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_D(1 + \lambda V_{DS})}dV \tag{4}$$

$$R_D = \frac{3(1 - \frac{7}{9}\lambda V_{DD})}{4K\frac{W}{L}\left[(V_{DD} - 2V_T)V_{DD} - \frac{VDD^2}{2}\right]} \tag{5}$$

$$R_M = \frac{3(1 - \frac{7}{9}\lambda (V_{DD} - V_{bb}))}{4K\frac{W}{L}\left[(V_{in} - V_{bb} - 2V_T)(V_{DD} - V_{bb}) - \frac{(V_{DD} - V_{bb})^2}{2}\right]} \tag{6}$$

Now, total load capacitance can be modelled as follows:

$$\begin{aligned} C_L =& C_{gN} + C_{gP} + (C_{gsN} + C_{gdP} + W_N L_N C_{ox}) \\ &+ (C_{gsP} + C_{gdP} + W_P L_P C_{ox}) \end{aligned} \tag{7}$$

where C_{gN} and C_{gP} are the gate to substrate capacitances, C_{gsN} and C_{gsP} are the gate to source capacitances, C_{ox} is the oxide capacitance, C_{gdP} and C_{gdP} are the gate to drain capacitances for NMOS and PMOS transistors respectively. This circuit is followed by a conventional inverter that produces rail to rail delayed (amplified delay) output in response to a change in the input voltage. The sizing of this transistor has been selected in order to produce symmetric outputs for high-to-low and low-to-high transitions. We have designed the proposed design using 45 nm freePDK technology. The layout of the VTC circuit is shown in Figure 4 . The area of VTC is 350 nm $\times$ 270 nm is smaller than the state-of-the-art design [12]. The detailed comparative result analysis of the proposed circuit is discussed in the next section.

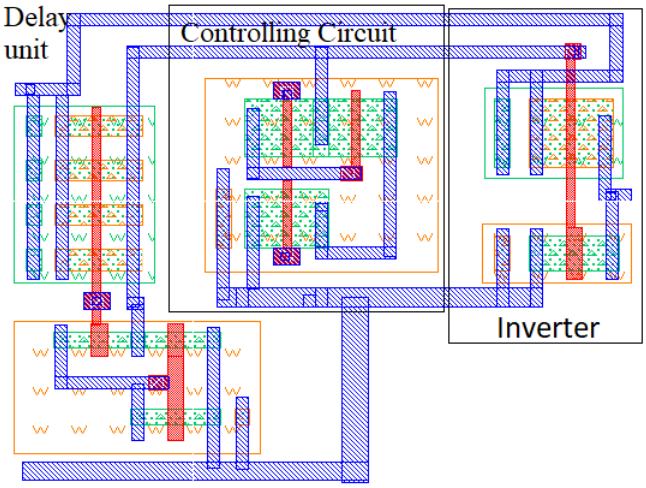

Figure 4. Layout diagram of the proposed VTC.

3. Results and Analysis

The proposed design has been verified using the mathematical equivalent modeling and simulation results. We have used the 500 mV supply voltage for simulation. The design was made for near sub-threshold operation in order to reduce power consumption. Figure 5a compares the V-T conversion characteristics with the model. The conversion-gain is the ratio of change in output delay with the change in input voltage. The conversion-gain of the proposed circuit is 101.43 ns/V, which is 52× greater than the conversion gains achieved by state-of-the-art designs (1.95 ns/V) [12,14]. The detailed comparison with the experimental result is shown in Table 1. The most recent VTC [12] uses the bootstrap switches to control the charging and discharging of the capacitors. The on-chip active capacitor takes more charging and discharging time than the MOSFET capacitors. Hence, most recent designs cannot support the high-frequency input. Still, it has some useful features. The proposed design is not using any on-chip capacitor, thus it cannot limit the input frequency. The exiting design also used 25 transistors to control the capacitors, whereas we are using only 12 transistors. Another existing design [14] can support 2.5 GHz input signal frequency, but the conversion gain is not good enough then the proposed VTC.

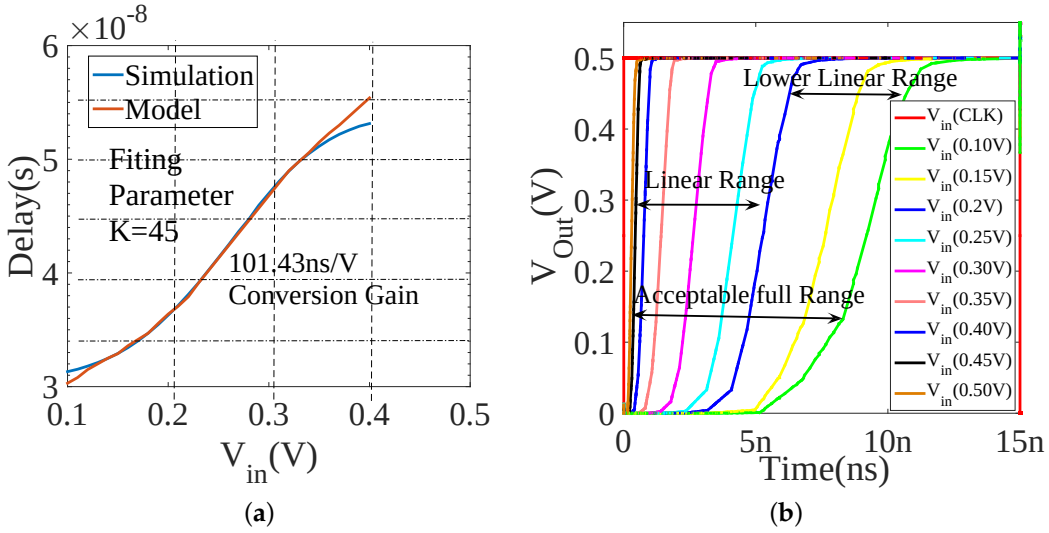

Figure 5. (**a**) V-T conversion characteristics (**b**) Output vs. time curve.

Table 1. Comparison of conversion Gain with experimental works.

S. No.	V_{DD} (V)	Conversion Gain	Remark
1	1.2	1.95 ns/V	[12]
2	1	25 ps/100 mV	[14]
3	0.5 V	101.43 ns/V	This Work

Figure 5b shows the T-V characteristic for a range of input voltages which can be used to identify the best possible linear range for the given input voltage. Change in the operating temperature is also important for the CMOS circuits. The proposed VTC is tested for a wide range of temperatures, which is −40 °C to 125 °C. The change in the V-T characteristic for different temperatures is shown in Figure 6. Results show moderate variation in the characteristic due to temperature variation. Controlling circuit optimization is shown in Figure 7a. The controlling circuit can be further optimized using the biasing voltage (V_{bb}) as shown in Figure 7b. To achieve a better linear range, the sizing of the super MOS has been determined to be 120 nm transistor width and 0.35 V source biasing voltage.

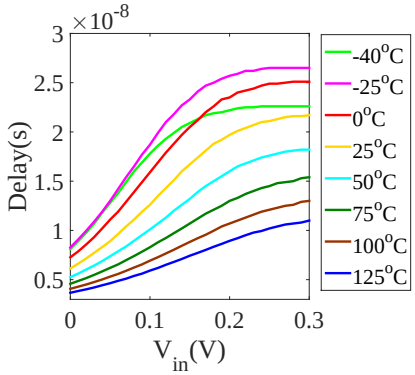

Figure 6. V-T characteristics of VTC for different temperature.

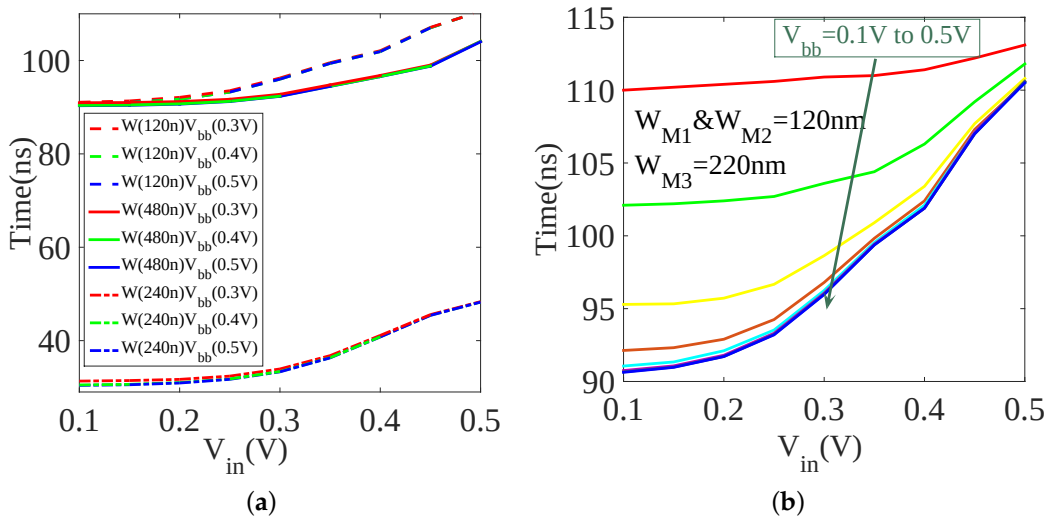

Figure 7. Optimization of (**a**) the transistor widths of controlling circuit and (**b**) biasing voltage (V_{bb}).

The source biasing voltage also helps to make design stable due to the parametric variation. We have chosen a particular biasing voltage through the Monte Carlo simulation. We have used 5000 Monte Carlo samples. Figure 8a shows that the proposed circuit can tolerate process variation effects at 0.35 V biasing voltage. This is reflected by the small deviation (σ) from the mean value at 0.35 V

biasing voltage. Mosra model is used for the time-dependent reliability analysis [15]. The change in threshold voltage of the MOSFET due to DC stress is shown in the Equitation (8) [16].

$$\alpha\Delta|V_{th_{Dc}}| = K_{DC}t^n \tag{8}$$

where α is the perfection parameter, n is the time constant, t is the aging time and K_{DC} is fabrication-technology dependent constant. The change in threshold voltage due to AC stress is given by [16]:

$$\Delta|V_{th_{AC}} \approx \alpha\Delta|V_{th_{AC}}| = \alpha \times K_{AC} \times t^{0.25} \tag{9}$$

where α is the perfection parameter which depends on the operating AC frequency. It has already been testified that DC stress more impact the lifetime than AC stress. The NMOS and PMOS devices experience DC stress when they are in the ON state and perform recovery when they are in the OFF. Figure 8b shows the dependence of reliability overtime where the V-T results are compared for 3-year and 10-year stress. It is shown that 3.95% shift has been achieved for 10-year stress which is very small than the existing design [12]. This is due to the smaller number of PMOS transistors used in the proposed circuit compared to existing designs.

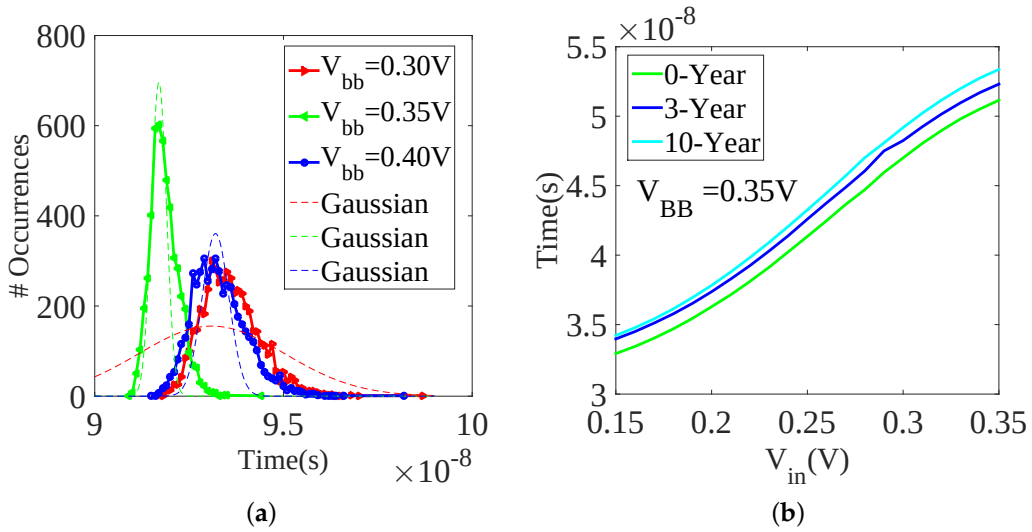

Figure 8. (**a**) Process Variation and (**b**) Reliability (bias temperature instability [BTI]) analysis.

4. Conclusions

This paper presents an on-chip design solution for reliable and secure automotive vehicles. The proposed voltage to time converter (VTC) circuit is a high speed and reliable component for the modern analog to digital converters (ADC). The proposed VTC is shown to have very high speed and large conversion gain. The proposed VTC circuit was designed based on the principle of voltage to delay conversion with a speed that matches the real-time speed. The area of the proposed VTC circuit is very small, and its conversion gain is 52 times greater than the gains achieved by state-of-the-art designs. The proposed VTC circuit has proved its effectiveness to show stable response under process variation. It is also reliable for ten years of stress due to bias temperature instability (BTI) and Hot-carrier Injection (HCI). The proposed VTC can also be used with the sensor nodes and on-chip data converters.

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