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Design and Development of BTI Model and 3D InGaAs HEMT-Based SRAM for Reliable and Secure Internet of Things Application

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Abstract: It is broadly accepted that the silicon-based CMOS has touched its scaling limits and alternative substrate materials are needed for future technology nodes. An Indium-Gallium-Arsenide (*InGaAs*)-based device is well situated for further technology nodes. This material also has better mobility of the electrons and holes for the high performance and real-time system design. The improved mobility helps to increase the operating frequency of the device which is useful for Internet of Things (IoT) applications. However, *InGaAs*-based High Electron Mobility Transistors (HEMT) limits the reliability of the device due to the presence of dangling bonds at the channel–gate insulator interfaces. Weak dangling-bonds get broken under electric stress, and positive hydrogen atoms are trapped into the oxide. This charge trapping depends on the material parameters and device geometry. In this paper, the existing Bias-Temperature-Instability (BTI) model is modified based on the material parameters and device geometry. Charge trapping and annealing constants are the most critical BTI model parameters that are modeled and evaluated based on different HEMT material parameters. The proposed model was compared to experimental and TCAD simulation results. The proposed model has been used for lifetime prediction of the InGaAs HEMT-based Static Random-Access Memory (SRAM) cell because it is used to store and process the information in the IoT applications.

Keywords: Internet of Things (IoT); autonomous vehicle; HEMT; FinFET; BTI; NBTI; PBTI; charge-trapping; reliability

1. Introduction

Wireless sensor networks (WSNs) have been extensively used as devices for information collection and decision making. These capabilities have expanded the scope of applications of WSNs in many fields including Internet of Things (IoT), healthcare, search and rescue where sensor nodes are deployed at remote locations and under extreme conditions [1]. Power-consumption is one of the important challenges that restrict the efficiency of WSN since sensor nodes are battery operated. Hence, life time prediction of the VLSI chips used for WSN circuits has become a necessity. Speed is another design requirement for WSN circuits which are required to operate at high frequencies. Since MOSFET no longer supports high-frequency operation, High Electron Mobility Transistors (HEMT) provide an alternative solution to achieve high-performance circuit design for WSNs [2]. HEMT has been used to design satellite receivers and sensor nodes [3,4]. Some compound semiconductor materials are used to increase the operating frequency of HEMT such as Gallium-Nitride (*GaN*) and Indium-Gallium-Arsenide (*InGaAs*). In *InGaAs*-based HEMT, the indium material provides

extra strain to increase the mobility of electrons and holes. These semiconductor devices use high-k dielectric materials in order to establish strong insulation of the gate terminal. This helps to reduce the gate leakage current for the low power circuit design. Unlike the conventional bulk-based MOSFET, the high-k dielectric materials in HEMT establish a weak interafce with the bulk material. Therefore, more dangling bonds are generated in HEMT than MOSFET in order to strengthen the contact at the bulk dielectric interface. (SiO_2/Si) [5].

When HEMT devices are operated under electrical stress, the dangling-bonds get broken, and positive hydrogen atoms get trapped inside the gate-insulator, which increases the threshold voltage of the HEMT. Consequently, the HEMT threshold voltage increases which causes a decrease in the operating frequency. Such effects are further escalated at higher temperatures due to the Bias-Temperature-Instability (BTI) which is one of the main reliability degradation sources in HEMT. Other reliability degradation sources include Time-Dependent Dielectric Breakdown (TDDB) and Hot Carrier Injection (HCI) [6]. Therefore, an efficient HEMT-based circuit design should carefully consider the effects of those sources. Due to the complexity of developing a physical VLSI chip, CAD tools are used to model and simulate the behavior of VLSI circuits. Models should incorporate all the reliability degradation sources in order to obtain an accurate simulation of the VLSI circuit under their effects. The Reaction–Diffusion (RD) model [7] can be used to model the increase in the threshold voltage of the HEMT. The RD model is based on using electrochemical reactions and activation energies to represent the interface state [7]. Reliability models should also account for the various device parameters and geometrical properties and therefore they should be modified accordingly based on the device under test.

The primary components of an IoT system are a data converter, a transmitter, and a receiver [1]. These components can be designed using logic circuits and storing elements such as Static Random-Access Memory (SRAM) [8]. Hence, the proposed reliability model for HEMT can be tested on SRAM. SRAM is considered to be the fundamental storing element occupying more than 80% of the on-chip area of the processor. Since HEMT is used for high-frequency SRAM design, the prediction of its lifetime becomes necessary [9]. In this paper, an $InGaAs$-based SRAM is designed and analyzed to evaluate its stability under BTI stress. Based on this analysis, a BTI model for SRAM lifetime prediction has been proposed, and further, it is used for an SRAM circuit simulation using SystemVerilog-based modeling and the HSPICE EDA tool. The highlights of the proposed works are as follows:

1. Design and simulation of the $InGaAs$-based HEMT;
2. Calibration of simulation models and HEMT with experimental data;
3. Proposed a PBTI/NBTI model for HEMT;
4. Proposed model is modified according to the material parameters;
5. Use of proposed model for 6T SRAM cell design.

The rest of the paper is organized as follows: In Section 2, the state-of-the-art BTI models are discussed. In Section 3, the proposed $InGaAs$-based HEMT design is discussed. In Section 4, simulation setup, model calibration with experimental results, and design are proposed. In Section 5, the 6T SRAM cell is briefly described and simulation results are discussed. In Section 6, a spice equivalent BTI model for the $InGaAs$-based HEMT is discussed. In Section 7, the simulation results of the proposed model are discussed. Section 8 concludes the work.

2. State-Of-The-Art BTI Models

It was already mentioned in a previous study, that the trapping of the charge carrier in the gate insulator due to the NBTI/PBTI can be defined by the RD-model [7]. Due to the unclear nature of NBTI/PBTI, more realistic RD-models that better incorporate the effects of those sources have been proposed. Kufluoglu et al. [10] has proposed a model where the transistor structure and scaling-based compact NBTI model were included. It shows similar characteristics with the numerical simulation results despite the superiority of this model to all other kinds of transistor structures, the model parameters were not experimentally determined. Furthermore, the electron/hole

generation and annealing parameters were used but the model did not include the device structure and experimental data. Another RD-based model has been proposed by Islam et al. [11,12], which showed the passivation/depassivation effects of the Si-H bond by using the initial charge density, electron/hole generation constant, and annealing constant. This model, however, did not show the geometrical effect on NBTI/PBTI. For circuit simulation purposes, this model was modified and applied for 65 nm CMOS technology [13]. When BTI is induced, the trap charge density was found to be dependent on the diffusion constant. Therefore, the RD model is further modified to include the diffusion length. This model used the default values for the hole/electron generation and annealing constant [14]. The same model was further modified for silicon body tied FinFET [15].

Some statistical reliability models were proposed for FinFET and SRAM cells and used to investigate the NBTI effects [16]. An NBTI framework for 20 nm node devices was presented by Mishra et al. [17]. The stress generated by BTI is found to be more significant than PBTI stress. NBTI reduces the inversion charges and degrades the electron and hole mobility. It is due to the Coulomb scattering and depends on the applied gate voltage, temperature, and stress time [16,17]. In these works, they also assumed that the generated interface state is designing a substrate gate interface bond with their energy distribution.

In this work, we have modified the existing model given by Kufluoglu et al. [10] and proposed a new geometry-based BTI model device for N-type $InGaAs$ HEMT (FinFET). The electron–hole generation constant and different parameter values are calculated for the $InGaAs - Al_2O_3$ interface. Due to the model dependency on the hydrogen diffusion consistent, this constant has been calculated for the $InGaAs - Al_2O_3$ interface. Further, the effectiveness of the proposed model has been tested with the TCAD simulator, and results are verified with state-of-the-art experimental results.

3. Proposed InGaAs HEMT

Figure 1 shows the architecture of the $InGaAs$-based HEMT [18]. The real physical device operation was simulated using a process equivalent TCAD simulation [19]. To design $In_{0.53}Ga_{0.47}As - Al_2O_3$ interface, InP was deposited over the insulator, and over it, an $InGaAs$ layer was deposited for device formation. Then, a Al_2O_3 gate insulator layer was deposited at the top. Tin material was deposited over the $InGaAs$ layer which formed the gate layer. After the device design, a simulation-based device characterization was done using the *Sdevice* TCAD simulator [19]. The values used for R_{ON} and I_{OFF} are 180 Ω/μm and 100 nA/μm, respectively, are obtained at V_{DS} = 0.5 V and calibrated as per the experimental data [20]. Other important parameters are shown in Table 1. Figure 2 shows the current–voltage characteristics of a device with W_{fin} = 22 nm, and L_g = 30 nm. Figure 2 and Table 1 both show the calibration results with experimental data [20].

Table 1. Device parameters for Indium-Gallium-Arsenide ($InGaAs$)-based High Electron Mobility Transistors (HEMT) as per the experimental results [20].

Operating voltage V_{DD} [V]	0.5
Operating overdrive =2/3 * V_{DD} [V]	0.33
EOT [nm]	1.8
Operating E_{ox} [mV/cm]	2
H_{fin} [nm]	35
W_{fin} [nm]	10
L_{Gate} [nm]	30
PBTI time exponent (n)	0.1
$\Delta V_{th}(t = 10Y)$ @$Op.E_{ox}$ [mV]	118
$\Delta N_{eff}(t = 1s)$ @$Op.E_{ox}$ [cm^{-2}]	2×10^{11}

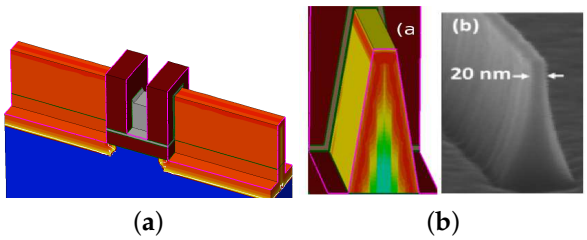

Figure 1. Proposed device (**a**) architecture and (**b**) aliment of the fin as per the experimental data [20].

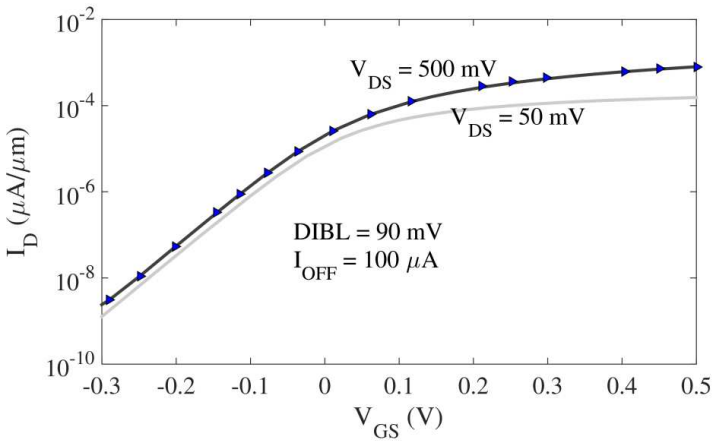

Figure 2. Calibration of the transfer characteristics of device with W_f = 22 nm and L_g = 30 nm with the experimental data (blue symbol graph) [20].

To understand the BTI effect in the proposed device, we need to understand the bulk–oxide and oxide–metal interface properties. The properties of this interface depend on the gate oxide materials such as SiO_2, HfO_2, La_2O_3, Al_2O_3, and $TaSiO_x$. The unbounded states, the band-decomposed charge density corresponding to the bandgap pinning energy interval are shown in a 3D plot by Kim et al. [21]. This 3D plot can be used to determine the exact location and the number of dangling bonds at the $InGaAs$ and Al_2O_3 insulator interface. The unbounded states are localized at the existing coordinated Aluminum (Al) atoms which have bonded with two Oxygen ($O's$) atoms and one Hydrogen (H) atom. In amorphous bulk, Al_2O_3 and Al primarily have four bonds with O, as shown in Figure 3. These dangling bonds change the electrical properties of a device and increase the density of the existing interface trapped charges (N_{it}).

Active depletion charge density is used to understand the interface properties which gives the device reliability information. The active interface charge in the depletion region can be measured using a quasi-static and high-frequency capacitance–voltage model. Figure 4 shows bi-directional capacitance–voltage (CV) curves for different gate insulator interfaces for $InGaAs$-based HEMT [22]. These data are taken from published experimental work [22]. Figure 4 shows the initial charge density for La_2O_3-based gate insulator is lower because the trivalent oxides Al_2O_3 and La_2O_3 have fewer dangling bonds. Having fewer dangling bonds reduces the interracial state. However, La_2O_3 is very unstable material [22], hence we are using Al_2O_3 as a gate insulator material in the proposed $InGaAs$-based HEMT. The next element of the proposed work is an SRAM cell for the IoT applications, which is explained in the next section.

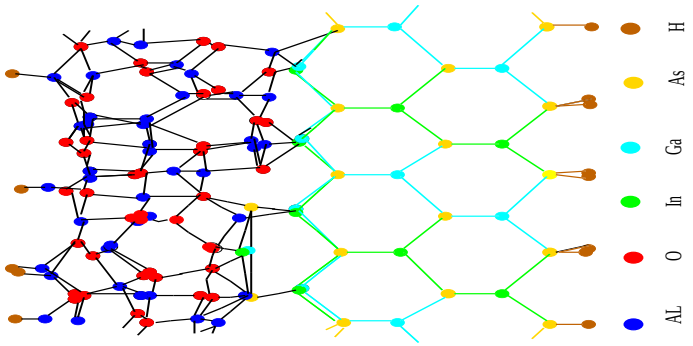

Figure 3. The amorphous oxide interface ($InGaAs - Al_2O_3$) shows the initial structure of oxide bulk placed on the clean semiconductor–oxide interface.

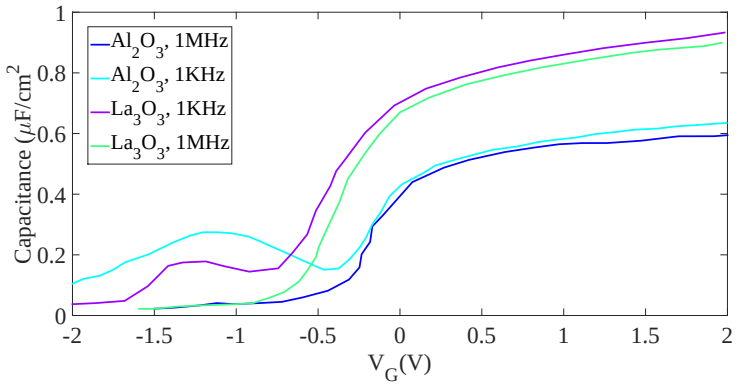

Figure 4. Capacitance voltage (CV) curves of different materials at 1 KHz and 1 MHz frequencies (AC analysis).

4. BTI Effects on 6T SRAM Cell

Figure 5 shows a 6T SRAM cell, which is designed by the *InGaAs*-based HEMT. It can also be called FinFET for circuit applications. The design parameters (Fin Number (NF)) of the proposed SRAM transistors are as follows; driver(PD) NF = 4, Access(A) NF = 2, and Pull-Up (PU) NF = 4. Data retention stability under standby condition is analyzed by Static Noise Margin (SNM), and read stability is analyzed by Read Noise Margin (RNM). Synopsys TCAD-mixed-mode simulator has been used for the *InGaAS* device-based circuit simulation. The 6T SRAM cell was analyzed in both standby and read mode operations using the two-stage NBTI and degradation models in [19]. The trap charge density under three-year stress in standby mode operation is shown in Figure 6. The figure shows a single driver transistor for the two-stage NBTI model because symmetric inverters design the 6T SRAM cell and NBTI affects the PMOS transistors only. In the degradation model, the effect of BTI is plotted for both NMOS and PMOS [19,23]. TCAD simulation results show a significant change in the trap charge density.

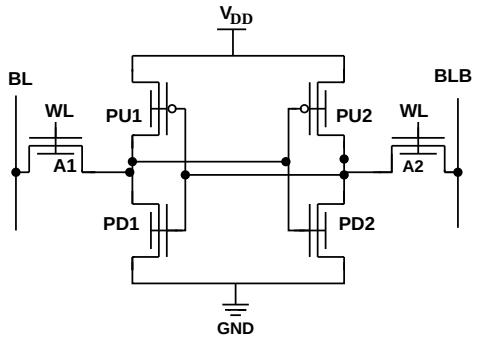

Figure 5. 6T SRAM cell design using proposed *InGaAs*-based HEMT (FinFET).

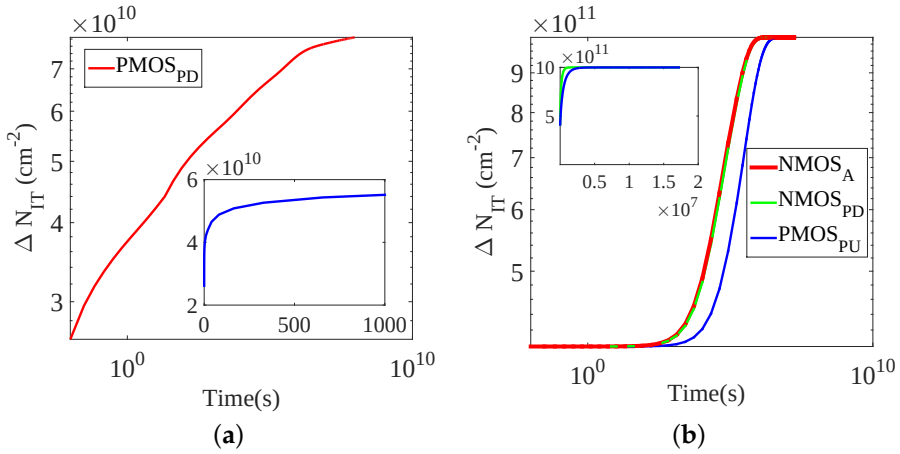

Figure 6. Change in trap charge carrier concentration due to NBTI and PBTI in 6T Static Random-Access Memory (SRAM) cell transistor in standby mode of operation: (**a**) using two stage NBTI model and (**b**) using degradation model (NBTI and PBTI).

The SNM butterfly curves of the proposed SRAM cell is shown in Figure 7a. We take a standard Gaussian doping and initial $N_{IT} = con = 4 \times 10^{12}$. The N_{IT} increases with three-year stress. A similar result is also shown for the RNM (as shown in Figure 7b). These variations can not be considered under the most of the available spice–circuit simulators. Hence, most of the circuit simulators can not predict the reliability of the chip (in terms of the lifetime). The MOSERA model bases reliability simulation can be performed in the H-SPICE simulator, but it uses a fundamental power–law model. Hence, the proposed BTI model, which is developed especially for *InGaAs*-based FinFET, can be used in circuit simulation.

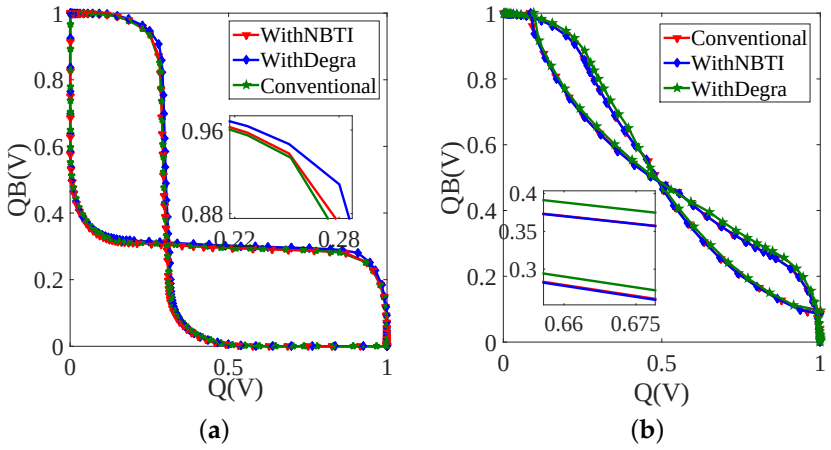

Figure 7. Change in 6T SRAM cell stability due to NBTI and PBTI: (**a**) Static Noise Margin (SNM) and (**b**) Read Noise Margin (RNM).

5. Proposed BTI Model for HEMT

HEMT is a three-dimensional (3D) device with three trapping regions; two of them are from side walls and one from the top. Top and side walls show one-dimensional (1D) trap-induced BTI, whereas the corners show two-dimensional (2D) trap-induced BTI, as shown in Figure 8.

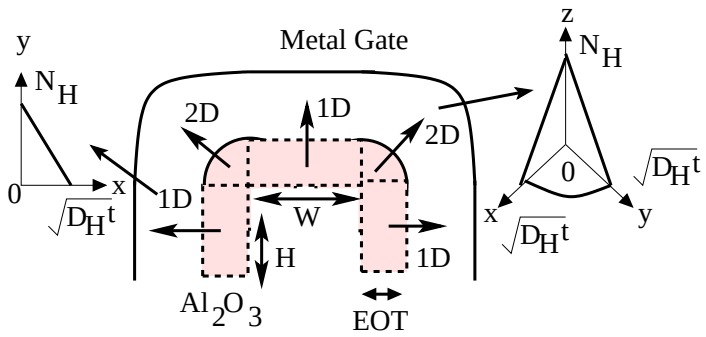

Figure 8. Cross section of the interface at the fin, 1D from the side walls and corners contributes the 2D trap-induced Bias-Temperature-Instability (BTI) effect.

We have already discussed that the RD model is used for the electric's stress-induced trapping. The RD model follows the time-dependent power–law model [10]. In the RD model, the shift in NMOS parameters induced by PBTI is represented by the breaking of the hydrogen passivated substrate material bonds in the $InGaAs--Al_2O_3$ interface. The total charge trap density at $InGaAs--Al_2O_3$ interface due to BTI (PBTI and NBTI) is given by [10]:

$$\frac{dN_{IT}}{dt} = k_f\left[N_0 - N_{IT}\right] - k_r N_{IT} N_H(x=0,t) \tag{1}$$

$$\frac{dN_{IT}}{dt} = D\frac{dN_H(x,t)}{dx}|_{x=0} + \frac{\delta}{2}\frac{N_H(x,t)}{dt} \tag{2}$$

where N_0 is the initial trap charge density and N_{IT} shows the total interface charge due to the BTI in the $InGaAs--Al_2O_3$ interface. N_{IT} depends on the rate at which H atoms are generated. Therefore, k_f is the H generation rate and k_r is the annealing rate. This parameter is used in the recovery phase. Some time N_{IT} may approach N_0 because the diffusion process is slower than ionization and annealing [13]. Annealing is responsible for the removal of hydrogen from the $InGaAs-Al_2O_3$ interface. The diffusion process can also be considered to be taking place in the quasi-steady-state condition of this reaction. Therefore, $dN_{IT}/dt \sim 0$ Equation (1) may be simplified as:

$$\frac{k_f(N_0 - N_{IT})}{k_r} = N_H^0 N_{IT} \tag{3}$$

Using this relation in Equation (2), the total trap charge density can be modeled by:

$$\frac{dN_{IT}}{dt} = D_H\frac{N_H^0}{\sqrt{D_H t}} = \sqrt{\frac{D_H}{t}}\frac{k_f}{k_r}\left(\frac{N_0 - N_H}{N_{IT}}\right) \tag{4}$$

Equation (1) shows that the trap charge density increases with the net reaction. Diffusion in FinFET is a process that happens in 2D at the corners and in 1D at the top and sidewalls. Hence, Equation (1) cannot be used to describe this process. For a more realistic representation, diffusion in the 1D and 2D are explained first. Assuming that H is one interface yields to the equation $N_{IT}(t) = \int N_H(r,t)d^3r$. It is previously mentioned that the rate at which H atoms are released is much greater than the diffusion rate. The hydrogen profile represented by $(D_H t)^{0.5}$ is shown on the left side of Figure 8b. Therefore, the 1D diffusion of hydrogen on a plane surface in the x direction is derived as:

$$N_{IT}^{1D}(t) = \int_0^{\sqrt{D_H t}} N_H^0\left(1 - \frac{x}{\sqrt{D_H t}}\right)dx \tag{5}$$

by putting values from Equation (3) into Equation (5), we obtain the solution:

$$N_{IT}^{1D}(t) = \sqrt{\frac{k_f N_0}{2k_r}}(D_H t)^{0.25} \tag{6}$$

Further, The hydrogen diffusion at the corners is a 2D process, as shown in Figure 8. There, the corresponding hydrogen diffusion profile is shown on the right in Figure 8b, which is circular and makes only a 1/4 circles at each corner, which is obtained by the circumference of the circle [10].

$$N_{IT}^{2D}(t) = \frac{1}{4}\int_0^{\sqrt{D_H t}} N_H^0 \left(1 - \frac{r}{\sqrt{D_H t}}\right) 2\pi r dr \tag{7}$$

where r is the radius of the circle which is equivalent to the thickness of the oxide. Now putting the values from Equation (3) into Equation (7)

$$N_{IT}^{2D}(t) = \sqrt{\frac{\pi k_f N_0}{12 r k_r}}(D_H t)^{0.5} \tag{8}$$

Similarly, the above explanation can be used to estimate the diffusion of hydrogen on a 2D surface. In the prescribed structure, the side and top walls show 1D diffusion, whereas the two corners show the 2D diffusion interface, as shown in Figure 8a,b. Hence, the interface state density generated by BTI is given by:

$$\begin{aligned} N_{IT_{stress}} = & \left[2\int_0^{\sqrt{D_H t}} N_H^0 (1 - \frac{x}{\sqrt{D_H t}})\right] dx \\ & + \int_0^{\sqrt{D_H t}} N_H^0 (1 - \frac{y}{\sqrt{D_H t}}) dy \\ & + \frac{2}{4}\int_0^{\sqrt{D_H t}} N_H^0 (1 - \frac{r}{\sqrt{D_H t}}) 2\pi r dr \end{aligned} \tag{9}$$

By substituting $r = t_{ox} \sim EOT$ and W into Equation (1), we can write:

$$N_{IT_{stress}}(t) = \sqrt{\frac{k_f N_0}{2k_r}} \left[(D_H t)^{\frac{1}{2}} + \frac{\pi (D_H t)}{9 W t_{ox}}\right]^{\frac{1}{6}} \tag{10}$$

where, k_f and k_r are the rates of generation of H_2 i.e., electron/hole and k_r is the annealing rate. The shift of the trap threshold is described by:

$$V_{th} = \alpha \frac{q}{C_{ox}} N_{IT_{stress}} \tag{11}$$

where α is a multiplication factor that depends on the type of device structure, temporal parameter degradation caused by BTI depends on the physical properties of the channel and type of gate oxide.

We did not work on the recovery model and we have used the recovery model as given by Reis et al. [24]. The recovery process happens in two stages: The first stage involves a fast recovery caused by H_2 atoms inside the gate oxide. The second stage involves a slow recovery caused by H_2 due to the back diffusion from gate oxide to $InGaAs$ (bulk or channel). The number of annealed traps consists of two parts represented by the recombination of H_2 in Al_2O_3 and the back diffusion of H_2 in the gate. At the end of the stress (time t_0), the number of generated trap charges is given by the following equation and it becomes zero if $k_f = 0$:

$$\frac{N_{IT_{rec}}}{dt} = -k_r (N_H^0 - N_H^*)(N_{IT}^0 - N_{IT}^*) \tag{12}$$

where, N_H^0 is the hydrogen concentration generated after stress at time t_0 and C is a constant [7]. Therefore, the change in threshold voltage after recovery is given by:

$$V_{th} = \alpha \frac{q}{C_{ox}} N_{IT_{rec}} \tag{13}$$

where α is a multiplication factor that depends on the type of device structure, Equations (11) and (13) describe the stress and recovery process of the trap charges caused by NBTI/PBTI for $InGaAs$-based HEMT, respectively.

6. Modeling of Charge Generation Constant

In this section, a mathematical model of the electron/hole generation constant (K_f) for $InGaAs$–FinFET (HEMT) is derived. The following expression conventionally gives the K_f constant:

$$K_f = \sigma E_{eff} P_{eff} \tag{14}$$

where σ is the electron/hole capture cross-section, E_{eff} is the effective oxide field across the gate oxide, and P_{eff} is the effective potential. Such factors were all investigated in previous material level studies [25,26]. σ depends on the activation energy, temperature, doping concentration, and the layer thickness [25]. The electron capture cross-section area is an important parameter for K_f. If the capture cross-section is more than K_f, is also more. The electron capture cross-section areas are greater, by 3× of magnitude, than the hole capture cross-section. The electron capture cross-sectional area is very large and has a value that ranges from 10^{-15} to 10^{-14}. It depends on the recombination center [25,26]. The value of σ for $InGaAs$-based HEMT can be given by:

$$\sigma = \sigma_\infty exp(\frac{-E_B}{KT}) \tag{15}$$

where E_B is the activation energy, σ_∞ is the pre-exponential factor, K is the Boltzmann constant, and T is the temperature in Kelvins. The values of the pre-exponential factor σ_∞ and the activation energy E_B for an $InGaAs$ substrate and insulator Al_2O_3-based HEMT are derived in this work. The default value of σ_∞ used in the literature is in the range of 6×10^{-15} to 1×10^{-17} [25], and the values of σ_∞ for $GaAs$ and $InGaAs$ are 6×10^{-15} and 1×10^{-20}, respectively [25]. Hence, these values have been employed in different simulation experiments to find the optimal value for the $InGaAs - -Al_2O_3$ interface. The change of the electron capture cross-section with respect to temperature variation is depicted in Figure 9 which shows that K_f is directly proportional to the temperature and that K_f increases as V_{gs} increases. The effective oxide field (E_{eff}) and the effective potential P_{eff} depends on the gate voltage (V_{gs}), the threshold voltage (V_{th}), and the oxide capacitance (C_{ox}). Hence, k_f can be modeled as:

$$k_f = \sigma_\infty exp(\frac{-E_B}{KT}) \left[exp(\frac{E_{ox}}{E_0}) C_{ox}(V_{gs} - V_{th}) \right] \tag{16}$$

$$k_r = \sigma_\infty exp(\frac{-E_B}{KT}) \left[C_{ox}(V_{gs} - V_{th}) \right] \tag{17}$$

The annealing constant K_r also depends on the oxide electric field, the gate voltage, and the threshold voltage of the device. For K_r, V_{gs} is either zero or has a positive value for apposite stress. The values of E_{ox} and E_0 are always zero. The parameter values extracted from the simulation results and are listed in Table 2.

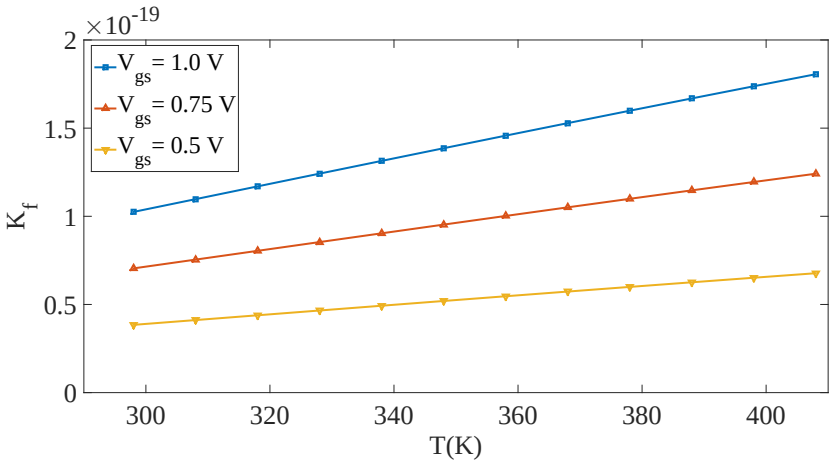

Figure 9. Hold generation constant for the $InGaAs--Al_2O_3$ interface for varying temperatures (T).

Table 2. Extracted BTI model parameters for $InGaAs--Al_2O_3$ interface.

σ_∞	1×10^{-16}
K	1.38×10^{-23}
EOT	1.8 nm
$K_{Al_2O_3}$	9
ϵ_0	8.85×10^{-14}
$K_r = K_{r0}e^{\frac{E_A K_r}{kT}}$	$K_{r0} = 9.9 \times 10^{-7}$
D_{H0}	9.56×10^{-11} cm^2/s
E_a	0.2 eV
E_{ox}	2 eV
E_0	0.5 eV
N_0	2×10^{11}
ξ	0.58
E_B	0.054 eV

Modeling of Hydrogen Diffusion Constant

Another important factor for BTI-induced trapping is Hydrogen diffusion constant (D_H). As per experimental data, the value of E_B for the $InGaAs$–Al_2O_3 interface is in the range of 0.05 to 0.066 eV [5,25]. Temperature is important parameter for the diffusion constant. These parameters were extracted for the BTI model using different experimental data in these papers [5,25]. The Hydrogen diffusion constant D_0 is given by:

$$D_H = D_0 exp(\frac{-E_a}{KT}) \tag{18}$$

where E_a is the activation energy, K is the Boltzmann constant, and T is the temperature. The value of D_0 for H_2 diffusion in Al_2O_3 ranges from 1.5×10^{-5} to 1×10^{-6} as per the state-of-the-art experimental results [5,25]. The diffusion constant values for varying temperatures are shown in Figure 10 which shows that the diffusion constant is highly dependent on the temperature. Therefore, the temperature is an important parameter required to estimate K_f, K_r, and D_H. All the related parameters for the $InGaAs$-based HEMT are shown in Table 2.

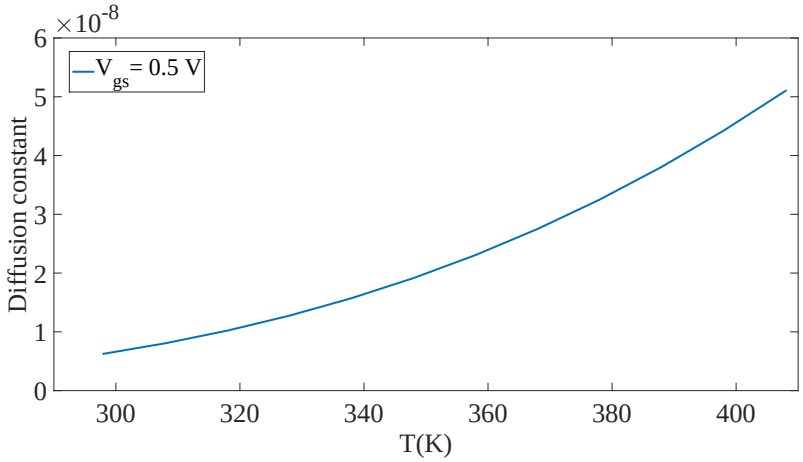

Figure 10. Diffusion constant for $InGaAs--Al_2O_3$ interface with varying temperatures.

7. Model Verification and Circuit Simulation

To verify the proposed model, modeling results are compared with the experimental result. The first model is verified for silicon-based MOSFET (Figure 11) and further, it is verified for 3D InGaAs HEMT. It is also used to predict the lifetime prediction of the SRAM. The required parameters are calculated from the model file for the model. The flat band voltage and the vertical gate oxide (E_{ox}) are calculated from the BSIM model then the change in the threshold voltage (V_{th}) due to PBTI is calculated. All calculated and optimized parameters are shown in Table 2. The comparative results for the model with the experimental results for the change in the threshold voltage are shown in Table 3 [27–30]. All results are calculated for different device dimensions, but one of the available studies is very similar to the proposed work, hence, we made a detailed comparison with the similar study. Hence, the proposed model has been further verified using the experimental results for 10-year stress and different temperatures values obtained from data given by Franco et al. [30]. The stress voltage from -1 V to maximum V_{gs} has been applied for the P-FinFET. The initial trap density (N_0) from -1 V to maximum V_{gs} was extracted from [30]. The hole capture constant (K_f) is calculated using the proposed model and calibrated as per the literature. The simulation results for 10-year stress are shown in Figure 12 [30] which clearly shows that PBTI is strongly affected by the vertical electric field has a linear relationship with V_{gs}. A similar plot at a *log* scale is shown in Figure 13 [30].

Table 3. Comparison of the modeling results with the experiment results.

S.No.	ΔV_{th}	Stress Time(s)	t_{ox}	Ref.
1	0.15	1000	2.0	[27]
2	0.125	1000	4.2	[28]
3	0.15	1000	3.5	[29]
4	0.15	1000	1.8 nm	[30]
4	0.15	1000	1.8 nm	Calculated in this work

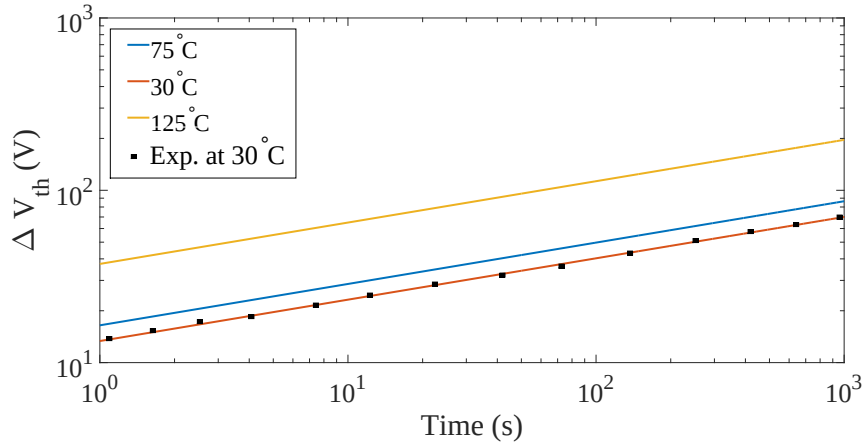

Figure 11. NBTI model results compared with measured data for SiO_2 and Si interface of a MOSFET.

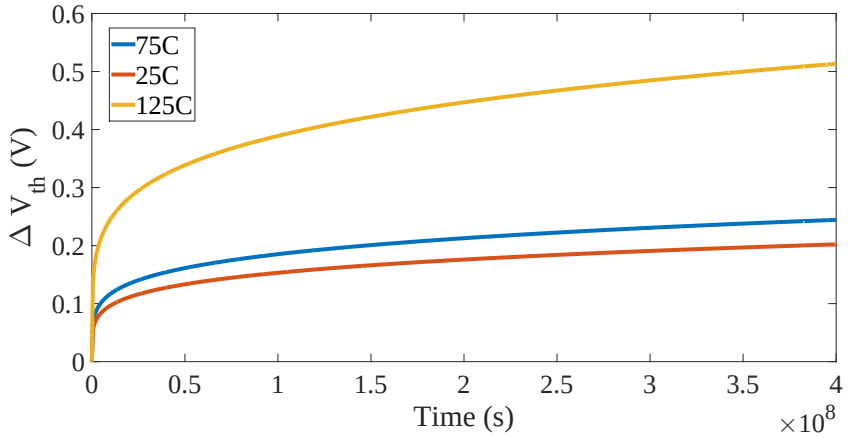

Figure 12. PBTI model results compared to the measured data for the $InGaAs$ to Al_2O_3 interface.

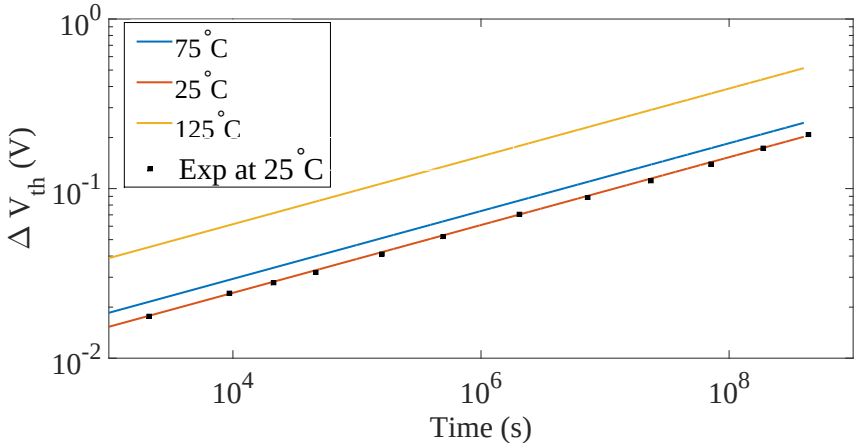

Figure 13. PBTI model results compared to the measured data for the $InGaAs$ to Al_2O_3 interface in log scale.

Circuit simulation was conducted using the 6T SRAM cell for testing purposes. The total change in the trap charge density for three-year stress and the corresponding shift in the threshold voltage was calculated. The simulation flow and strategy are shown in Figure 14. The initial charge density and the other parameters are calculated from the device model file. In HSPICE, the parameters given by the *.param* command in the spice net-list are used to calculate the change in the threshold voltage due to BTI i.e., $v_{th} = v_{th0} + \Delta V_{th}$. The *.alter* command used to simulate the second stage gives the

final simulation output. Figure 15 shows the comparative results of the proposed model and TCAD simulation for a 6T SRAM cell. The SNM and RNM results of the 6T SRAM cell are calibrated according to the TCAD simulation results.

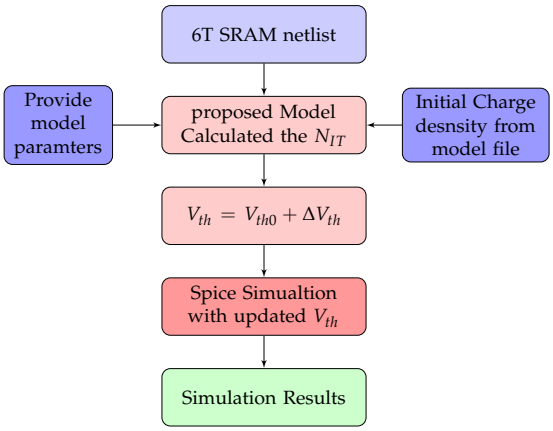

Figure 14. Proposed flow chart for the SRAM circuit simulation in a spice-based circuit simulation environment using the proposed model.

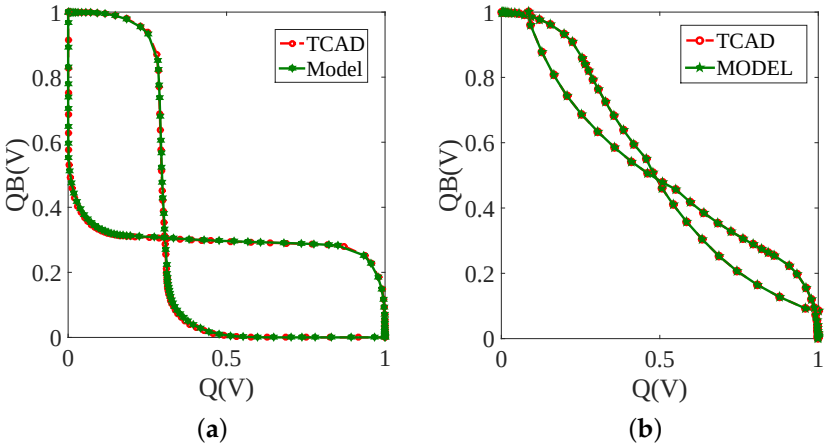

Figure 15. Model calibration results for the 6T SRAM cell stability: (**a**) SNM; (**b**) RNM.

8. Conclusions

Static Random-Access Memory (SRAM) is used as a data storing and processing element in Wireless Sensor Networks and the Internet of Things (IoT) applications. Hence, SRAM should be a high-performance, reliable element. In this work, We have analyzed the stability of the 6T using the two-stage NBTI and degradation models under the deference electric stress. It is revealed from the results that NBTI affects almost 20% of the stability compared to the conventional target design only in the three-year stress. Also, the RD-based BTI model was modified for the 3D *InGaAs*-based HEMT and presented as a proposed BTI model for circuit simulation. This model has been used for lifetime prediction of the 6T SRAM cell. The BTI model parameters have been calculated, extracted, and optimized using material parameters and device geometrical dimensions. The modified model contains all the main characteristics of the reaction–diffusion model. The proposed model can be used to predict DC stress for electrical stresses. Consequently, this model can be utilized to predict BTI under real device and circuit working conditions.

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