*Article*

# Layout Strengthening the ESD Performance for High-Voltage N-Channel Lateral Diffused MOSFETs

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**Abstract:** An electrostatic discharge (ESD) event can negatively affect the reliability of integrated circuits. Therefore, improving on ESD immunity in high-voltage (HV) n-channel (n) lateral diffused metal–oxide–semiconductor field-effect transistor (HV nLDMOS) components through drain-side layout engineering was studied. This involved adjusting the operating voltage, improving the non-uniform turned-on phenomenon, and examining the effects of embedded-device structures on ESD. All proposed architectures for improving ESD immunity in this work were measured and evaluated using a transmission-line pulse system. The corresponding trigger voltage ($V_{t1}$), holding voltage ($V_h$) and secondary breakdown current ($I_{t2}$) results of the tested devices were obtained. This paper first addresses the drift-region length modulation to design different operating voltages, which decreased as the drift region length and shallow trench isolation (STI) length shrunk. When an HV nLDMOS device decreased to the shortest drift region length, the $V_{t1}$ and $V_h$ values were closest to 21.85, and 9.27 V, respectively. The $I_{t2}$ value of a low-voltage operated device could be increased to a maximum value of 3.25 A. For the channel width modulation, increasing the layout finger number of an HV LDMOS device did not really help the ESD immunity that because it may suffer the problem of non-uniform turned-on phenomenon. Therefore, adjusting the optimized channel width was the best one method of improvement. Furthermore, to improve the low ESD reliability problem of nLDMOS devices, two structures were used to improve the ESD capability. The first was a drain side—embedded silicon-controlled rectifier (SCR). Here, the SCR PNP-arranged type in the drain side had the best ESD capability because the SCR path was short and had been prior to triggering; however, it also has a latch-up risk and low $V_h$ characteristic. By removing the entire heavily doped drain-side $N^+$ region, the equivalent series resistance in the drain region was increased, so that the $I_{t2}$ performance could be increased from 2.29 A to 3.98 A in the structure of a fully embedded drain-side Schottky diode. This component still has sufficiently high $V_h$ behaviour. Therefore, embedding a full Schottky-diode into an HV nLDMOS in the drain side was the best method and was efficient for improving the ESD/Latch-up abilities of the device. The figure of merit (FOM) of ESD, Latch-up, and cell area considerations improved to approximately 80.86%.

**Keywords:** electrostatic discharge (ESD); latchup (LU); n-channel lateral diffused MOSFET (nLDMOS); non-uniform conduction; secondary breakdown current ($I_{t2}$); transmission-line pulse system (TLP system)

## 1. Introduction

As semiconductor technology progresses, the functions and efficiency of integrated circuits (ICs) have greatly improved, and microelectronic circuits and power technologies are receiving more attention. In recent years, many electronic manufactures have been designing intelligent products, smart power systems, intelligent vehicles, and Internet of things (IoTs) applications [1–9]. Among these,

electrostatic discharge (ESD) damage remains a serious problem in high-voltage (HV) units. However, IC applications for HV power conversion must remain highly reliable.

Lateral diffused metal–oxide–semiconductor field-effect transistor (LDMOS) devices have been efficiently applied to ICs for power electronics, power managements and display driver, given their advantages of low ON-resistance and ability to withstand high operating voltages [10–16]. Therefore, design methods for each operating voltage devices to develop various HV and low-voltage devices by using single-process chips are crucial for many applications. The ESD immunity of devices, under different operating voltages, is worthy of investigation. Furthermore, LDMOS devices may act as HV devices and ESD protection device simultaneously. To reduce the effects of ESD, improving the self-protection performance of HV devices is significant [17–28]. Therefore, to achieve good ESD capability in devices, parameters including trigger voltage ($V_{t1}$), holding voltage ($V_h$), and secondary breakdown current ($I_{t2}$) are critical. Theoretically, the $I_{t2}$ value of devices is a standard evaluation for defining the ESD capability and should have a sufficient $I_{t2}$ value for a device to withstand high ESD currents. Therefore, the human-body model (HBM) ESD capability of a component is actually closely related to the $I_{t2}$ measurement value of the component. However, the holding voltage value must be high enough to avoid the latch-up (LU) problem.

In this study, the operating voltage of a device was adjusted by varying the drift-region length (shallow trench isolation [STI] or drift region modulation) to conveniently form various n- channel (n) LDMOS (nLDMOS) devices operating under different operating voltages. Unfortunately, the ability of discharging ESD current remains affected by the non-uniform turned-on phenomenon for the multi-finger layout type, which easily weakens the immunity level per unit device width from ESD particularly for HV LDMOS devices [29–31]. Therefore, after confirming the length effect of the drift region, the total channel width and finger number of an MOSFET should be adjusted to clearly understand the non-uniform turned-on problem in the benchmark (reference) nLDMOS device. Then, strengthening the ESD capabilities of an HV LDMOS through drain-side device engineering is necessary. Some improvement techniques embed a silicon-controlled rectifier (SCR) to improve the discharge capability. However, this may cause an LU effect because of its very low holding voltage [32–36]. Therefore, this study evaluated the effect of different parasitic SCR paths on the ESD immunity of LDMOS related devices. The last part of the study involved removing the heavily doped $N^+$ region to embed a parasitic Schottky diode into the drain side of an HV nDLMOS. The series resistance characteristics of embedded Schottky diodes in the drain side indicated that this method can effectively increase the $I_{t2}$ value (ESD reliability) of HV nLDMOS devices.

## 2. Cell Design of the HV nLDMOSs

### 2.1. HV nLDMOS Reference Device

Generally, nLDMOS devices are operated in an HV environment for many applications. Therefore, this paper focuses on the physical-parameter optimization and ESD capability enhancement studies for HV nLDMOS devices. All samples of HV nLDMOS related devices were fabricated using a Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 μm HV Bipolar-Complementary metal-oxide-semiconductor-Double-diffused MOSFET (BCD) standard process with a gate-grounded nMOSFET (GGnMOS) configuration. Figure 1a displays a cross-sectional view of the HV nLDMOS Reference device, which has a long drift-region length D and STI isolation length Ds. The breakdown voltage ($V_{BK}$) of the nLDMOS device exhibited a higher HV performance as the large drift region resistance ($R_{drift}$) can suppress the high electric field concentrated at the gate edge and extend the length of depletion region. Moreover, the length of La in H60PW layer, which is below the gate electrode, could be adjusted to increase the channel length L and affect channel resistance. Figure 1b presents a three-dimensional (3D) structure view of the HV nLDMOS Reference device. When an MOSFET transistor under the configuration of a gate-grounded electrode forms a GGnMOS structure, it can discharge the ESD surge current through the parasitic bipolar-junction transistor (BJT) underneath.

This device can release ESD current through the drain side N$^+$, HV N-well, drift region H60NW, H60PW, SH_P, HVPB, and source side N$^+$ as the ESD current enters the device. Based on the device structure, the equivalent circuit of the nLDMOS Reference device is shown in Figure 1c; R$_{bulk}$ is the parasitic resistances of the source-to-bulk; the parasitic resistance (R$_{drift}$) in the drift region is sufficiently high, as compared with a conventional CMOS MOSFET. In this paper, various types of HV nLDMOS devices are designed with the multi-fingers layout. The total finger number is four (except for in Section 2.3), each channel length (L) is varied, the channel width is 75 μm (except for in Section 2.3), and STI length in the drain side is 12.83 μm. The layout view of the nLDMOS Reference device is presented in Figure 1d.
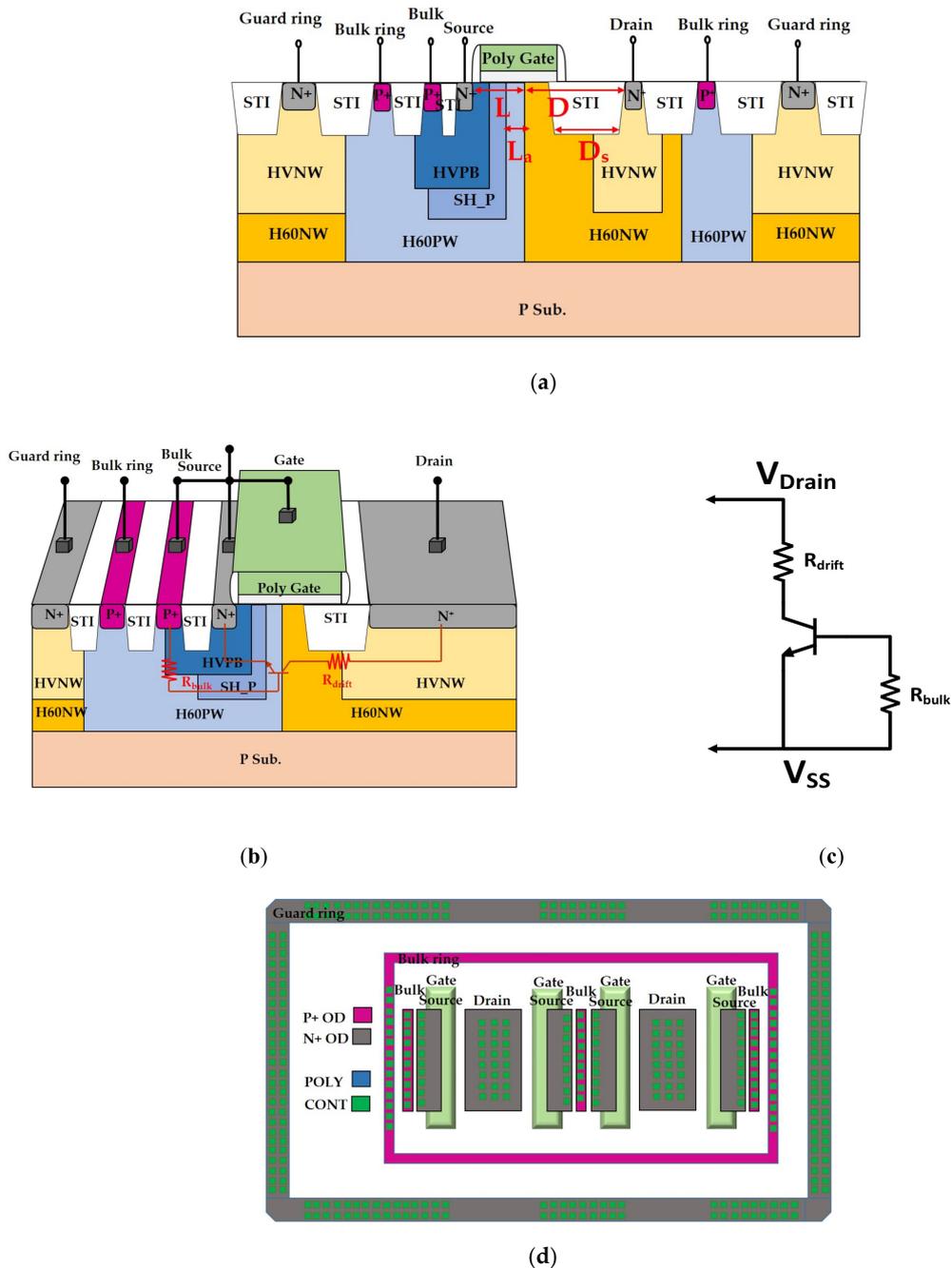


(a)



(b)



(c)



(d)

**Figure 1.** (**a**) Cross-sectional view, (**b**) three-dimensional (3D) structure view, (**c**) parasitic equivalent circuit, and (**d**) layout view of the HV nLDMOS Reference device.

## 2.2. HV nLDMOS DUTs with Drift Region Modulation (Operating Voltage Modulation)

　　As detailed in this subsection, the drain-side STI region (i.e., the STI length Ds) of the nLDMOS Reference device was shrunk. Figure 2a,b illustrate the 3D structure and layout view of an HV nLDMOS device with drift region modulation at the lowest voltage (shrunk to the shortest STI = 0 μm) usage. Due to thesufficiently long Ds, the nLDMOS Reference device could disperse a high electric field that focused on the gate edges and extended the depletion region for operation in HV situations. Therefore, drift region STI distance Ds was adjusted to achieve drift region modulation (which also shrinks the length D). The Ds distance reduced by a quarter from the original Reference device Ds (12.83 μm) in order, which were 9.63 μm (STI 3/4), 6.43 μm (STI 2/4), 3.23 μm (STI 1/4), and finally to the shortest 0 μm (STI 0) with the structure of the shortest length in the drift region, respectively. These devices were designed to effectively reduce the extended depletion region and drift resistance ($R_{drift}$) shown in Figure 1c, and these HV nLDMOS devices were estimated to be able to be appropriately adjusted for many voltage operations. Thus, their corresponding ESD reliability capabilities should be evaluated to discharge transient current through this process.
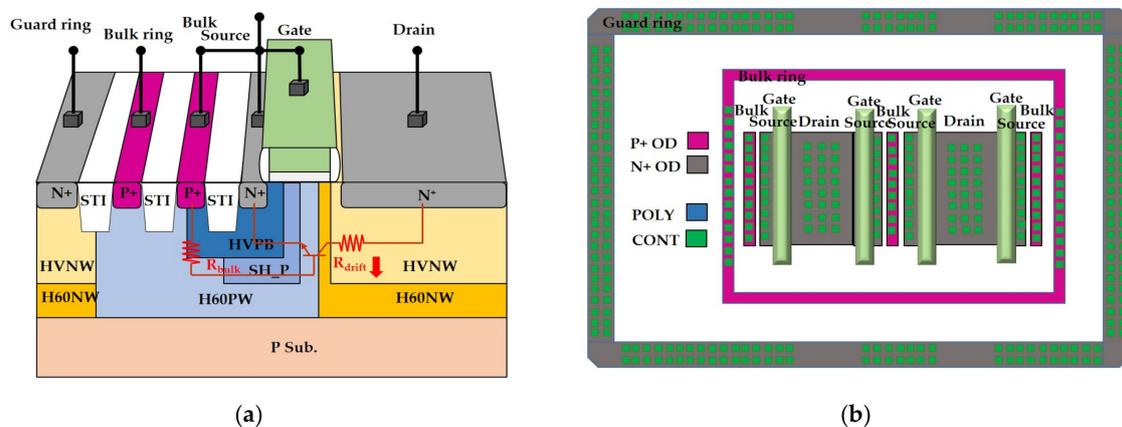


(**a**)　　　　　　　　　　　　　　　　　　　　　　　　　(**b**)

**Figure 2.** (**a**) 3D structure view; and (**b**) layout view of the HV nLDMOS with the shortest (STI 0) condition.

## 2.3. HV nLDMOS DUTs with Channel Width Modulation

　　To improve the withstand voltage and ESD immunity of an HV device, the layout ways need to be well-planned. For efficient manufacturing an HV semiconductor MOSFET device, it generally designed with a large channel width and multifinger layout manner. However, the issue of non-uniform turned-on phenomenon is always a serious problem in HV GGnMOS devices, because a multi-finger structure cannot fully turn on in each MOSFET, causing the ESD capability to be very weak per unit channel-width of ESD. Therefore, it seems to be no way to effectively protect a transient ESD current by this large cell-area HV nLDMOS.

　　The $R_{bulk}$ resistance of each finger shown in Figures 1b and 2a of a GGnMOS ESD device by the multi-finger structure will have a slight difference in manufacturing process. However, each finger of an nLDMOS device is independent and any one finger with the largest $R_{bulk}$ on-resistance will be the first one to turn on, where an ESD pulse occurred, this finger would easily reach the secondary breakdown. If the other fingers have not been triggered to turn on instantly, this nLDMOS device may reach the melting point to cause device failure. Eventually, the ESD immunity of this protection device becomes not proportional to the device size. As shown the voltage-current characteristic curve of a protection device in Figure 3, the difference between the secondary breakdown voltage ($V_{t2}$) and $V_{t1}$ values affects the turned-on probability and non-uniform turned-on issues on each MOSFET [24]. In order to enhance uniform conduction, it is generally desirable to adjust the snapback curve as shown by the dashed curve in Figure 3. Therefore, the next sub-section further purposes a drain-side embedded SCR structure to improve the ESD capability. This new added SCR can have a very strong capability

of ESD that can be applied in high voltage applications. However, it also has some disadvantages, which includes a very low $V_h$ value. In this sub-section, the finger number and channel-width effects of multi-finger nLDMOS devices will be evaluated for the issue of non-uniform turned-on problem. Then, the La length is adjusted and makes the channel length L= 2.75 µm in this nLDMOS Reference device. Figure 4a is a two-fingers (M = 2) structure with each channel width being 75 µm and the drain region sharing. Meanwhile, it will be used to compare the ESD capability between the two-finger and four-finger structures. Furthermore, Figure 4b was extended each channel width of Figure 4a to 150 µm, and its ESD capability will be compared with the device of Figure 1d (M = 4 and same total channel width).
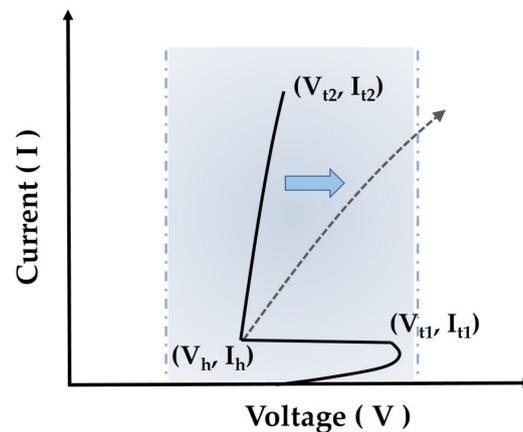


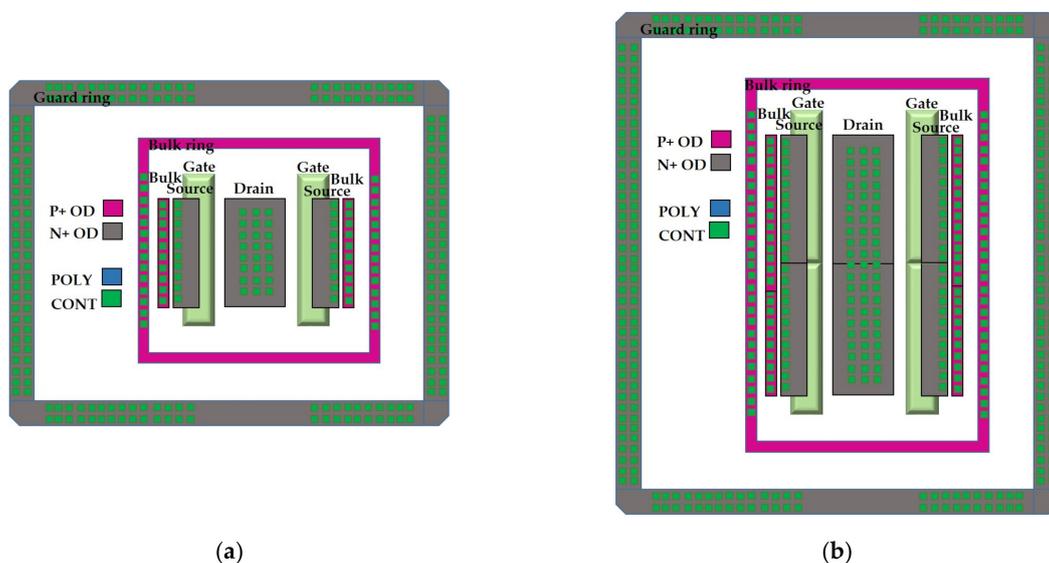**Figure 3.** Voltage-current characteristic curves of an ESD protection device.



| (**a**) | (**b**) |
|---|---|

**Figure 4.** Two-finger layout views of an HV nLDMOS with total channel width (Wtot) being (**a**) 150 µm, and (**b**) 300 µm.

## 2.4. HV nLDMOS DUTs with Embedded SCR Modulation

A silicon-controlled rectifier (SCR) is often applied in power electronics or as an ESD protection device as it has a strong capability in discharging transient current. In order to improve the ESD reliability of an nLDMOS, which has the serious problems, including non-uniform turned-on issue and low ESD capability in the multi-finger structure. Therefore, one idea based on the nLDMOS Reference device, a parasitic SCR element (by embedded a P$^+$ zone) can be built into the drain side. An HV nLDMOS with the drain side NPN-arranged type and PNP-arranged type for ESD dissipation. It means that these embedded SCRs may achieve the result of improving ESD capability on the nLDMOS

Reference device. Figure 5 shows some layout structures, which are divided the drain region into three or five equal partitions and regularly embedded P$^+$ zones to form four different embedded SCR arrangements. Figure 5a,c are the SCR embedded structures of NPN- and NPNPN-arranged types, which indicates that the SCR path is inner and longer to the drain electrode. On the contrary, Figure 5b,d are the SCR embedded structures of PNP and PNPNP-arranged types, and the SCR paths are outer and shortest to the both side of the drain electrode. Figure 6 shows the parasitic equivalent circuits of an nLDMOS with drain-side NPN- and PNP-arranged types. The main difference between these two circuits is the location of the P$^+$ implants of an SCR anode. Meanwhile, the drain end R$_{drain}$ is sufficiently high and cannot be neglected for these NPN- and PNP-arranged types. Similarly, the equivalent circuit situations of Figure 6 also occur for the drain-side PNPNP-arranged type and NPNPN-arranged type. Therefore, the major ESD discharging path will be varied and depended on these embedded SCRs locations. Eventually, they will affect the ability of nLDMOS-SCR related devices to withstand ESD surges.
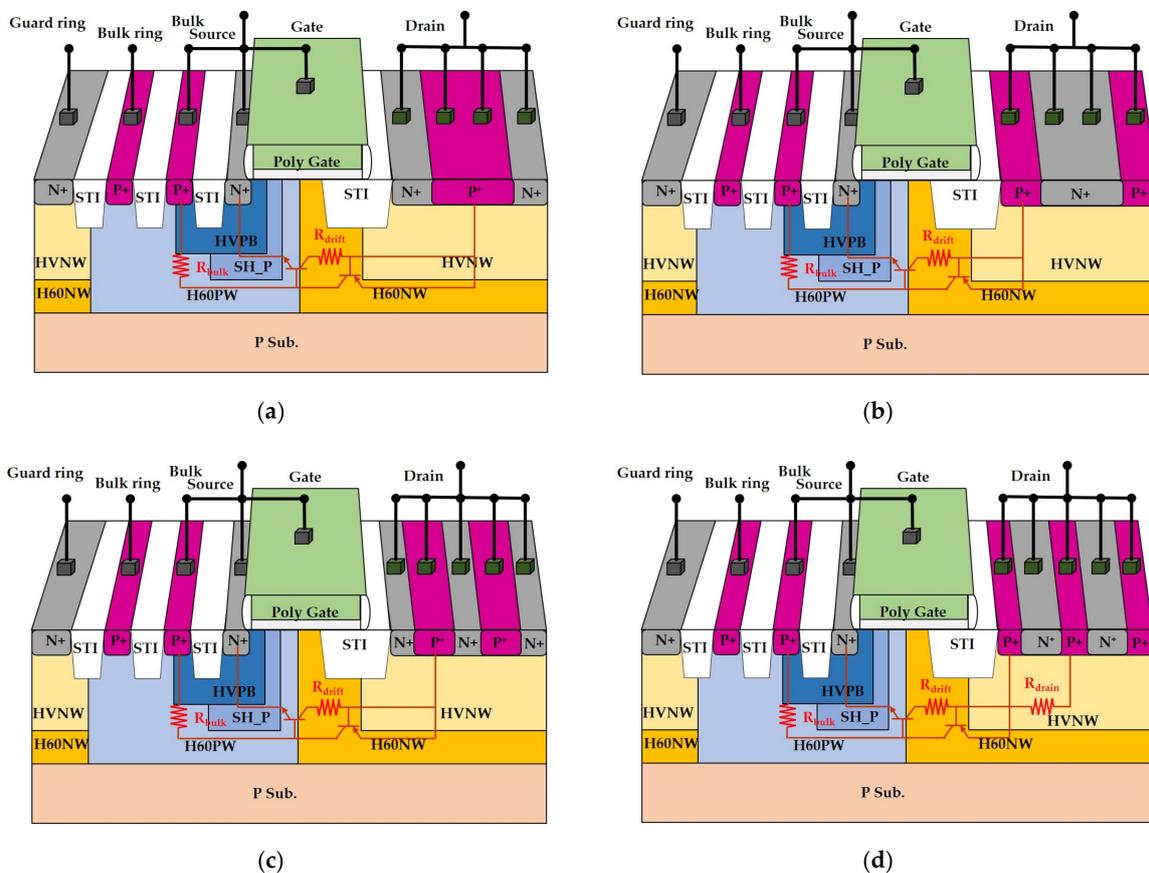


**Figure 5.** 3D structure views of an HV nLDMOS-SCR with drain-side; (**a**) NPN-arranged type, (**b**) PNP-arranged type; (**c**) NPNPN-arranged type; and (**d**) PNPNP-arranged type.

*2.5. HV nLDMOS DUTs with Embedded Schottky-Diode Modulation*

As mentioned previously, an nLDMOS device has the non-uniform turned-on problem as with a multi-finger layout. However, this component still need to have a perfect capability of self-protection when it acts as a protection device in integrated circuits, it means that this nLDMOS transistor need to have a good ESD dissipation capability. Therefore, in this sub-section, another reinforced structure which explored for purposes of increasing I$_{t2}$ level to improve the self-protection capability. The channel length of nLDMOS Reference device here is L = 2 μm. In order to improve the ability to discharge ESD current per unit area on the nLDMOS Reference device, the implants of heavily doped N$^+$ layer in the drain side were removed, which made this device forming an equivalent series Schottky-diode by

silicide and HVNW lightly-doped layer in the drain region. Therefore, the nLDMOS Reference device is changed and embedded a series Schottky diode in the current-conduction path. Figure 7a shows a 3D structure of full removing the entire drain side heavily-doped $N^+$ layer, it can be regarded as the original current discharging path with an embedded Schottky diode beneath the drain electrode. Thus, a heavily-doped $N^+$ ring around the central Schottky diode to form a structure of nLDMOS parallel with an embedded Schottky diode shown in Figure 7b. Different drain-side area ratios of the Schottky diode by periphery heavily-doped $N^+$ region is modulated, which is used to evaluate the ESD-capability influence upon the embedded different area ratio of Schottky diode at the drain side. Finally, the area ratio of heavily-doped $N^+$ versus Schottky diode region is shown in Table 1. Meanwhile, the parasitic equivalent circuits of an nLDMOS with drain-side full removing $N^+$ heavy doping and a central-type embedded Schottky diode modulation in the drain side are shown in Figure 8, respectively.
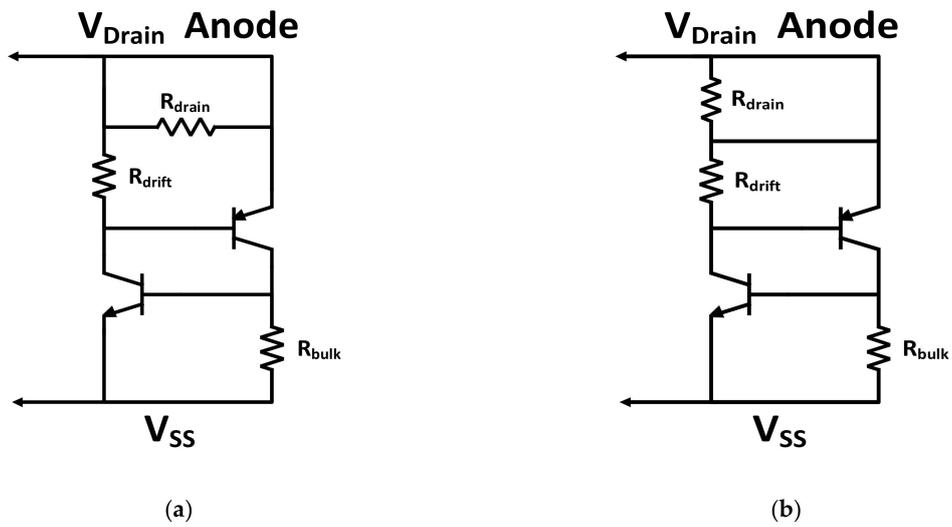


(a)

(b)

**Figure 6.** Parasitic equivalent circuits of an HV nLDMOS-SCR with drain-side; (**a**) NPN-arranged type; and (**b**) PNP-arranged type.
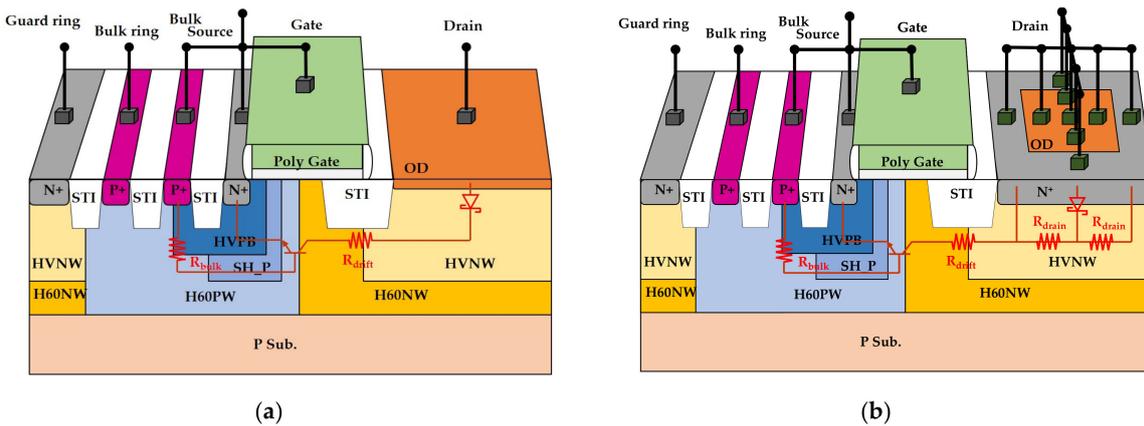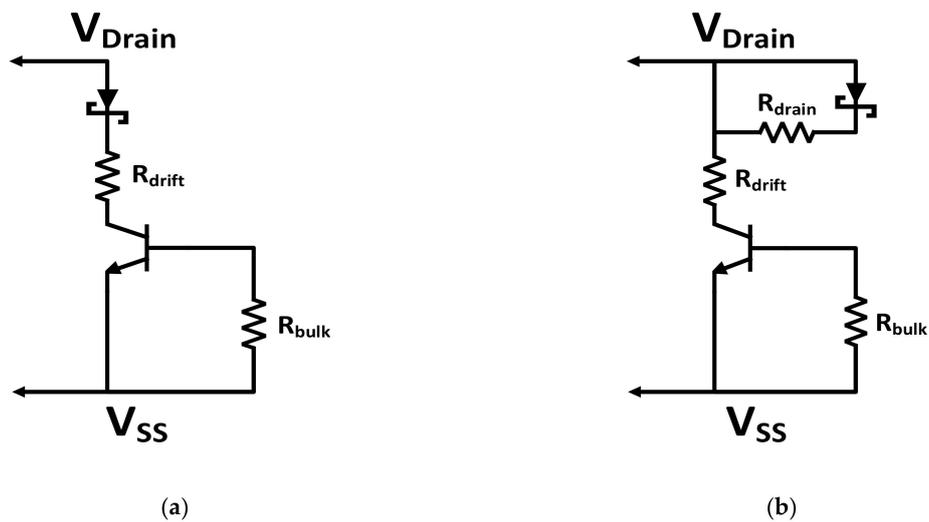


(a)

(b)

**Figure 7.** 3D structure views of HV nLDMOS as with (**a**) full removing $N^+$ heavy doping, and (**b**) a central-type embedded Schottky diode modulation in the drain side.

**Table 1.** Area ratios of N$^+$ and Schottky diode regions in the drain electrode.

| nLDMOS | N$^+$ (%) | Schottky (%) |
|---|---|---|
| Schottky_Drain | 0 | 100 |
| Schottky_SUR1 | 72 | 28 |
| Schottky_SUR2 | 84 | 16 |
| Schottky_SUR3 | 91 | 9 |
| Ref. DUT (L= 2 µm) | 100 | 0 |



(**a**)                                                                 (**b**)

**Figure 8.** Parasitic equivalent circuits of an HV nLDMOS with drain-side (**a**) full removing N$^+$ heavy doping, and (**b**) a central-type embedded Schottky diode modulation in the drain side.

## 3. Experimental Testing Systems

A measurement instrument of transmission-line pulse (TLP) system was used in this paper which is used to simulate the human-body model (HBM) of a transient waveform from an ESD event into a device and which is widely exercised to measure the ESD capability of protection devices. Furthermore, this system can generate a square wave with 100 ns short pulse width and has a short rising/falling time less than 10 ns, and the voltage-current characteristics including the trigger voltage ($V_{t1}$), holding voltage($V_h$) and secondary breakdown current($I_{t2}$) on the devices under test (DUTs) can be tested. Therefore, from these important physical extracted parameters, the capability of ESD immunity of these DUTs can be easily determined. Meanwhile, the breakdown-voltage measurement of a device is executed by a semiconductor parameter analyzer.

## 4. Experimental Results

### 4.1. ESD Capability of HV nLDMOS DUTs with Drift-Region Modulation (Operating-Voltage Modulation)

HV nLDMOSs of the Reference device and drift-region modulation devices were measured by a TLP testing machine, all of measurement results and important physical extracted parameters are presented in Figure 9 and Table 2. Then, it can be found that as the length of the drift region is reduced, the $R_{drift}$ resistance of the drift region shown in Figure 1c on a DUT will be decreased accordingly. Therefore, the DUT of STI0 would have properties for the lowest operating voltage, and the junction breakdown voltage ($V_{bk}$) would be decreased to the lowest voltage being 11.12 V. In Figure 10 (the $V_{t1}$ and $V_h$ distribution curves), because of reducing the length of STI region which will make the $V_{t1}$ having a significant downward trend due to a decreasing of the equivalent series resistance $R_{drift}$. Although the $V_h$ value has a little rising while shrinking the STI length by 1/4, however it will have a significant reduction as the STI length being decreased and then the series resistance decreased too. In addition, the $I_{t2}$ value has a slightly decreasing by reducing the drift region length at the

first and second adjustments, but the $I_{t2}$ abilities of the DUTs will also obviously increase after it continues to shrink which even promoted larger than the nLDMOS Reference device. This is also due to a decreasing of the series resistance and power consumption in the drift region, then the $I_{t2}$ distribution curve is shown in Figure 11. Moreover, when the drift region was shrinked to the shortest (STI0) DUT, the $V_{t1}$ and $V_h$ values were become to the lowest 21.85 V and 9.27 V, respectively. In other words, as the STI length is shrunk to 0, the STI zone in the drain side will be completely disappeared; the difference gap between $V_{t1}$ and $V_h$ values is smaller accordingly shown in Table 2. Then, the phenomenon of non-uniform turned-on of this new device has been slight which made the $I_{t2}$ value (STI0) has the largest value being 3.25 A, and it can be effectively applied to a low operating voltage situation. Moreover, the figure of merit (FOM) of the ESD, LU, and cell area considerations are defined as $(I_{t2} \times V_h)/\text{Cell-area}$. Then, the FOM value of the STI_3/4 DUT has highest performance being 3045.68 $\mu A \times V/\mu m^2$ in this modulation.
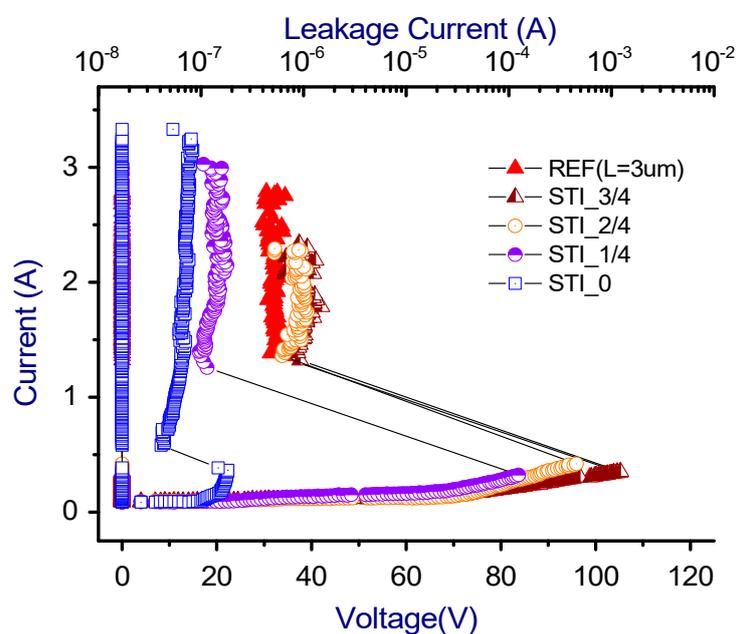


**Figure 9.** Snapback I-V curves and leakage currents of HV nLDMOSs with drift-region modulation.

**Table 2.** Snapback extracted parameters of HV nLDMOSs with drift-region modulation.

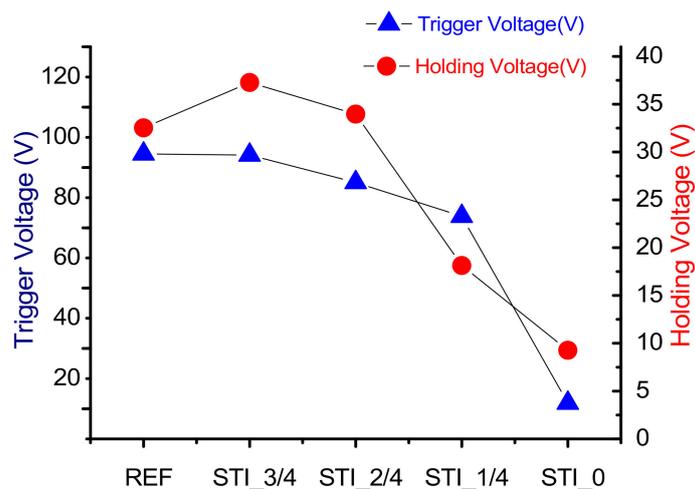| nLDMOS | $V_{t1}$ (V) | $V_h$ (V) | $V_{t1}$-$V_h$ (V) | $I_{t2}$ (A) | $V_{bk}$ (V) | FOM ($\mu A \times V/\mu m^2$) |
|---|---|---|---|---|---|---|
| Ref (L = 3 μm) | 104.47 | 32.53 | 71.94 | 2.79 | 23.52 | 2938.50 |
| STI_3/4 | 104.10 | 37.27 | 66.83 | 2.39 | 23.45 | 3045.68 |
| STI_2/4 | 95.02 | 33.97 | 61.05 | 2.32 | 23.40 | 2948.87 |
| STI_1/4 | 83.82 | 18.13 | 65.69 | 3.01 | 23.10 | 2194.21 |
| STI0 | 21.85 | 9.27 | 12.58 | 3.25 | 11.12 | 1309.59 |

**Figure 10.** Trigger voltage/holding voltage distribution charts of HV nLDMOSs with drift-region modulation.
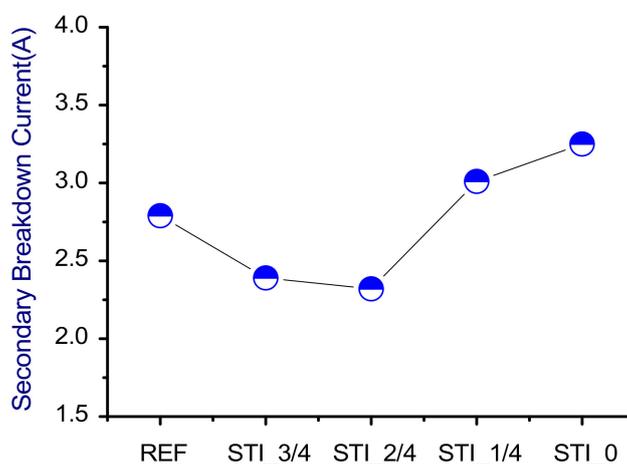


**Figure 11.** Secondary breakdown-current distribution chart of HV nLDMOSs with drift-region modulation.

*4.2. ESD Capability of HV nLDMOS DUTs with Channel-width Modulation*

Measurement results of HV nLDMOS devices with the channel-width modulation are shown in Figure 12 and Table 3. Meanwhile, the corresponding important physical-extracted parameters of snapback $V_{t1}/V_h$ and $I_{t2}$ data are shown in Figures 13 and 14. When the channel length (L) of the nLDMOS Reference device in this sub-section decreased as the H60PW layer shrunk, which was reduced from 3 μm of the Reference device in the previous sub-section to 2.75 μm. The lower channel resistance caused higher ESD surge current, which reduced the $I_{t2}$ value from 2.79 A to 2.5 A in this new HV nLDMOS Reference device. Furthermore, it can be found that by adjusting the finger number M = 2 and then total channel width is 150 μm of this nLDMOS (M2_W150) device, the $I_{t2}$ value has slightly decreased to 2.45 A as compared with the M = 4 and total channel width is 300 μm of the nLDMOS Reference (M4_W300) device. However, because of the HV nLDMOS DUT in M = 4 (M4_W300) has a serious non-uniform turned-on phenomenon by a multi-finger structure which is severely limited the capability of discharging ESD current. Next, by increasing the total channel width of M2_W150 from 150 μm to 300 μm which is named as the M2_W300. Then, the $I_{t2}$ value of M2_W300 can be greatly increased to 2.73 A. As the M2_W300 (M = 2) device compared with the same total channel width DUT of the M4_W300 (M = 4) device, the ESD capability of M2_W300 has indeed improved. In other words, the DUT of M4_W300 whose probability was higher on the first turned-on finger easily reached the failure point before others fingers of this MOSFET turned-on as compared with the

DUT of M2_W300. Moreover, in the FOM consideration, the M2_150 is best in this modulation being FOM= 4691.63 µA × V/µm². However, the designing of fingers number and channel-width manner in the circuit design are affected by the free space that the I/O cell area can be used. Therefore, how to improve the capability of non-uniform turned-on in a multi-finger structure for the HV nLDMOS device is a very important subject.
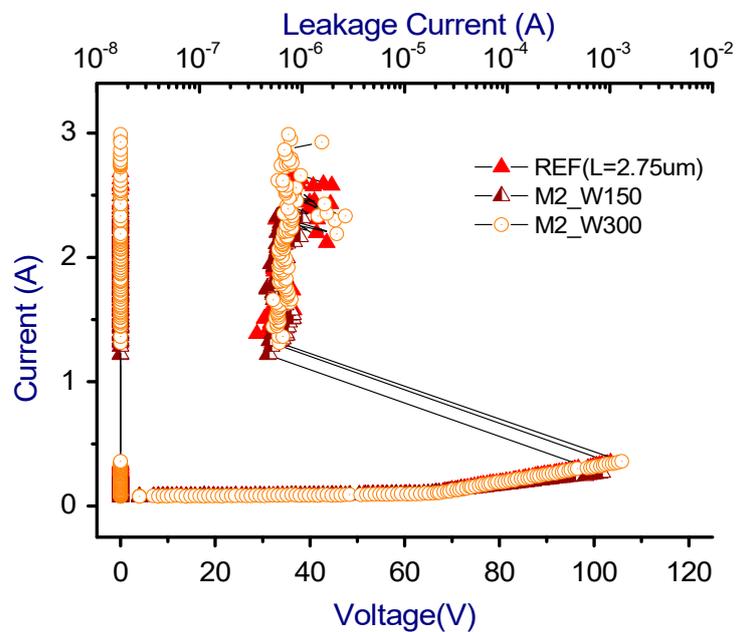


**Figure 12.** Snapback I-V curves and leakage currents of HV nLDMOSs with channel-width modulation.

**Table 3.** Snapback extracted parameters of HV nLDMOSs with channel-width modulation.

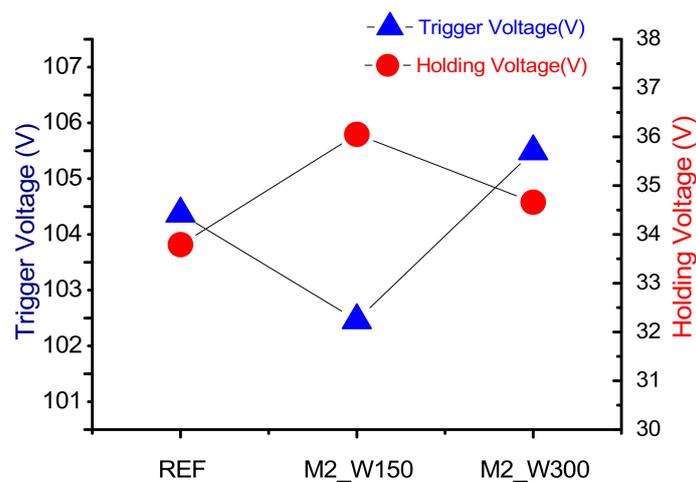| nLDMOS | $V_{t1}$ (V) | $V_h$ (V) | $I_{t2}$ (A) | FOM (µA × V/µm²) |
|---|---|---|---|---|
| Ref. (M4_W300, L = 2.75 µm) | 104.87 | 33.79 | 2.50 | 2836.95 |
| M2_W150 | 102.96 | 36.05 | 2.45 | 4691.93 |
| M2_W300 | 105.99 | 34.66 | 2.73 | 3257.45 |



**Figure 13.** Trigger voltage/holding voltage distribution charts of HV nLDMOSs with channel-width modulation.
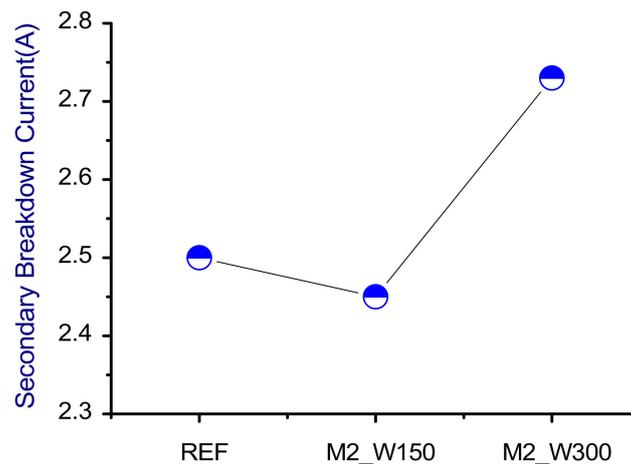
**Figure 14.** Secondary breakdown-current distribution chart of HV nLDMOSs with channel-width modulation.

### 4.3. ESD Capability of HV nLDMOS DUTs with Embedded SCR Modulation

Measurement data of HV nLDMOS devices with the embedded SCR modulation are presented in Figure 15 and Table 4. From Figure 5a,c and Figure 6a, it can be found that the SCRs (P$^+$ stripes) of the nLDMOS-SCR NPN and NPNPN-arranged types were embedded in the drain region far away from the gate, the parasitic BJT of LDMOS (N$^+$ stripe) was the first one to turn on when an ESD surge current entered. After the ESD surge voltage increased enough (as an ESD current passed through $R_{drain}$ and $R_{drift}$) to trigger these embedded SCRs, these components can partially discharge the ESD current through the parallel path of SCRs. As the characteristics of nLDMOS are more obvious, their $V_{t1}$ values will be higher. Of course, $V_h$ values of these components can maintain higher performance. However, in Figure 5b,d, and Figure 6b, if the SCRs (P$^+$ stripes) of an nLDMOS were embedded in the both side of drain region which are more nearer the poly-gate like the nLDMOS-SCR PNP and SCR PNPNP-arranged structures do, then they have higher ESD dissipation capability. When an ESD event occurred, these structures of nLDMOS-SCR PNP- and SCR PNPNP-arranged types just require lower voltage (as an ESD current passed through $R_{drift}$) to trigger SCRs under the conductive path, it is due to the P$^+$ zone in the drain side being closer the gate. It made the $V_{t1}$ values of these structures having the lower values of 103.66 V, and 103.98 V, respectively, as compared with others DUTs, which included the nLDMOS Reference device. In addition, because of they have notable SCR characteristics; the corresponding $V_h$ values will be decreased. Obviously, it can discharge larger ESD current by the path of embedded SCRs. Therefore, the $I_{t2}$ data have the best improvement from 2.5 A to 4.96 A and 4.44 A, respectively, for the nLDMOS-SCR PNP and PNPNP-arranged components. As for the nLDMOS-SCR PNP -arranged, it has a larger area of P$^+$ zone on the both side of drain, the FOM of this ESD protection device can be upgraded from 2831.83 $\mu A \times V/\mu m^2$ to 4255.51 $\mu A \times V/\mu m^2$ (50.27% improvement). Finally, the corresponding $V_{t1}$, $V_h$ and $I_{t2}$ values of the nLDMOS related devices by embedded different SCRs arrangements are shown in Figures 16 and 17.
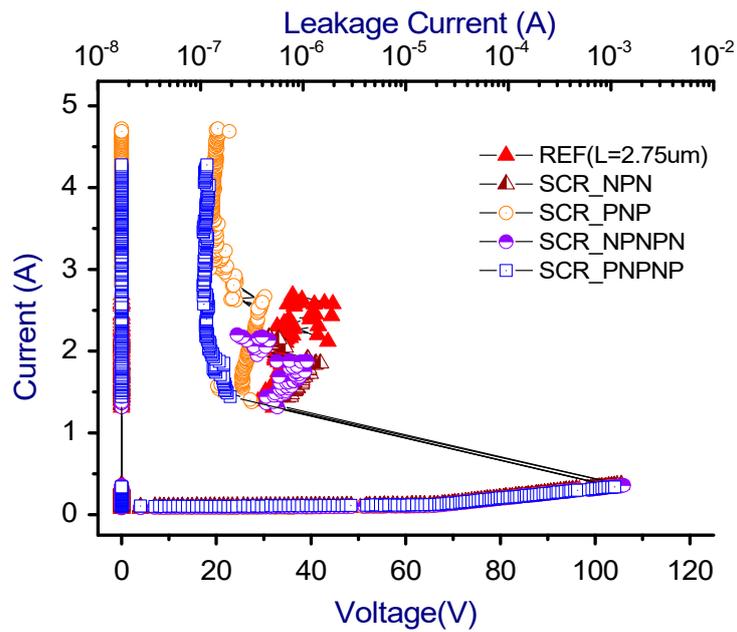
**Figure 15.** Snapback I-V curves and leakage currents of HV nLDMOSs with embedded SCR modulation.

**Table 4.** Snapback extracted parameters of HV nLDMOSs with embedded SCR modulation.

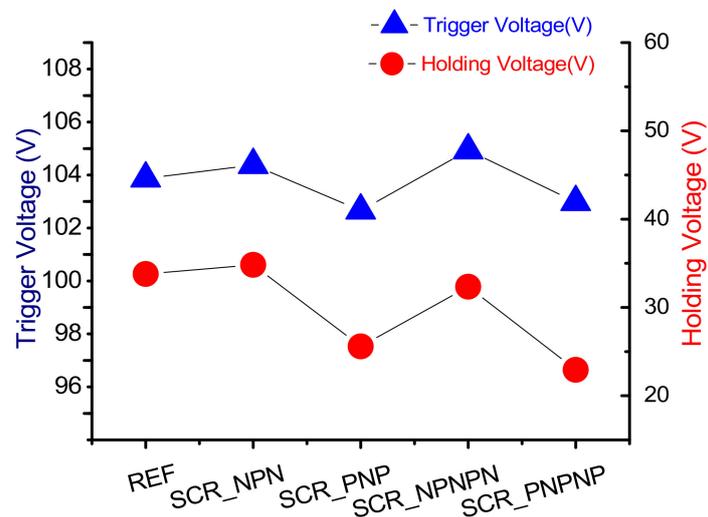| nLDMOS | $V_{t1}$ (V) | $V_h$ (V) | $I_{t2}$ (A) | FOM ($\mu A \times V/\mu m^2$) |
|---|---|---|---|---|
| REF (L = 2.75 $\mu$m) | 104.87 | 33.79 | 2.50 | 2831.83 |
| SCR_NPN | 105.38 | 34.83 | 2.22 | 2587.60 |
| SCR_PNP | 103.66 | 25.59 | 4.96 | 4255.51 |
| SCR_NPNPN | 105.93 | 32.35 | 2.22 | 2406.87 |
| SCR_PNPNP | 103.98 | 22.93 | 4.44 | 3410.64 |



**Figure 16.** Trigger voltage/holding voltage distribution charts of HV nLDMOSs with embedded SCR modulation.
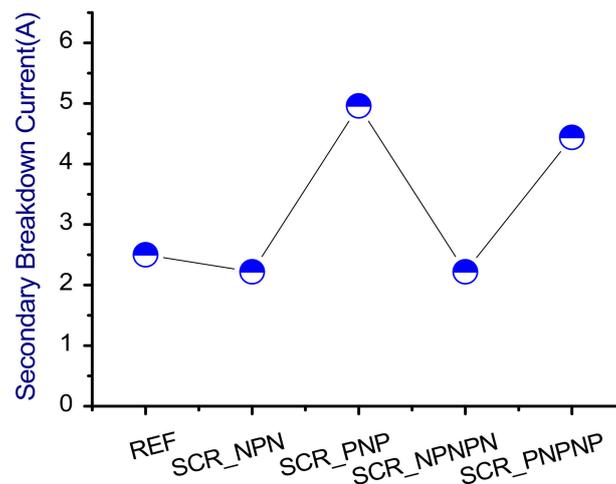
**Figure 17.** Secondary breakdown-current distribution chart of HV nLDMOSs with embedded SCR modulation.

### 4.4. ESD Capability of HV nLDMOS DUTs with Embedded Schottky-Diode Modulation

Measurement results of HV nLDMOS devices with the embedded Schottky-diode modulation are shown in Figure 18 and Table 5. The channel length L of this nLDMOS Reference device was set to be 2 μm, the $I_{t2}$ value of this Ref. device is significantly decreased to 2.29 A due to the channel-length reduction. However, the $I_{t2}$ level could be effectively promoted by adding an embedded Schottky diode in the drain side. In other words, after removing the entire heavily doped $N^+$ layer in the drain side, the $I_{t2}$ value of this device has higher performance than that of other DUTs. It is equivalent to serializing the Schottky diode in the drain end shown in Figure 8a, it has higher impedance when an ESD transient entered the drain electrode. Therefore, this new architecture made the $V_{t1}$ value therefore increasing to 109.43 V, and the $I_{t2}$ value of this device can be increased from 2.29 A for the Reference device (L = 2 μm) to 3.98 A (73.8% improvement). Meanwhile, the FOM value can be improved from 2400.38 μA/μm$^2$ to 4341.27 μA × V/μm$^2$ (80.86% improvement as compared with the Ref. device). Furthermore, it has a higher $V_h$ value as compared with the nLDMOS-SCR PNP-arranged type structure in the previous sub-section. Finally, the $V_{t1}$, $V_h$ and $I_{t2}$ distribution charts about the embedded Schottky-diode related components are shown Figures 19 and 20. These experimental results revealed that the $V_{t1}$ and $I_{t2}$ values have a decreasing trend when the area ratio of Schottky diode decreased (more like the original nLDMOS Reference device). To explain simply, if the area ratio of this parasitic Schottky diode is small, the characteristic of equivalent series Schottky diode will be not apparent (the $R_{drain}$ more higher shown in Figure 8b), which causes the $V_{t1}$ and $I_{t2}$ values, corresponding to these devices decreased accordingly. The relevant area ratio of embedded Schottky diode of this modulation can refer to Table 1. Overall, this new architecture (embedded a Schottky diode in the drain) has the most positive impact (80.86% ↑) on the FOM, compared with previous three techniques shown in Table 6.
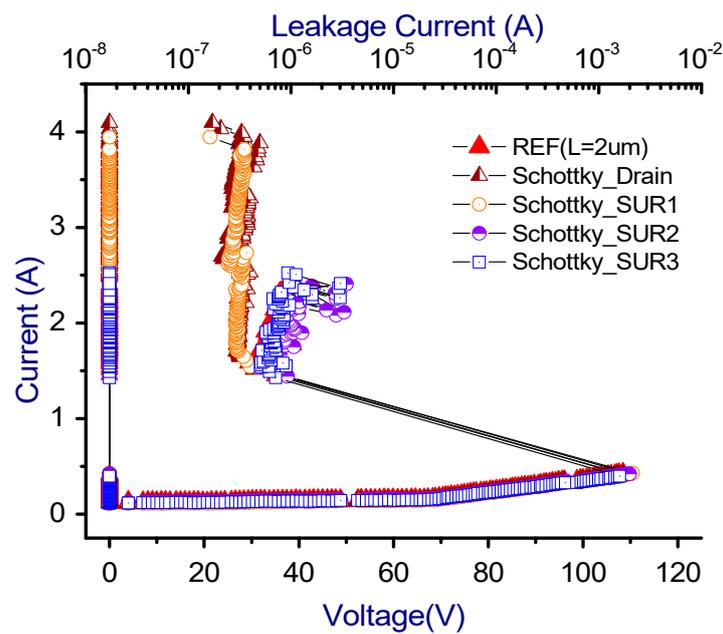
**Figure 18.** Snapback I-V curves and leakage currents of HV nLDMOSs with embedded Schottky-diode modulation.

**Table 5.** Snapback extracted parameters of HV nLDMOSs with embedded Schottky-diode modulation.

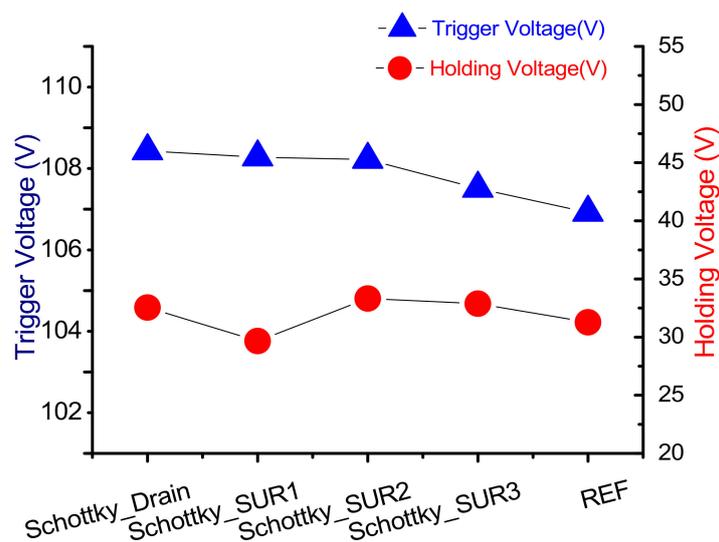| nLDMOS | $V_{t1}$ (V) | $V_h$ (V) | $I_{t2}$ (A) | FOM ($\mu A \times V/\mu m^2$) |
|---|---|---|---|---|
| Schottky_Drain | 109.43 | 32.54 | 3.98 | 4341.27 |
| Schottky_SUR1 | 109.28 | 29.66 | 3.75 | 3728.36 |
| Schottky_SUR2 | 109.22 | 33.32 | 2.40 | 2680.60 |
| Schottky_SUR3 | 108.51 | 32.88 | 2.34 | 2579.07 |
| Ref. (L = 2 $\mu$m) | 107.92 | 31.27 | 2.29 | 2400.38 |



**Figure 19.** Trigger voltage/holding voltage distribution charts of HV nLDMOSs with embedded Schottky-diode modulation.
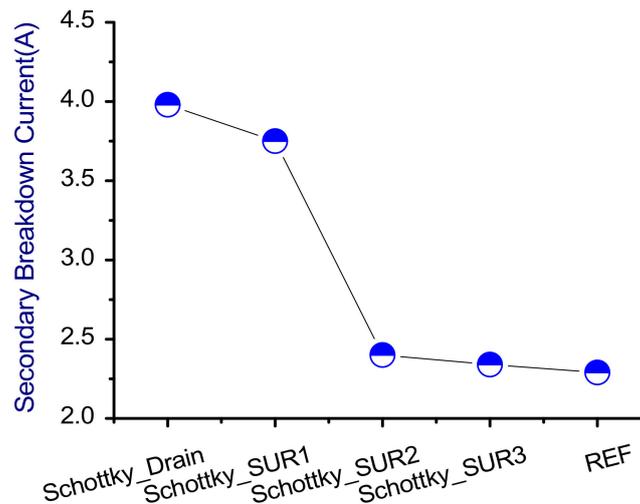
**Figure 20.** Secondary breakdown current distribution chart of HV nLDMOSs with embedded Schottky-diode modulation.

**Table 6.** A comparison of FOM improvement percentages for four ESD strengthening methods.

| Samples | FOM ($\mu A \times V/\mu m^2$) | Improvement |
| --- | --- | --- |
| Method-1: STI_3/4 | 3045.68 | 3.65% ↑ |
| Method-2: M2_W150 | 4691.93 | 65.39% ↑ |
| Method-3: SCR_PNP | 4255.51 | 50.27% ↑ |
| Method-4: Schottky_Drain | 4341.27 | 80.86% ↑ |

## 5. TCAD Simulation and Verification

For verification of ESD-reliability improvement by this novel embedded Schottky-diode in the LDMOS device drain side, the Silvaco EDA software was used to simulate a 2D total current density and lattice-temperature distributions with embedded Schottky-diode variations. Figures 21 and 22 are the diagrams of total current density and lattice temperature of these related devices at the drain-current $I_d = 1 \times 10^{-4}$ A injecting condition. From these diagrams, the high current density and lattice temperature are obviously concentrated near the drain side and below the STI region. In the Figures 21a and 22a, the structure of nLDMOS Reference device which had the highest current density and lattice temperature being $1.5 \times 10^{-3}$ (A/cm$^2$), and 693 (K), respectively. On the contrary, in the Figures 21b and 22b, the structure of removing entire drain-side heavily N$^+$ zone which has the maximum series resistance by embedded a 100% area of Schottky diode in drain side, then the total current density and lattice temperature could be reduced to $1.15 \times 10^{-3}$ (A/cm$^2$), and 684(K), respectively. It made this nLDMOS component can withstand higher ESD current (current density) and it is not easily concentrated to reach the melting point to damage. Finally, the Schottky_SUR1, Schottky_SUR2, and Schottky_SUR3 samples with different area ratios of embedded Schottky diode in the drain side are shown in Figures 21c–e and 22c–e. It can be found that an nLDMOS device would have higher current density and lattice temperature as with fewer Schottky-diode area ratio at the drain side. Therefore, it can be concluded that it is an easy and effective technique to increase the ESD withstanding capability for an HV nLDMOS with a drain-side embedded Schottky diode.
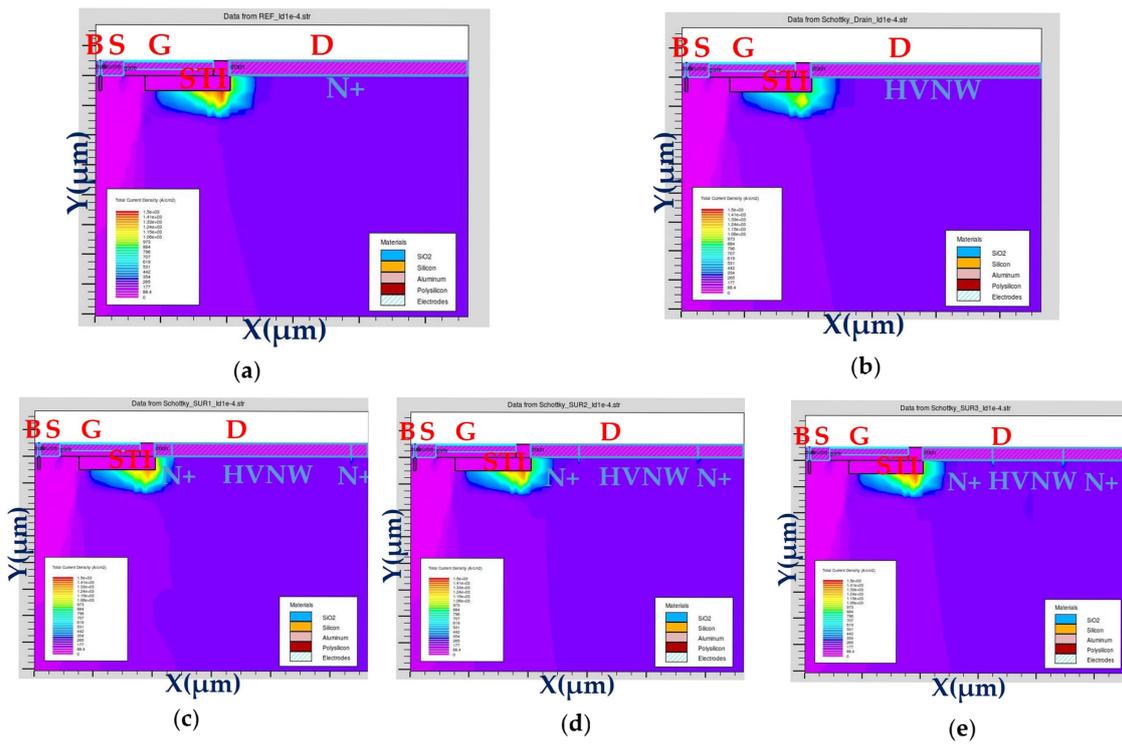
**Figure 21.** Total current-density diagrams of (**a**) Reference; (**b**) Schottky_Drain; (**c**) Schottky_SUR1; (**d**) Schottky_SUR2; and (**e**) Schottky_SUR3 at $I_d = 1 \times 10^{-4}$ A injection condition.



**Figure 22.** Lattice temperature diagrams of; (**a**) Reference; (**b**) Schottky_Drain; (**c**) Schottky_SUR1; (**d**) Schottky_SUR2; and (**e**) Schottky_SUR3 at $I_d = 1 \times 10^{-4}$ A injection condition.
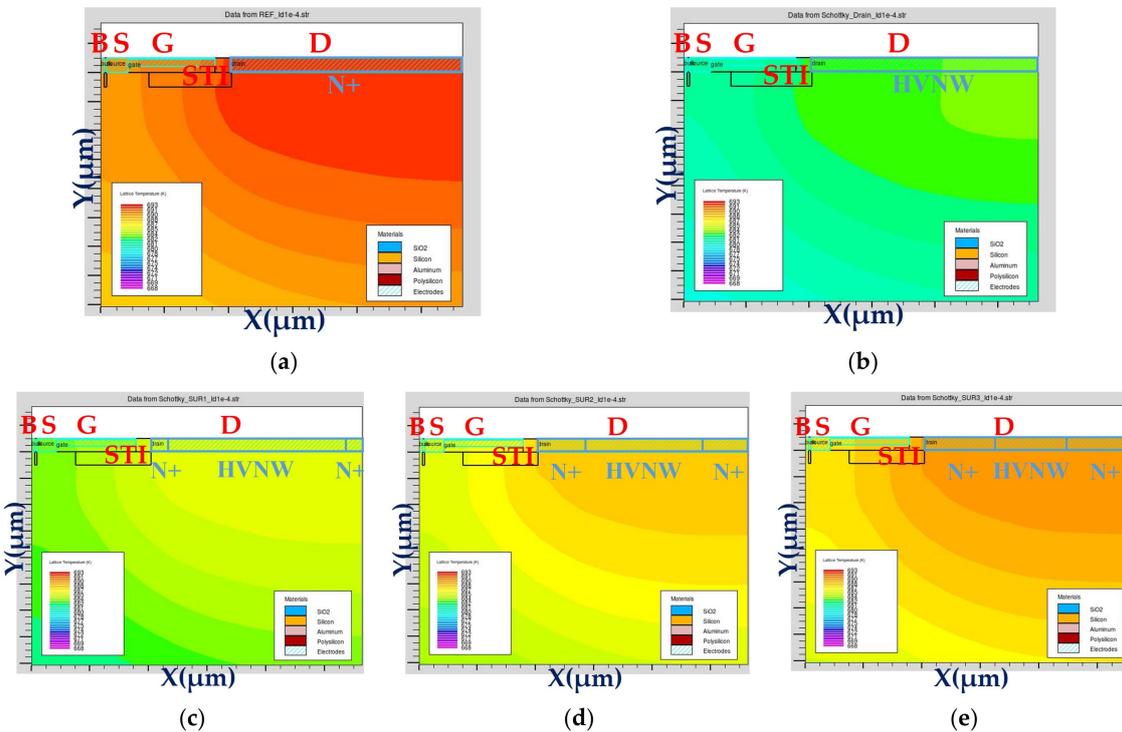
## 6. Conclusions

This research paper is divided into four parts focussed on promoting the ESD immunity of HV nLDMOS devices. The first part focuses on the effect of drift region modulation and the corresponding

ESD immunity of these related devices. As the length of the drift region decreased, the operating voltage directly decreased from reduced equivalent series resistance. Therefore, for the with the shortest distance (STI0), the $V_{t1}$ and $V_h$ values decreased from 104.47 V to 21.85 V and 32.53 V to 9.27 V from those of the nLDMOS Reference device, respectively. Then, protection devices were conveniently designed for high and low operating voltages in a single chip and improved the $I_{t2}$ value from 2.79 A to 3.25 A (and saved the layout area). The second part revealed that, for improved the ESD immunity per unit area of an HV LDMOS device, shortening the channel width and enlarging the finger number are not optimal strategies within the same layout area. An optimized channel width from fine adjustment is the best method for improvement of ESD immunity. In third part, to alleviate the problem of non-uniform turned-on of protection devices, the embedded SCR PNP-arranged type in the drain side had the highest ESD current discharge capability, and the FOM data was increased to 4255.51 $\mu A \times V/\mu m^2$; however, the $V_h$ value decreased to the low value of 25.59 V. Finally, by using an embedded Schottky-diode in the drain side to remove the entire heavy $N^+$-doped zone, the $I_{t2}$ value of this fully embedded Schottky diode in an HV nLDMOS device could be increased from 2.29 A to the largest 3.98 A. The FOM value improved significantly to 4341.27 $\mu A \times V/\mu m^2$, and the $V_h$ value stayed higher value (32.54 V) than did the embedded SCR PNP-arranged type. Therefore, improving ESD immunity capability (higher $I_{t2}$ value) requires consideration of LU reliability (higher $V_h$ vlaue) and saving the cell layout area (smaller cell area). An HV nLDMOS device embedded with a Schottky diode in the drain side is a favorable improvement strategy. A device with this architecture can consider ESD, LU, and cell-area saving. Therefore, the FOM significantly improved by approximately 80.86% over that of the nLDMOS Reference device.

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## Abbreviation

| Symbol | Meaning |
| --- | --- |
| BCD | Bipolar-Complementary metal-oxide-semiconductor-Double-diffused MOSFET |
| BJT | Bipolar-junction transistor |
| DUT | Device under test |
| ESD | Electrostatic discharge |
| FOM | Figure of merit |
| GGnMOS | Gate Grounded nMOSFET |
| HV nLDMOS | High voltage n-channel lateral diffused MOSFET |
| HBM | Human-body model |
| $I_{t2}$ | Secondary breakdown current |
| IC | Integrated circuit |
| IoT | Internet of things |
| LU | Latch-up |
| SCR | Silicon-controlled rectifier |
| STI | Shallow trench isolation |
| TLP | Transmission-line pulse system |
| $V_{bk}$ | Breakdown voltage |
| $V_h$ | Holding voltage |
| $V_{t1}$ | Trigger voltage |

## References

1. Lee, M.; Uhm, Y.; Kim, Y.; Kim, G.; Park, S. Intelligent power management device with middleware based living pattern learning for power reduction. *IEEE Trans. Consum. Electron.* **2009**, *55*, 2081–2089. [CrossRef]
2. Murphey, Y.; Park, J.; Kiliaris, L.; Kuang, M.; Masrur, M.; Phillips, A.; Wang, Q. Intelligent Hybrid Vehicle Power Control—Part II: Online Intelligent Energy Management. *IEEE Trans. Veh. Technol.* **2013**, *62*, 69–79. [CrossRef]
3. Vidya, V.; Dharmana, M. Model reference based intelligent control of an active suspension system for vehicles. In Proceedings of the International Conference on Circuit, Power and Computing Technologies, Kollam, India, 20–21 April 2017; pp. 1–5.
4. Yang, L. Research on Design of Weak Current Protection Circuit in Intelligent Home Control Circuit under the Background of Internet of Things. In Proceedings of the International Conference on Mechanical, Control and Computer Engineering, Huhhot, China, 14–16 September 2018; pp. 189–191.
5. Yi, D.; Su, J.; Liu, C.; Chen, W. Trajectory Clustering Aided Personalized Driver Intention Prediction for Intelligent Vehicles. *IEEE Trans. Ind. Inf.* **2019**, *15*, 3693–3702. [CrossRef]
6. Vdovic, H.; Babic, J.; Podobnik, V. Automotive Software in Connected and Autonomous Electric Vehicles: A Review. *IEEE Access* **2019**, *7*, 166365–166379. [CrossRef]
7. Zhongzheng, T.; Yangzi, S.; Silong, W. Design of Power Production Safety Monitoring System Based on Intelligent Internet of Things. In Proceedings of the International Conference on Smart Grid and Electrical Automation, Xiangtan, China, 10–11 August 2019; pp. 73–77.
8. Lu, T.; Chen, X.; Bai, W. Research on environmental monitoring and control technology based on intelligent Internet of Things perception. *J. Eng.* **2019**, *23*, 8946–8950. [CrossRef]
9. Sun, Z.; Xing, X.; Wang, T.; Lv, Z.; Yan, B. An Optimized Clustering Communication Protocol Based on Intelligent Computing in Information-Centric Internet of Things. *IEEE Access* **2019**, *7*, 28238–28249. [CrossRef]
10. Zhang, Y.; Pendharkar, S.; Hower, P.; Giombanco, S.; Amoroso, A.; Marino, F. A RESURF P-N bimodal LDMOS suitable for high voltage power switching applications. In Proceedings of the International Symposium on Power Semiconductor Devices & IC's, Hong Kong, China, 10–14 May 2015; pp. 61–64.
11. Kojima, J.; Matsuda, J.; Kamiyama, M.; Tsukiji, N.; Kobayashi, H. Optimization and analysis of high reliability 30–50 V dual RESURF LDMOS. In Proceedings of the International Conference on Solid-State and Integrated Circuit Technology, Hangzhou, China, 25–28 October 2016; pp. 1–3.
12. Matsuda, J.; Kuwana, A.; Kojima, J.; Tsukiji, N.; Kobayashi, H. Wide SOA and High Reliability 60–100 V LDMOS Transistors with Low Switching Loss and Low Specific On-Resistance. In Proceedings of the International Conference on Solid-State and Integrated Circuit Technology, Qingdao, China, 31 October–3 November 2018; pp. 1–3.
13. Zhang, G.; Zhang, W.; He, J.; Zhu, X.; Zhang, S.; Zhao, J.; Zhang, Z.; Qiao, M.; Zhou, X.; Li, Z.; et al. Experiments of a Novel low on-resistance LDMOS with 3-D Floating Vertical Field Plate. In Proceedings of the International Symposium on Power Semiconductor Devices and ICs, Shanghai, China, 19–23 May 2019; pp. 507–510.
14. Guo, S.; Chen, X. A Novel p-LDMOS Additionally Conducting Electrons by Control ICs. *IEEE J. Electron Devices Soc.* **2019**, *7*, 710–716. [CrossRef]
15. Bhoir, M.; Kaushal, K.; Panda, S.; Singh, A.; Jatana, H.; Mohapatra, N. Source Underlap—A Novel Technique to Improve Safe Operating Area and Output-Conductance in LDMOS Transistors. *IEEE Trans. Electron Devices* **2019**, *66*, 4823–4828. [CrossRef]
16. Wei, Y.; Luo, X.; Ge, W.; Zhao, Z.; Ma, Z.; Wei, J. A Split Triple-Gate Power LDMOS with Improved Static-State and Switching Performance. *IEEE Trans. Electron Devices* **2019**, *66*, 2669–2674. [CrossRef]
17. Duvvury, C.; Carvajal, F.; Jones, C.; Briggs, D. Lateral DMOS design for ESD robustness. In Proceedings of the International Electron Devices Meeting. IEDM Technical Digest, Washington, DC, USA, 10–10 December 1997; pp. 1–4.
18. Kawamoto, K.; Takahashi, S.; Fujino, S.; Shirakawa, I. A no-snapback LDMOSFET with automotive ESD endurance. *IEEE Trans. Electron Devices* **2002**, *49*, 2047–2053. [CrossRef]
19. Wang, C.; Ker, M. ESD Protection Design with Lateral DMOS Transistor in 40-V BCD Technology. *IEEE Trans. Electron Devices* **2010**, *57*, 3395–3404. [CrossRef]

20. Chen, W.; Ker, M. New Layout Arrangement to Improve ESD Robustness of Large-Array High-Voltage nLDMOS. *IEEE Electron Device Lett.* **2010**, *31*, 159–161. [CrossRef]

21. Chen, W.; Ker, M. Improving Safe Operating Area of nLDMOS Array With Embedded Silicon Controlled Rectifier for ESD Protection in a 24-V BCD Process. *IEEE Trans. Electron Devices* **2011**, *58*, 2944–2951. [CrossRef]

22. Malobabic, S.; Salcedo, J.; Hajjar, J.; Liou, J. NLDMOS ESD Scaling Under Human Metal Model for 40-V Mixed-Signal Applications. *IEEE Electron Device Lett.* **2012**, *33*, 1595–1597. [CrossRef]

23. Ye, R.; Liu, S.; Sun, W.; Su, W.; Lin, F.; Sun, G.; Lin, Z. ESD failure mechanism and optimiztion for the LDMOS with low on-resistance and large geometric array used as output device. In Proceedings of the International Symposium on Power Semiconductor Devices and ICs, Prague, Czech Republic, 12–16 June 2016; pp. 239–242.

24. Chen, S.; Lee, M. Reliability Analysis of P+ Pickup on Anti-ESD Performance in Four CMOS Low-voltage Technology Nodes. *IETE J. Res.* **2016**, *62*, 752–761. [CrossRef]

25. Kumar, B.; Shrivastava, M. Part II: RF, ESD, HCI, SOA, and Self Heating Concerns in LDMOS Devices Versus Quasi-Saturation. *IEEE Trans. Electron Devices* **2018**, *65*, 199–206. [CrossRef]

26. Lee, J.; Prabhu, M.; Natarajan, M. Engineering ESD Robust LDMOS SCR Devices in FinFET Technology. *IEEE Electron Device Lett.* **2018**, *39*, 1011–1013. [CrossRef]

27. Kranthi, N.; Kumar, B.; Salman, A.; Boselli, G.; Shrivastava, M. Physical Insights into the Low Current ESD Failure of LDMOS-SCR and its Implication on Power Scalability. In Proceedings of the International Reliability Physics Symposium, Monterey, CA, USA, 31 March–4 April 2019; pp. 1–5.

28. Jin, X.; Wang, Y.; Zhong, Z. Optimization of LDMOS-SCR Device for ESD Protection Based On 0.5 μm CMOS Process. In Proceedings of the International Workshop on the Electromagnetic Compatibility of Integrated Circuits, Hangzhou, China, 21–23 October 2019; pp. 195–197.

29. Oh, K.; Duvvury, C.; Salling, C.; Banerjee, K.; Dutton, R. Non-uniform bipolar conduction in single finger NMOS transistors and implications for deep submicron ESD design. In Proceedings of the International Reliability Physics Symposium Proceedings, Orlando, FL, USA, 30 April–3 May 2001; pp. 226–234.

30. Oh, K.; Banerjee, K.; Duvvury, C.; Dutton, R. Non-uniform conduction induced reverse channel length dependence of ESD reliability for silicided NMOS transistors. In Proceedings of the International Electron Devices Meeting, San Francisco, CA, USA, USA, 8–11 December 2002; pp. 341–344.

31. Ker, M.; Chen, J. Self-Substrate-Triggered Technique to Enhance Turn-On Uniformity of Multi-Finger ESD Protection Devices. *IEEE J. Solid-State Circuits* **2006**, *41*, 2601–2609. [CrossRef]

32. Ker, M.; Hsu, K. Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits. *IEEE Trans. Device Mater. Reliab.* **2005**, *5*, 235–249.

33. Liang, H.; Gu, X.; Dong, S.; Liou, J. RC-Embedded LDMOS-SCR with High Holding Current for High-Voltage I/O ESD Protection. *IEEE Trans. Device Mater. Reliab.* **2015**, *15*, 495–499. [CrossRef]

34. Do, K.; Woo, J.; Koo, Y.; Lee, K. A Study of Dual-Directional SCR with Low Dynamic Resistance and High Holding Voltage for Low-Voltage Application. In Proceedings of the International Conference on Electrical Engineering and Photonics, San Francisco, St. Petersburg, Russia, 17–18 October 2019; pp. 5–8.

35. Guan, J.; Wang, Y.; Hao, S.; Zheng, Y.; Jin, X. A Novel High Holding Voltage Dual-Direction SCR with Embedded Structure for HV ESD Protection. *IEEE Electron Device Lett.* **2017**, *38*, 1716–1719. [CrossRef]

36. Huang, C.; Chiu, F.; Ou, C.; Chen, Q.; Huang, Y.; Tseng, J. ESD and Latchup Optimization of an Embedded-Floating-pMOS SCR-Incorporated BJT. *IEEE Trans. Electron Devices* **2016**, *63*, 3036–3043.