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High-Speed Wide-Range True-Single-Phase-Clock CMOS Dual Modulus Prescaler

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Abstract: This manuscript presents two novel low-power high-speed true-single-phase-clock (TSPC) prescalers with division ratios of 2/3 and 4/5, respectively, in a standard 90-nm CMOS technology. The logic gates incorporated between the D-flip-flops (DFFs) of a conventional 2/3 prescaler are modified to reduce the propagation delay and hence increase the maximum operating frequency. The measurement results show that the proposed divide-by-2/3 and divide-by-4/5 prescalers can operate up to 17 GHz and 15.3 GHz, respectively, which increase by 5.4 GHz and 4.3 GHz compared with conventional TSPC prescalers. The power of the proposed divide-by-2/3 prescaler is 0.67 mW and 0.92 mW, and 0.87 mW and 1.06 mW for the proposed divide-by-4/5 prescaler. The chip occupies an area of 20×35 μm^2 and 20×50 μm^2 for the proposed divide-by-2/3 and divide-by-4/5 prescalers.

Keywords: CMOS; frequency divider; high speed; prescaler; propagation delay; true-single-phase-clock (TSPC)

1. Introduction

The frequency synthesizer plays an important role in CMOS radio-frequency (RF) and millimeter-wave (MMW) applications [1,2]. The high speed dual-modulus frequency prescaler is one of the key blocks in the design of pulse swallow frequency dividers in frequency synthesizers [3,4], since it can achieve multiple division ratios. Operating frequency, power consumption and circuit complexity are usually the main design considerations.

Several types of prescalers have been discussed in previous works. Current mode logic (CML) topology can realize a higher operating frequency while consuming higher power. True-single-phase-clock (TSPC) dividers [5] and prescalers are usually consisted of several stages of TSPC logic gates, which have single-phase clock-controlled latches. Compared to the CML structure, TSPC topology suffers from a relatively lower operating frequency, but benefits from a lower power consumption and smaller area [5–11]. In addition, the TSPC technique exhibits lower phase noise due to the fewer transistors and faster transitions [12]. The extended-TSPC (E-TSPC) topology has a higher speed than the TSPC topology, since it has one less transistor of each stage, and it is widely studied and optimized [13–16]. However, the power consumption of E-TSPC blocks is largely affected by the amplitude and DC level of the input clock signal, which have little influence on the TSPC blocks. Besides, E-TSPC architecture has a higher short circuit power than TSPC structures [17]. Moreover, since the NMOS and PMOS transistors may turn on simultaneously, the E-TSPC structure can cause the wrong state in the following stages [5]. Therefore, TSPC prescalers with extended operating frequency are a better choice, which are widely studied [6,17–24] and applied [2,25] for low power applications.

A TSPC dual-modulus prescaler generally consists of several stages of TSPC D-flip-flops (DFFs) and other logic gates to realize two division ratios. There are many ways to enhance the operating frequency range, such as DFF optimizing [26–29] and logic-gate embedding [17]. In order to achieve the

highest possible speed using the traditional TSPC DFF, this work mainly focuses on logic modification to reduce the total propagation delay. In addition, logic gates are embedded as well.

This manuscript presents a new structure of a TSPC divide-by-2/3 prescaler and divide-by-4/5 prescaler in a 90-nm CMOS technology. Section 2 describes the circuit design of the proposed prescalers. The measurement results are discussed in Section 3. Finally, a conclusion is provided in Section 4.

2. Circuit Design

Figure 1 shows the topology and gate level circuit schematic of the conventional divide-by-2/3 prescaler, which consists of two stages of DFFs, an AND gate and an OR gate. MC (modulus control signal) is used for the divider modulus control. The logic gates incorporated between the DFFs introduce an extra time delay, which limits the operating frequency of the conventional divide-by-2/3 prescaler.

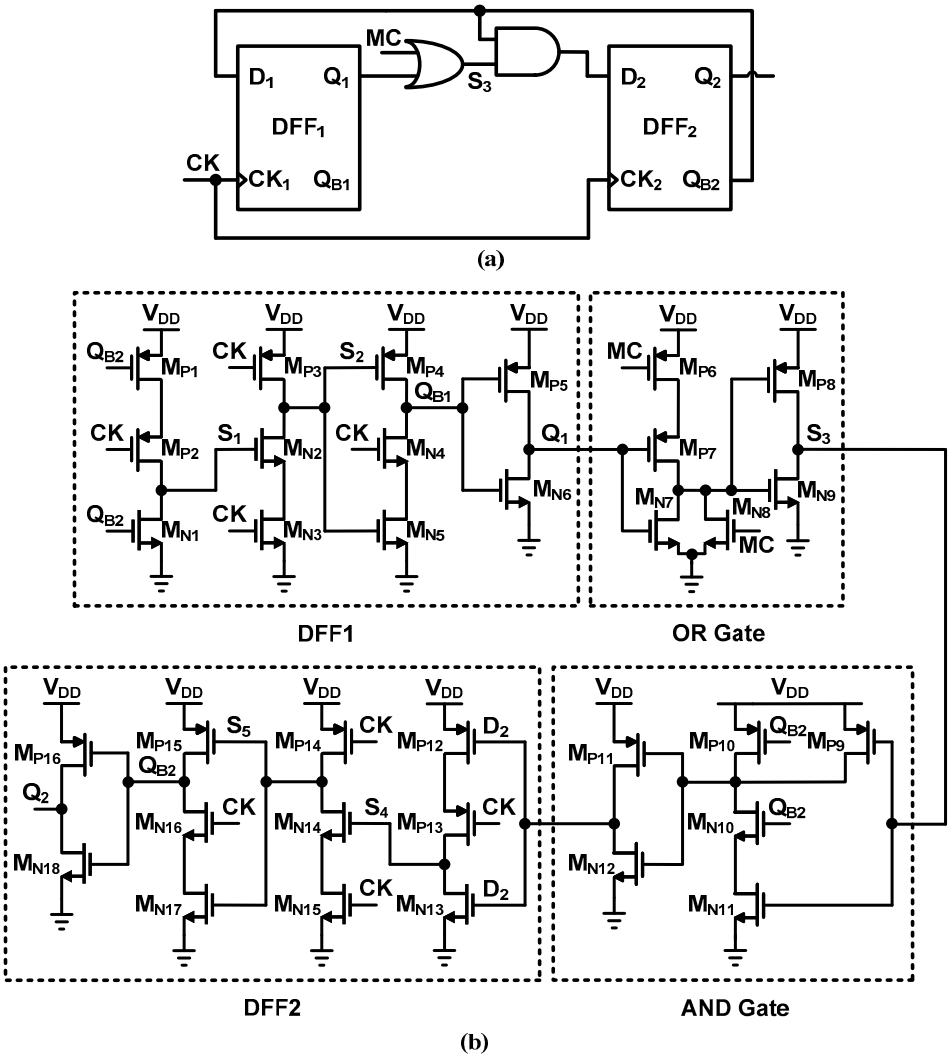

Figure 1. (**a**) Block diagram and (**b**) schematic of the conventional true-single-phase-clock (TSPC) divide-by-2/3 prescaler.

The block diagram and schematic of the proposed TSPC divide-by-2/3 prescaler is shown in Figure 2a,b, respectively, which consists of two stages of DFF and two stages of NAND gates. When MC_1 is logically low, the 2/3 prescaler operates in the divide-by-2 mode, whereas the 2/3 prescaler operates in the divide-by-3 mode when MC_1 is logically high. The advantages of the proposed prescaler can be better understood by comparing the signal path between nodes Q_{B1} and S_4 in Figures 1b and 2b. Specifically, two inverters (i.e., inverters consisted of M_{P5}&M_{N6} and M_{P8}&M_{N9} in Figure 1b) are

eliminated from Q_{B1} to S_3 by replacing the OR gate in the conventional topology with the NAND gate in the proposed structure, which helps to reduce the propagation delay of the clock signal and hence boost the maximum operating frequency. In addition, another two inverters (i.e., inverters made of M_{P11}&M_{N12} and M_{P12}&M_{N13} in Figure 1b) are saved from S_3 to S_4 in Figure 2b, owing to the co-design of the second NAND gate with the first TSPC gate of DFF_2, which further decreases the path delay and increases the operating frequency. As a result, when the proposed prescaler operates under the divide-by-2 mode, S_3 is kept high and the prescaler is configured just the same as a fixed-modulus divide-by-2 divider. In other words, it achieves the highest possible speed using the same DFF, since there is no extra delay from the logic gate. As for the divide-by-3 mode, the total propagation delay is reduced by that of four inverters, thereby greatly increasing the maximum operating frequency of the prescaler.

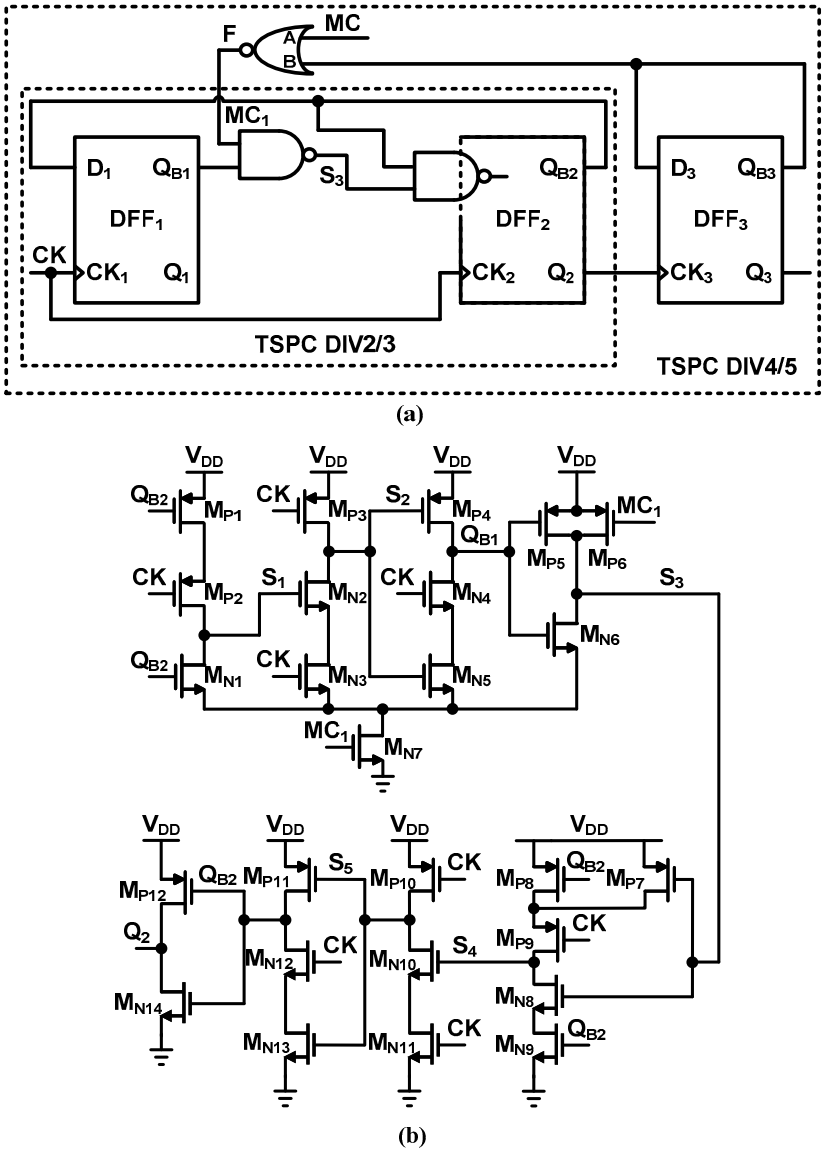

Figure 2. (**a**) Block diagram of the proposed divide-by-2/3 and divide-by-4/5 prescalers, (**b**) schematic of the proposed divide-by-2/3 prescaler.

In addition, the transistor M_{N7} is controlled by the MC_1 signal. When the prescaler operates in the divide-by-2 mode, the first DFF stage and NAND logic are shielded, so that the current through this stage will be turned off, thereby reducing the static power consumption of the prescaler.

The static power consumptions for the divide-by-2 mode and divide-by-3 mode are 217 μW and 436 μW, respectively.

The simulated waveforms of the internal nodes for the conventional and designed divide-by-2/3 prescalers under the divide-by-3 mode are shown in Figure 3. When the input frequency exceeds the maximum operating frequency, signal D_2 in Figure 1 is delayed into the next clock period due to the large delay of the OR and AND gates, resulting in a false logic high level of S_4. Under such a circumstance, S_5 will drop below the threshold voltage ($V_{DD}/2$) when the clock is low, causing a false level for Q_{B2}, as shown in Figure 3a. The waveforms of the conventional and designed structures are compared in Figure 3b, where the operating frequency is slightly below the maximum operating frequency of the conventional prescaler, to make sure that both structures work correctly. Thanks to the proposed new structure, the delay time from Q_{B1} to S_3 and from S_3 to S_4 is greatly reduced. Therefore, the maximum operating frequency of the proposed prescaler is much higher than the conventional one.

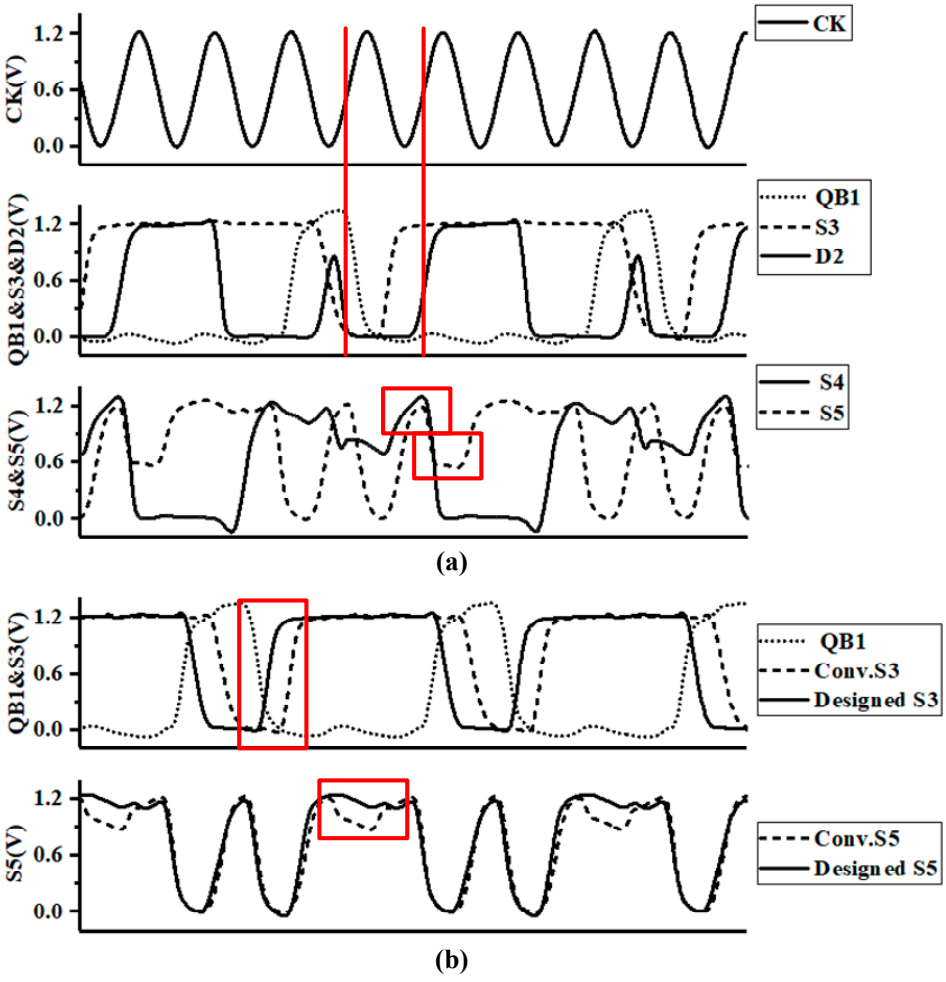

Figure 3. (**a**) Simulated waveforms of the conventional divide-by-2/3 prescaler beyond the maximum operating frequency, (**b**) comparisons of the simulated waveforms of the conventional and designed divide-by-2/3 prescalers.

Figure 2a also shows the block diagram of the proposed divide-by-4/5 prescaler by adopting the proposed divide-by-2/3 prescaler, a NOR logic and a fixed-modulus TSPC divide-by-2 divider. When the MC is logically low, the prescaler operates in the divide-by-5 mode, while the prescaler operates in the divide-by-4 mode if the MC is logically high. The positive output Q_2 of the second stage is used as the input clock signal of the TSPC divide-by-2 divider. The modulus control signal of the

2/3 prescaler MC_1 is generated by the negative output (Q_{B3}) of the divide-by-2 divider and modulus control signal of the MC through the NOR logic.

Corner simulations are preformed to further show the improvement of the proposed structure. The waveforms of some key nodes are simulated and analyzed under the same operating frequency as Figure 3b. The corner simulations of process, voltage and temperature (PVT) of node Q_{B2} for the divide-by-3 mode are shown in Figure 4. For the conventional structure, the output is incorrect under the worst case, while the proposed prescaler can work correctly. The process variation simulations for the divide-by-3 mode of node Q_{B2} are shown in Figure 5. For the conventional structure, the output is incorrect when the transistors are under a slow mode, while the temperature and supply voltage remain the same. The corner simulation waveform of node Q_{B1}, S_3 and S_5 of the proposed prescaler under divide-by-3 are shown in Figure 6. Compared with Figure 3b, there is no false level around the threshold voltage (in the red box) under each corner of the proposed prescaler. Therefore, the proposed structure is more PVT robust.

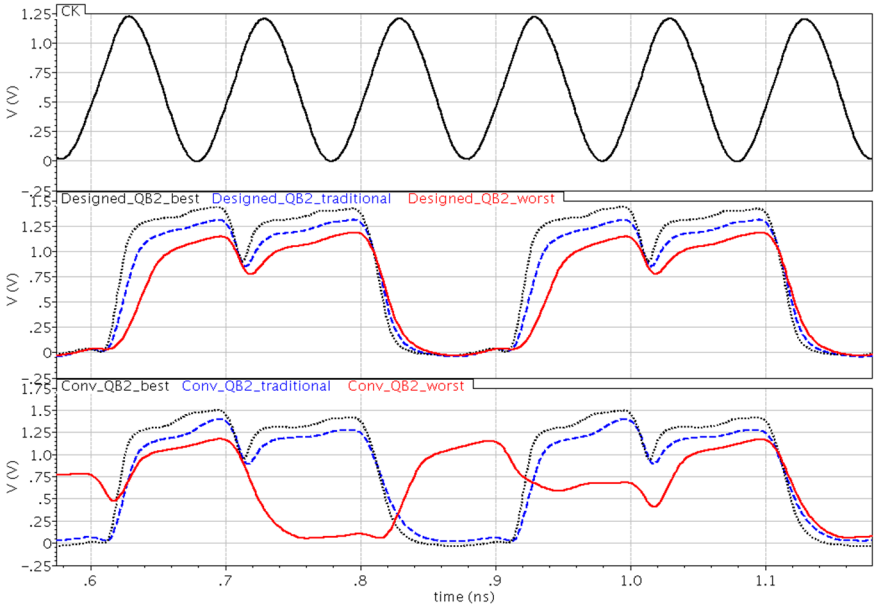

Figure 4. Corner simulation waveform of node Q_{B2} under divide-by-3 (Best case: ff, 1.1VDD, −45 °C; Traditional case: tt, VDD, 50 °C; Worst case: ss, 0.9VDD, 125 °C.).

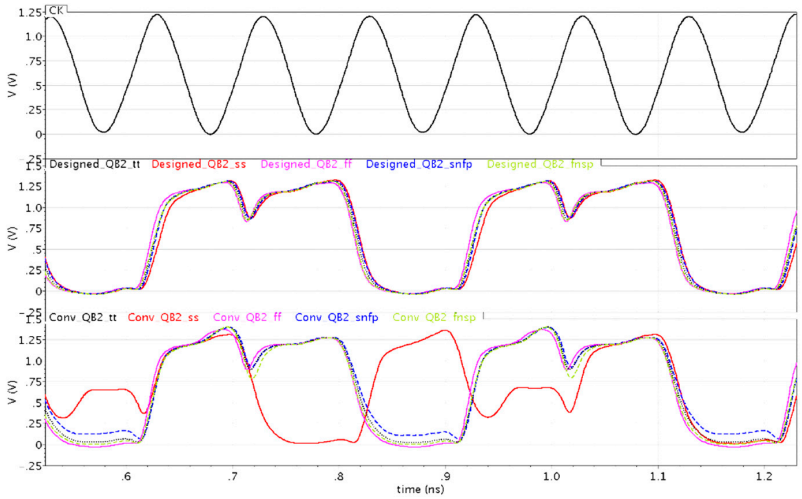

Figure 5. Corner simulation waveform of node Q_{B2} under divide-by-3 (Only process variation: tt, ss, ff, snfp, fnsp).

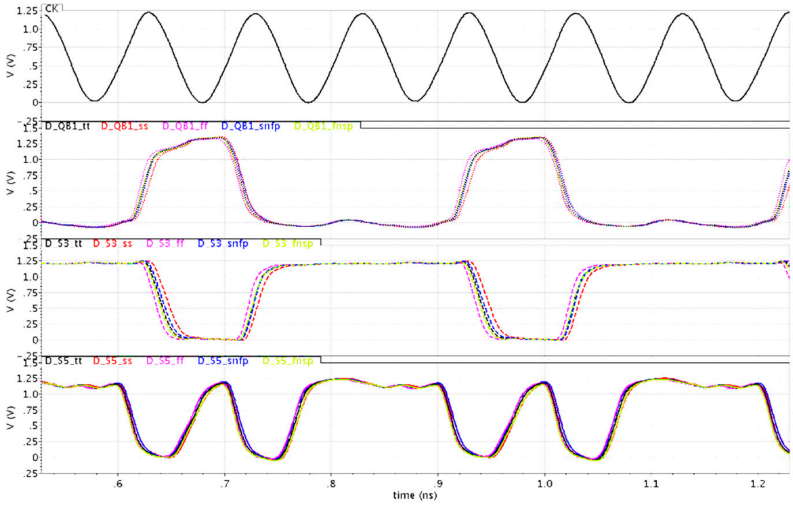

Figure 6. Corner simulation waveform of the proposed prescaler under divide-by-3 (Only process variation: tt, ss, ff, snfp, fnsp).

3. Measurement Results and Discussion

The proposed divide-by-2/3 and divide-by-4/5 prescalers are designed and fabricated in a 90-nm CMOS technology. The conventional prescalers are also fabricated for comparison. Figure 7 shows the chip microphotograph, which includes a prescaler core, a fixed divider chain and DC pads for the power supply and modulus control. As shown in Figure 7b, for each prescaler, two 100-Ω resistors are used for the input biasing as well as input impedance, roughly matching to 50-Ω. In order to alleviate the influence of parasitic capacitance from the bonding pads on the output signal, a fixed divider chain is applied after the prescaler core to lower the output frequency by a factor of 64 for the divide-by-2/3 prescaler and a factor of 32 for the divide-by-4/5 prescaler. The cores of the divide-by-2/3 and divide-by-4/5 prescalers occupy a chip area of 20 × 35 μm^2 and 20 × 50 μm^2, respectively. The measurements are carried out on an RF probe station, where the input signal is provided by the Agilent E8257D analog signal generator, and the output signals are measured using the Keysight N9030B signal analyzer.

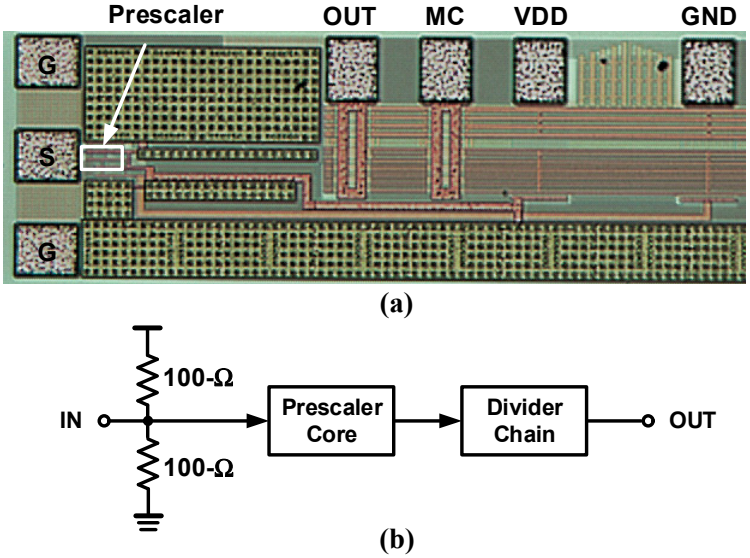

Figure 7. (**a**) Die micrograph of the fabricated prescalers, including a prescaler core, a fixed divider chain and DC pads for the power supply and modulus control; (**b**) Test structure.

The measured input sensitivity curves of the divide-by-2/3 and divide-by-4/5 prescalers are compared with the conventional TSPCs, as shown in Figures 8 and 9, respectively. It can be seen from Figure 8 that the maximum operating frequency for the conventional divide-by-2/3 prescaler is 11.6 GHz for the divide-by-2 mode and 7.8 GHz for the divide-by-3 mode, respectively, which has been increased to 17 GHz and 15.9 GHz by utilizing the proposed structure. Furthermore, the maximum operating frequency of the proposed divide-by-4/5 prescaler also extends from 11 GHz to 15.3 GHz for the divide-by-4 mode and from 7.7 GHz to 14.2 GHz for the divide-by-5 mode, respectively.

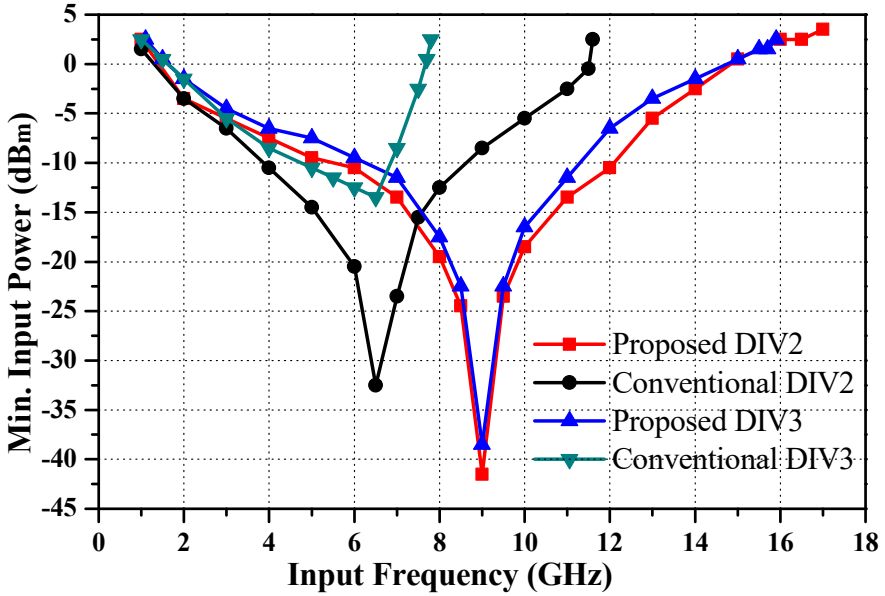

Figure 8. Measured input sensitivity curves of the conventional and proposed divide-by-2/3 prescalers.

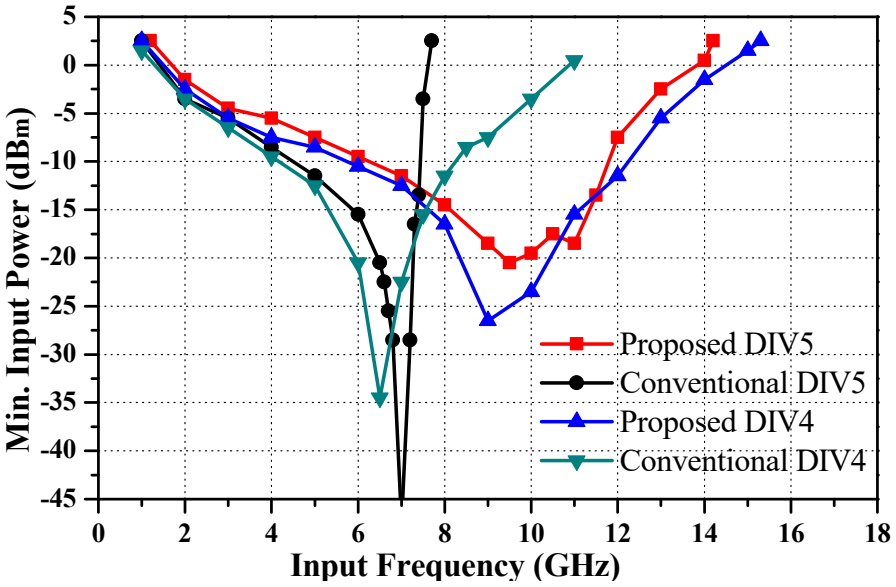

Figure 9. Measured input sensitivity curves of the conventional and proposed divide-by-4/5 prescalers.

Table 1 summarizes the performance of this work and compares with the other state-of-the-art CMOS TSPC prescalers. As is shown in the table, the proposed design achieves a higher operating frequency, a wider frequency range and a considerable power consumption, which is suitable for modern communication systems.

Table 1. Comparison with previous works.

Design	Process	Division Ratio	Freq. Range (GHz)	Power (mW) *	Chip Area (μm^2)
[19]	180 nm	6/7/8	0.2–4.2	0.81 **	35 × 40
[20]	180 nm	16/17	0.002–5.8	2.2	40 × 80
[21]	130 nm	2/3	14.1	0.8/1.1	-
[22]	65 nm	2/3 4/5	17 ***	0.318 0.938	-
[23]	180 nm	2/3	0.7–5.7	0.95	30 × 40
[30]	22 nm	/4, /8	10–64	2.2 **	154
This work	90 nm	2/3	1–17/ 1.1–15.9	0.67/0.92	20 × 35
This work	90 nm	4/5	1–15.3/ 1.2–14.2	0.87/1.06	20 × 50

* Measured at 5 GHz. ** Measured at maximum power consumption. *** Only maximum operating frequency.

Many works have been published concerning the improvement of TSPC DFFs [26–29] and single-phase clocked (SPC) DFFs [31] in recent years. The aim of work is to achieve the highest possible speed using the traditional TSPC DFF under the divide-by-2 mode, as there is no extra delay from the logic gate. Furthermore, the total propagation delay is reduced by that of four inverters as for the divide-by-3 mode.

Some references are about the design, optimization [13–16] and application [32,33] of the E-TSPC structure, while our paper focuses on the improvement of TSPC prescalers. Reference [33] combines the E-TSPC and TSPC structures. Compared with the E-TSPC topology, the amplitude and DC level of the input clock signal will have little influence on the power consumption of TSPC blocks, which are more PVT-robust. Therefore, our goal is to investigate TSPC prescalers with an extended operating frequency.

4. Conclusions

Two low-power high-speed TSPC divide-by-2/3 and divide by-4/5 prescalers are designed and implemented in a 90-nm CMOS technology. The logic gates incorporated between the DFFs of the conventional 2/3 prescaler are modified in order to reduce the extra propagation delay and increase the operating frequency. The proposed divide-by-2/3 and divide-by-4/5 prescalers can operate from 1 GHz to 17 GHz, and 1 GHz to 15.3 GHz, respectively, which can be used for the design of frequency synthesizers. The power of the proposed divide-by-2/3 prescaler is 0.67 mW and 0.92 mW, and 0.87 mW and 1.06 mW for the proposed divide-by-4/5 prescaler. The chip occupies an area of 20 × 35 μm^2 and 20 × 50 μm^2 for the proposed divide-by-2/3 and divide-by-4/5 prescalers, which is promising in the low-power and small-area design tendency.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. El-Halwagy, W.; Nag, A.; Hisayasu, P.; Aryanfar, F.; Mousavi, P.; Hossain, M. A 28-GHz Quadrature Fractional-N Frequency Synthesizer for 5G Transceivers with Less Than 100-fs Jitter Based on Cascaded PLL Architecture. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 396–413. [CrossRef]
2. Kim, N.; Rabaey, J.M. A 3.1–10.6-GHz 57-Bands CMOS Frequency Synthesizer for UWB-Based Cognitive Radios. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 4134–4146. [CrossRef]

3. Rategh, H.R.; Samavati, H.; Lee, T.H. A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver. *IEEE J. Solid-State Circuits* **2000**, *35*, 780–787. [CrossRef]
4. Manthena, V.K.; Do, M.A.; Boon, C.C.; Yeo, K.S. A Low-Power Single-Phase Clock Multiband Flexible Divider. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2012**, *20*, 376–380. [CrossRef]
5. Deng, Z.; Niknejad, A.M. The Speed–Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers. *IEEE J. Solid-State Circuits* **2010**, *45*, 2457–2465. [CrossRef]
6. Chen, W.H.; Jung, B. High-Speed Low-Power True Single-Phase Clock Dual-Modulus Prescalers. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2011**, *58*, 144–148. [CrossRef]
7. Liu, F.; Wang, Z.; Li, Z.; Li, Q.; Yang, G.; Guo, T. Low-power 25.4–33.5 GHz programmable multi-modulus frequency divider. *Electron. Lett.* **2014**, *5050*, 1067–1068. [CrossRef]
8. Gu, Q.J.; Gao, Z. A CMOS high speed multi-modulus divider with retiming for jitter suppression. *IEEE Microw. Wirel. Compon. Lett.* **2013**, *23*, 554–556. [CrossRef]
9. Shi, J.; Mo, T.; Ma, C.; Ye, T. A current-shaping technique for static MOS current-mode logic prescalers. *IEICE Electron. Express* **2013**, *10*, 20120887. [CrossRef]
10. Tsai, J.-H.; Chung, Y.-W.; Shih, H.-D.; Chou, J.-P. A 7-12 GHz Multi-Modulus Frequency Divider. In Proceedings of the Asia Pacific Microwave Conference Proceedings, Kaohsiung, Taiwan, 4–7 December 2012; pp. 1232–1234.
11. Vigilante, M.; Reynaert, P. A 25-102GHz 2.81-5.64mW Tunable Divide-by-4 in 28nm CMOS. In Proceedings of the IEEE Asian Solid-State Circuits Conference (ASSCC), Xiamen, China, 9–11 November 2015; pp. 1–4.
12. Razavi, B. TSPC logic [a circuit for all seasons]. *IEEE Solid-State Circuits Mag.* **2016**, *8*, 10–13. [CrossRef]
13. Hwang, Y.; Lin, J. Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2012**, *20*, 1738–1742. [CrossRef]
14. Jia, S.; Wang, Z.; Li, Z.; Wang, Y. A Novel Low-Power and High-Speed Dual-Modulus Prescaler Based on Extended True Single-Phase Clock Logic. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, Canada, 22–25 May 2016; pp. 2751–2754.
15. Shen, T.; Liu, J.; Song, C.; Xu, Z. A High-Speed Low-Power Divide-by-3/4 Prescaler using E-TSPC Logic DFFs. *Electronics* **2019**, *8*, 589. [CrossRef]
16. Wang, W.; Jia, S.; Wang, Z.; Pan, T.; Wang, Y. Low Voltage Dual-Modulus Frequency Divider Based on Extended True Single-Phase Clock Logic. In Proceedings of the IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC), Shenzhen, China, 6–8 June 2018; pp. 1–2.
17. Krishna, M.V.; Do, M.A.; Yeo, K.S.; Boon, C.C.; Lim, W.M. Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2010**, *57*, 72–82. [CrossRef]
18. Tooprakai, S.; Wisetphanichkij, S.; Tudsorn, A. A 1.1-V Low Power True Single-Phase Clock 2/3 Prescaler. In Proceedings of the International Electrical Engineering Congress (iEECON), Pattaya, Thailand, 8–10 March 2017; pp. 1–4.
19. Jiang, W.; Yu, F. 4.2 GHz 0.81 mW Triple-Modulus Prescaler Based on True Single-Phase Clock. *Electron. Lett.* **2016**, *52*, 1007–1008. [CrossRef]
20. Zhu, W.; Yang, H.; Gao, T.; Liu, F.; Yin, T.; Zhang, D.; Zhang, H. A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2015**, *23*, 194–197.
21. Chen, W.H.; Roa, E.; Loke, W.F.; Jung, B. A 14.1-GHz Dual-modulus Prescaler in 130nm CMOS Technology Using Sequential Implication Logic Cells. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Montreal, QC, Canada, 17–19 June 2012; pp. 341–344.
22. Krishna, M.V.; Jain, A.; Quadir, N.A.; Townsend, P.D.; Ossieur, P. A 1V 2mW 17GHz Multi-Modulus Frequency Divider Based on TSPC Logic Using 65nm CMOS. In Proceedings of the ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC), Venice Lido, Italy, 22–26 September 2014; pp. 431–434.
23. Jiang, W.; Yu, F.; Huang, Q. A Low-Power High-speed True Single-Phase Clock-Based Divide-By-2/3 Prescaler. *IEICE Electron. Express* **2017**, *14*, 20160446. [CrossRef]
24. Jia, S.; Yan, S.; Wang, Y.; Zhang, G. Low-power, High-Speed Dual Modulus Prescalers Based on Branch-Merged True Single-Phase Clocked Scheme. *Electron. Lett.* **2015**, *51*, 464–465. [CrossRef]
25. Silva-Pereira, M.; Caldinhas Vaz, J. Power optimization of both a high-speed counter and a retiming element for 2.4 GHz digital PLLs. *Electron. Lett.* **2018**, *54*, 284–285. [CrossRef]
26. Stas, F.; Bol, D. A 0.4-V 0.66-fJ/cycle Retentive True-Single-Phase-Clock 18T Flip-Flop In 28-Nm Fully-Depleted SOI CMOS. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2018**, *65*, 935–945. [CrossRef]

27. Shaikh, J.; Rahaman, H. High Speed and Low Power Preset-Able Modified TSPC D Flip-Flop Design and Performance Comparison with TSPC D Flip-Flop. In Proceedings of the International Symposium on Devices, Circuits and Systems (ISDCS), Howrah, India, 29–31 March 2018; pp. 1–4.
28. Li, Y.; Shin, G.; Li, Y. A Fully Static True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications. *IEEE Access* **2020**, *8*, 40232–140245.
29. Lin, J.; Sheu, M.; Hwang, Y.; Wong, C.; Tsai, M. Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 3033–3044. [CrossRef]
30. Szilagyi, L.; Li, S.; Xu, X.; Testa, P.V.; Gunia, M.; Seidel, A.; Carta, C.; Finger, W.; Ellinger, F. A Divide-by-4 and -8 Circuit for 77 GHz Radar in 22 nm FD-SOI CMOS. In Proceedings of the 4th Australian Microwave Symposium (AMS), Sydney, Australia, 13–14 February 2020.
31. Cai, Y.; Savanth, A.; Prabhat, P.; Myers, J.; Weddell, A.S.; Kazmierski, T.J. Ultra-Low Power 18-Transistor Fully Static Contention-Free Single-Phase Clocked Flip-Flop in 65-nm CMOS. *IEEE J. Solid-State Circuits* **2019**, *54*, 550–559. [CrossRef]
32. Yue, C.; Howard, C.L.; Zhiliang, H. Analysis and Design of a 14.1-mW 50/100-GHz Transformer-Based PLL With Embedded Phase Shifter in 65-nm CMOS. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 1193–1201.
33. Lo, Y.; Ho, W. A Low-Voltage PLL Design Using a New Calibration Technique for Low-Power Implantable Biomedical Systems. *Circuits Syst. Signal Process.* **2017**, *36*, 4809–4828. [CrossRef]