Article

Design and Analysis of f_T-Doubler-Based RF Amplifiers in SiGe HBT Technology

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Abstract: For performance-driven systems such as space-based applications, it is important to maximize the gain of radio-frequency amplifiers (RFAs) with a certain tolerance against radiation, temperature effects, and small form factor. In this work, we present a K-band, compact high-gain RFA using an f_T-doubler topology in a silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) technology platform. The through-silicon vias (TSVs), typically used for small-size chip packaging purposes, have been effectively utilized as an adjustable matching element for input impedance, reducing the overall area of the chip. The proposed RFA, fabricated in a modest 0.35 µm SiGe technology, achieves a gain of 14.1 dB at 20 GHz center frequency, and a noise figure (NF) of 11.2 dB at the same frequency, with a power consumption of 3.3 mW. The proposed design methodology can be used for achieving high gain, avoiding a complex multi-stage amplifier design approach.

Keywords: extreme-environment electronics; f_T doubler; heterojunction bipolar transistor (HBT); radio-frequency amplifier (RFA); silicon-germanium (SiGe); through-silicon-via (TSV)

1. Introduction

The continuous and growing need for high-performance extreme-environment electronics includes many applications, such as satellite systems, space exploration platforms, imaging systems, and energy exploration [1,2]. Due to intense radiation exposure in the space environment, the electronic devices suffer from different damaging effects, e.g., total ionizing dose (TID) effects, single event effects (SEE), which eventually leads to operation failure or device breakdown. For low earth orbit (LEO) applications such as small satellites or cubeSat, where TID is of primary interest, it is very important to build circuits and systems with required radiation hardness for ensuring their reliability. Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have garnered special attention from the space-electronics community due to their superior characteristics for a wide range of temperatures (−180 °C to 200 °C) as well as built-in tolerance against TID to multi-Mrad levels [3,4]. The built-in tolerance in SiGe HBTs are mainly due to the thin emitter-collector spacer, thin base oxide, and very thin shallow trench isolation between the collector-base junction [5].

A radio-frequency amplifier (RFA) is one of the main building blocks in radio frequency (RF) transmitter and receiver systems. It is critical to boost the gain of RFAs for loss compensation and signal conditioning while maintaining a compact form factor and low complexity. To improve the gain of an RFA, various circuit topologies, such as a cascode configuration and Darlington structure, have been proposed in the literature [6–10]. The cascode topology provides increased output resistance that leads to a higher output voltage, and increased isolation between the input and output ports, which simplifies the design of the matching network and reduces the Miller effect, at the cost of a higher power supply. Darlington structure-based amplifiers improve the unity-gain frequency (f_T) but suffer from inequal collector currents, which may cause potential instability at low frequencies [11]. The problem

of the inequal collector current of the Darlington pair structure can be removed by using a modified f_T-doubler cell. The use of f_T-doubler topology has been successfully implemented in power-amplifiers to have a high gain-bandwidth product [12,13]. Regarding the use of a SiGe-HBT f_T doubler, it has been shown that the f_T-doubler cell can be modeled as a single transistor for circuit-design purposes [14,15].

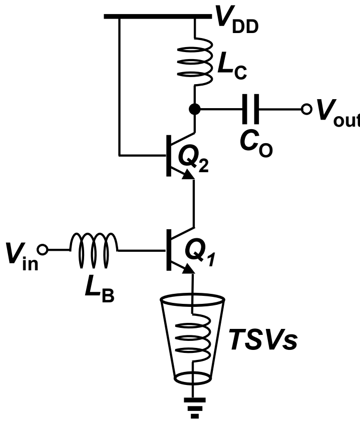
In this work, we propose f_T-doubler-based RFAs using a cascode configuration for improving the gain or the usable bandwidth of the amplifier. The f_T-doubler cell is used as the common-emitter (CE) input stage, and a single SiGe HBT is used as the common-base (CB) cascode stage. Furthermore, based on the findings in [16–18], we investigated the application of through-silicon vias (TSVs), which potentially reduce the overall area and complexity of the system. A TSV, which can be modeled as a very small resistor and an inductor in a series [19], also plays an important role in input matching and noise optimization. The rest of the paper is organized as follows. In Section 2, we describe the operation of the proposed f_T-doubler-based amplifier, and in Section 3, the experimental results and the relevant analysis are presented. Finally, Section 4 summarizes the paper.

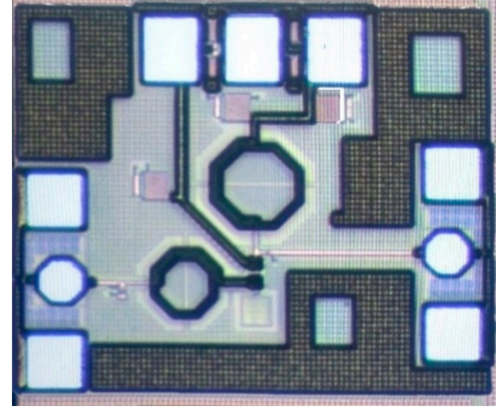
2. Proposed f_T-Doubler RF Amplifier with TSVs

In the proposed f_T-doubler amplifier, the f_T-doubler cell (the red box in Figure 1b) is used in the input CE stage, and a single transistor is used as the cascode stage (Q_4 in Figure 1b), whereas the conventional cascode topology is shown in Figure 1a. The f_T-doubler CE stage, which can be modeled as a single transistor [14,15], is realized by using a modified Darlington pair, wherein two transistors, Q_1 and Q_2, are connected in series, with an additional diode-connected transistor, Q_3, which adaptively adjusts the base-to-emitter voltage of Q_2 for a different DC bias condition or a large AC signal. In the proposed circuit, Q_1 and Q_2 are biased with the same (or almost similar) currents so that the transconductance (g_m) of both devices remain close to each other to maximize RF performance. The higher gain of the proposed amplifier is achieved by the Darlington operation, whose overall current gain of the f_T-doubler cell is given by the product of current gain β_1 and β_2 of Q_1 and Q_2, respectively.

$$\beta_{f_T\ doubler} \approx \beta_1 \times \beta_2 \tag{1}$$

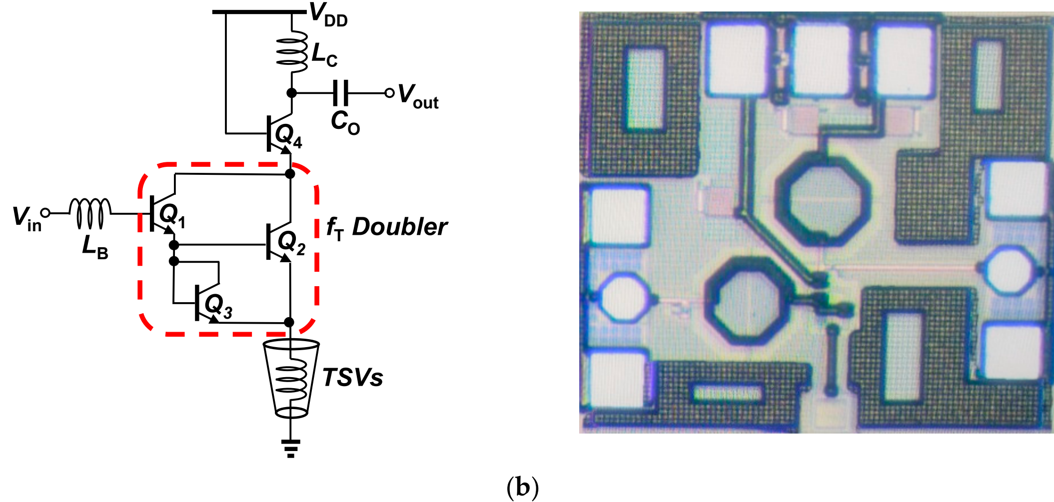
The amplified collector current enters the emitter of the CB transistor and exits the collector with a unity current gain in an ideal case. The collector current is converted to a voltage by the load impedance at the collector of the CB transistor. Due to the high output resistance of the cascode topology, the overall impedance is determined by the output collector inductor (L_C).





(a)

Figure 1. *Cont.*



(**b**)

Figure 1. (**a**) Schematic and micrograph of the conventional through-silicon vias (TSV)-integrated unity-gain frequency (f_T)-doubler amplifier; (**b**) the schematic of the proposed TSV-integrated cascode Silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) amplifier (biasing is not shown).

A TSV provides a low-loss electrical connection from the top side of the silicon substrate to the backside, and it is used to present a direct path to ground, eliminating a bonding wire and its parasitics. For simplicity, a TSV can be modeled as a negligible small resistance in series with an inductance [18]. At high frequencies, this inductance associated with a TSV can be used to design impedance matching and optimize noise figure. TSVs can form an array of shapes to adjust the effective resistance and inductance, and as a result, the number of TSVs can be selected based on the required inductance for design optimization [16]. Although, due to the resistance and the inductance associated with TSVs at the emitter of the CE transistor, the gain of the amplifier can be degraded theoretically, typical resistance will be much smaller than a few ohms, which can be ignored in the small-signal equivalent circuit of the f_T doubler, as shown in Figure 2.

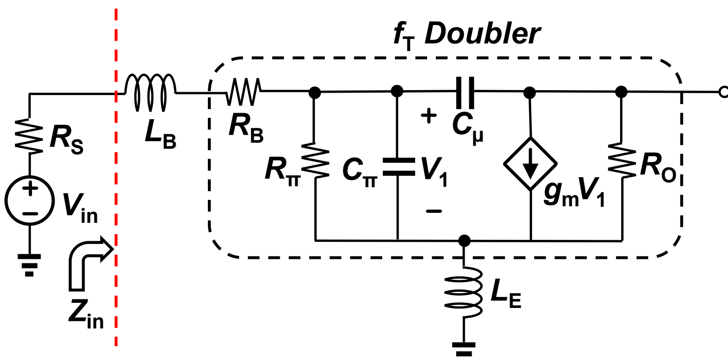


Figure 2. Equivalent small-signal model of the proposed TSV-integrated RF f_T-doubler amplifier.

For simplification of calculation, if we consider the small-signal model where R_π is very high and C_μ is very small, the effective G_m with degeneration inductance is [20],

$$G_m = \frac{g_m}{\omega_0(g_m L_E + C_\pi R_B)} \tag{2}$$

In (2), L_E, g_m, R_B, and ω_0 are emitter inductance, transconductance, base resistance, and the operation frequency, respectively. We can see that if the degeneration inductance (L_E) increases, the effective G_m decreases, so does the gain of the amplifier.

2.1. Input and Output Matching

The input and output matching networks affect the bandwidth and the power transfer between stages. In the proposed RFA, the input matching is accomplished using a series inductor (L_B) and degeneration inductance (L_E) in the TSV, achieving a higher gain and lower noise figure simultaneously. For input matching, the imaginary part of the input impedance should be zero, and the real part should be equal to 50 Ω. The input impedance of the amplifier can be found from Figure 2 and is derived as follows:

$$Z_{in} = [\frac{1 + \frac{sL_E}{R_\pi} + s^2 L_E C_\pi + g_m s L_E + \frac{sL_E(sC_\mu - g_m)}{\left(1+\frac{sC_\mu}{R_0}\right)}}{\frac{1}{R_\pi} + sC_\pi + sC_\mu - \frac{sC_\mu(sC_\mu - g_m)}{\left(\frac{1}{R_0} + g_m\right)}} + sL_B + R_B] \tag{3}$$

where R_π, C_μ, L_B, and R_0 are input resistance from base to emitter, base-to-collector capacitance, base series inductor for input matching, and the output resistance of the amplifier, respectively. Because of the complexity associated with (3), it is difficult to separate the real and the imaginary part with intuitive meanings for matching network design. If we simplify the small-signal model where $R_\pi = \infty,\ r_0 = \infty,\ and\ C_\mu = 0$, then the simplified expression would be

$$Z_{in} = sL_B + sL_E + \frac{1}{sC_\pi} + R_B + \frac{g_m L_E}{C_\pi} \tag{4}$$

From (4), it can be realized that the value of L_E of a TSV can be adjusted to achieve the 50 Ω real input impedance. This will eliminate the use of an extra on-chip emitter inductor or transmission line, which reduces the overall chip area as well. The output matching was straightforward, where collector inductor (L_C) and output capacitor (C_o) are tuned to resonate at the operation frequency.

2.2. Noise Figure Calculation

The overall noise figure (NF) of the amplifier will heavily depend upon the noise performance of the input stage (i.e., f_T-doubler cell) in the proposed amplifier since the noise contribution from the cascode CB stage is relatively smaller [21]. The main noise sources of a SiGe HBT is the noise generated at the base due to the base resistance and the base-emitter shot noise, whereas for the inductive degenerated amplifiers, the contribution of the collector-to-emitter noise is relatively smaller [22]. The NF of the proposed amplifier can be calculated by using the simplified small-signal noise model, as shown in Figure 3.

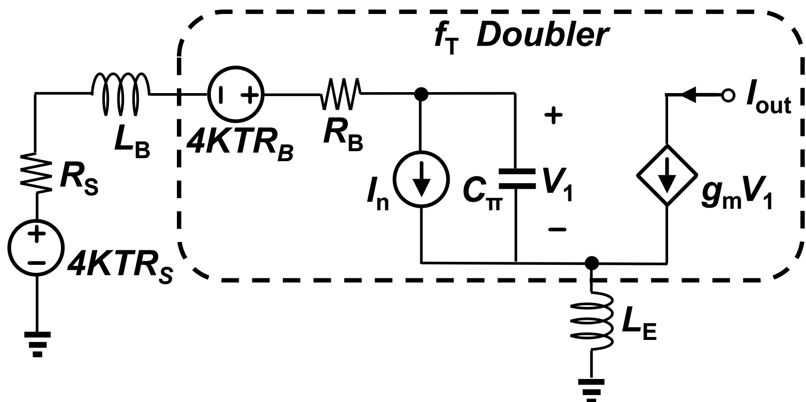


Figure 3. Simplified small-signal noise model of the proposed TSV-integrated f_T-doubler amplifier.

The NF of the proposed amplifier under impedance-matched conditions can be derived as follows [20,23,24],

$$NF = 1 + \frac{R_B}{R_S} + \frac{qI_B}{2kTR_S}\left[(R_B + R_S)^2 + \omega_0^2(L_B + L_E)^2\right] \quad (5)$$

Here, q, k, T, and I_B are electron charge, Boltzmann constant, absolute temperature, and the base bias current, respectively. The NF of the proposed f_T-doubler RFA will be degraded from that of conventional cascode amplifiers because R_B in the f_T-doubler cell is almost twice of that of single HBTs [14]. From (5), it is shown that by optimizing the number of TSVs, L_E can be adjusted for balancing both input matching and noise performance.

3. Measurement Results and Discussion

The proposed TSV-integrated f_T-doubler RF amplifiers (RFAs) were designed and fabricated for K-band operation, using a commercial 0.35-µm SiGe HBT technology [17], whose f_T and the maximum oscillation frequency (f_{max}) are in the range of 30 GHz and 60 GHz, respectively [25,26]. The scattering parameters (S-parameters) and the NF were measured using a network analyzer (Agilent PNA E8364B) and a signal analyzer (Agilent PXA N9030A) with a noise source (Agilent N4002A), respectively. For comparison purposes, three RFAs (on-chip conventional, TSV-integrated conventional, and the proposed TSV-integrated f_T-doubler RFAs) were characterized. The schematic and the chip micrograph of the TSV-integrated conventional and the proposed f_T-doubler RFAs are shown in Figure 1.

The measured S-parameter response of the proposed TSV-integrated f_T-doubler RFA under a fixed bias current of 1.1 mA is shown in Figure 4. For measurement purposes, the DC and RF probes shared the ground potential through the on-chip ground mesh, but they were isolated from the TSV ground, which was provided from the chuck of the probe station. The proposed RFA had a peak gain of 14.11 dB at the center frequency of 20 GHz, and the 3-dB gain bandwidth was about 1.3 GHz. The input and the output ports were matched around the peak gain frequency, showing broader input matching due to the lower Q-factor from the small-base resistance than the output.

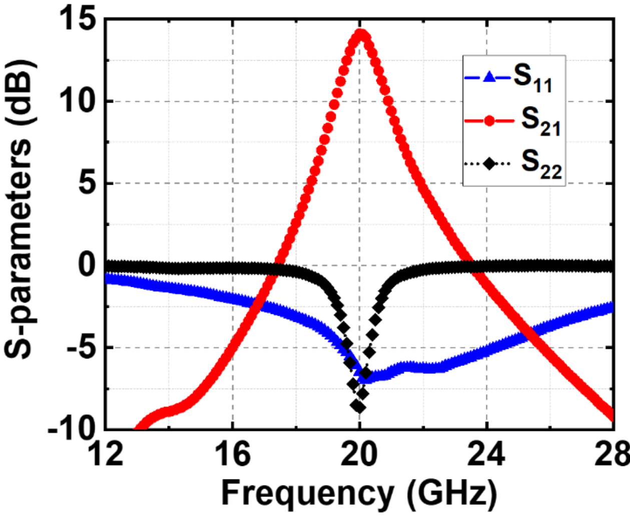


Figure 4. Measured S-parameters of the TSV integrated f_T-doubler radio-frequency amplifier (RFA).

Figure 5 shows the gain (S_{21}) comparison of the three RFAs versus frequency. The TSV-integrated conventional cascode RFA shows a slight degradation (0.8 dB) in gain compared with the on-chip conventional RFA. This is due to the presence of large parasitics at the interface between the backside of TSVs and the probe station chuck. Since the TSV-integrated f_T-doubler RFA provides an additional gain (or increased f_T), it shows that the proposed approach is a viable solution for gain boosting with compact size. The proposed RFA has a gain increase of 3.7 dB from that of the conventional TSV-integrated amplifier. In addition, the stability (µ factor) of our proposed RFA was confirmed

over a wide range of frequency (10–30 GHz) and compared with the conventional cascode amplifiers (Figure 6).

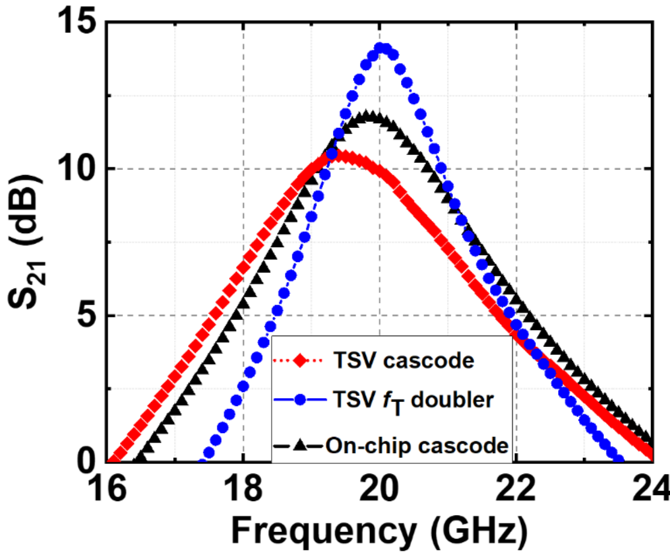


Figure 5. Comparison gain (S_{21}) between the on-chip RFAs and TSV-integrated RFAs.

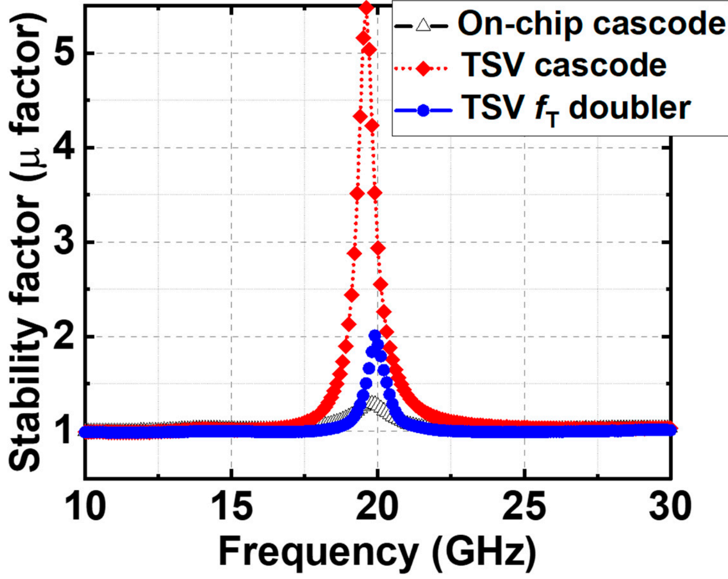


Figure 6. Stability factor (μ factor) of the proposed f_T-doubler and conventional cascode RFAs.

The noise performance of the proposed RFA is shown in Figure 7. The NF of the proposed RFA was degraded by 4.3 dB at 20 GHz from the conventional TSV-integrated cascode topology due to a larger R_B. Since the high-frequency metrics (f_T and f_{MAX}) of the given process was conservative, however, the resulting lowest NF of the conventional cascode RFA as well as the proposed RFA was inevitably high (6.5 dB and 10.4 dB, respectively) at 20 GHz compared with typical low-noise amplifiers in a similar frequency range in the literature. With more advanced SiGe BiCMOS technologies [27], it is expected that the NF will show a more significant improvement than the noise performance of the RFA prototypes.

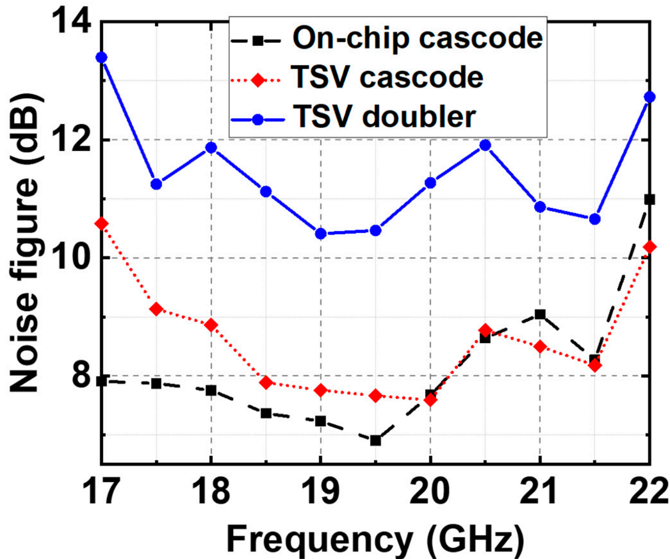


Figure 7. NF comparison between the proposed f_T-doubler and conventional cascode RFAs.

In Table 1, the performance parameters of the proposed RFAs and the conventional cascode RFA are summarized. The improved gain or extended frequency range of the proposed f_T-doubler RFA with the advantage of a reduced chip area was achieved with a tradeoff in NF and power consumption. With the use of advanced scaled transistors, the performance of the f_T-doubler-based amplifier can certainly improve maintaining a reasonable NF performance.

Table 1. Performance Summary.

RFA Type	f_{center} (GHz)	Gain (dB)	NF (dB)	P_{DC} (mW)
On-chip conventional cascode	19.6	11.2	6.6	1.8
TSV conventional cascode	19.4	10.4	6.9	1.8
Proposed TSV f_T-doubler	20.0	14.1	11.2	3.3

The fabricated RFAs were irradiated by an x-ray source for characterizing radiation-induced degradations. The RFAs were still functional after exposure to a total dose of 1 Mrad (SiO_2). The TID x-ray irradiation results of the TSV-integrated conventional cascode and the proposed RFAs are summarized in Table 2.

Table 2. X-ray Irradiation Results.

RFA Type	Gain	NF	P_{DC}
TSV cascode	−2.3 dB	+0.40 dB	<+2%
f_T-doubler cascode	−2.9 dB	+0.43 dB	<+2%

4. Conclusions

This work presents an improvement in the gain of radio-frequency amplifiers (RFAs) for high-performance applications by using the f_T-doubler cell as an input stage. Whereas there is a tradeoff in noise figure and power consumption in the proposed RFA, the peak gain increases significantly, demonstrating extended usable frequency range. In addition, the use of TSVs as impedance-matching elements enables the elimination of a transmission-line structure or a lumped inductor, potentially reducing the overall chip area.

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writing—review and editing, I.S.; visualization, M.A.R.S.; supervision, I.S.; All authors have read and agreed to the published version of the manuscript.

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