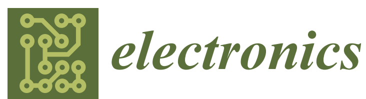

Article

Analytical Drain Current Model for a-SiGe:H Thin Film Transistors Considering Density of States

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Abstract: Thin film transistors (TFTs) fabricated on flexible and large area substrates have been studied with great interest due to their future applications. Recent studies have developed new semiconductors such as a-SiGe:H for fabrication of high performance TFTs. These films have important advantages, including deposition at low temperatures and low pressures, and higher carrier mobilities. Due to these advantages, the a-SiGe:H films can be used in the fabrication of TFTs. In this work, we present an analytical drain current model for a-SiGe:H TFTs considering density of states and free charges, which describes the current behavior at sub-and above- threshold region. In addition, 2D numerical simulations of a-SiGe:H TFTs are developed. The results of the analytical drain current model agree well with those of the 2D numerical simulations. For all characteristics of the drain current curves, the average absolute error of the analytical model is close to 5.3%. This analytical drain current model can be useful to estimate the performance of a-SiGe:H TFTs for applications in large area electronics.

Keywords: a-SiGe:H; density of states; current model; thin film transistor; simulations

1. Introduction

Thin film transistors (TFTs) are key devices to develop large area electronics applications such as active matrix liquid crystal displays (AMLCD) [1–3], wearable sensors [4,5] and passive tags RFID (radio frequency identification) [6–8]. Nowadays, TFT technology is based on amorphous silicon (a-Si), polysilicon (poly-Si) and IGZO (indium-gallium-zinc oxide) semiconductors. The a-Si TFTs offer small electron mobilities (<1 cm^2/Vs), and thus low switching speed [9]. The other hand, poly-Si TFTs are devices with high performance, but they are fabricated at higher temperatures (500–600 °C) [10–12], while IGZO TFTs have moderate mobilities (>10 cm^2/Vs) and low temperature of fabrication [13]. However, this semiconductor is only used for the fabrication of n-type devices, for p-type is used a different semiconductor, such as SnO [14]. To overcome these limitations, hydrogenated amorphous silicon-germanium (a-SiGe:H) films can be used to fabricate TFTs at low temperature of deposition (<300 °C) by PECVD technique. This allows carrier mobilities higher than 1 cm^2/Vs caused by the incorporation of germanium and hydrogen atoms. In addition, a-SiGe:H TFTs can have an ambipolar behavior, allowing their operation into either as n- or p-type [15]. In order to design a-SiGe:H TFTs

for specific applications, it is necessary to predict the behavior of their drain currents. Shur et al. [16] reported a physical drain current model for n- and p-channels hydrogenated amorphous silicon and polysilicon staggered bottom-gate top-contact TFTs. This model was implemented into an AIM-SPICE circuit simulator. However, it is adapted from MOSFET model and it does not include semiconductor density of states. Chen et al. [17] reported an analytical drain current model for both triode and saturation region of operation for a-Si:H TFTs considering semiconductor density of states and an effective temperature approach. However, this model registered a high error between measurements and modeled results. Liu et al. [18] presented an analytical drain current model for a-Si:H TFTs based on surface potential, which was compared with numerical simulations considering free and localized carrier densities into the semiconductor. Colalongo et al. [19] designed an analytical drain current model for a-Si:H TFTs based on deep and tail states in both semiconductors, which describe the behavior at sub-threshold and above-threshold mode of operation.

In this paper, we develop an analytical drain current model for a-SiGe:H TFTs that considers free and localized charges into semiconductor and its characteristic temperatures, which can represent the behavior at sub-threshold and above-threshold regions of operation without using fitting parameters. In addition, 2D numerical simulations using finite element method of the output and transfer characteristics of bottom-gate top-contact coplanar a-SiGe:H TFTs are reported. The results of our analytical drain current model agree well with respect to those of the numerical simulations. In Section 2, electrostatic analysis and derivation of expressions for electric field and drain current are explained. In Section 3, comparison of our model and simulation results are presented. Finally, the conclusions are discussed in Section 4.

2. Analytical Drain Current Model for a-SiGe:H TFTs

2.1. Density of Estates of Amorphous Semiconductors

The density of states, $g(E)$, of an amorphous semiconductor thin film consists of four energy bands over the bandgap: two tail bands and two deep bands. Tail bands consist of a donor-like valence band, $g_{TA}(E)$, and an acceptor-like conduction band, $g_{TD}(E)$. On the other hand, deep bands are composed of a donor-like valence band, $g_{GA}(E)$, and an acceptor-like conduction band, $g_{GD}(E)$, which are represented as follow, [20]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \tag{1}$$

$$g_{TA}(E) = NTA \cdot \exp[(E - E_C)/WTA] \tag{2}$$

$$g_{TD}(E) = NTD \cdot \exp[(E_V - E)/WTD] \tag{3}$$

$$g_{GA}(E) = NDA \cdot \exp\left[-((E - E_{GA})/WGA)^2\right] \tag{4}$$

$$g_{GD}(E) = NDD \cdot \exp\left[-((E - E_{GD})/WGD)^2\right] \tag{5}$$

where E is the trap energy, E_C and E_v are the conduction and valence band energy, respectively; WTA (kT_{tail}) and WTD (kT_{tail}) are acceptor and donor characteristic decay energy for the tail band, respectively; WGA (kT_{deep}) and WGD (kT_{deep}) are acceptor and donor characteristic decay energy for the deep band, respectively; NTA, NTD, NDA and NDD are the conduction and valence band edge intercept densities for the tail and deep band, respectively.

2.2. Analytical Drain Current Model

Figure 1a shows a schematic cross section of a n-type coplanar bottom-gate top-contact a-SiGe:H TFT with SiO_2 as gate insulator and a-Ge:H n+ layers for drain and source extensions. In this Figure, T_{ox} and T_{sc} are the gate oxide and semiconductor thickness, respectively. Figure 1b depicts the diagram of energy band for MIS (metal-insulator-semiconductor) region for this device working under

accumulation regimen, when a positive gate potential (V_G) is applied. For this Figure, E_C and E_V are energy levels of conduction and valence bands, respectively; E_{Fm}, and E_{Fn} are the Fermi energy levels for metal, intrinsic and n-type semiconductor, respectively; φ_S and $\varphi_{CH}(x)$ are surface and channel potential; and $\varphi_{F0}(x)$ is the potential between E_c and E_{Fn}.

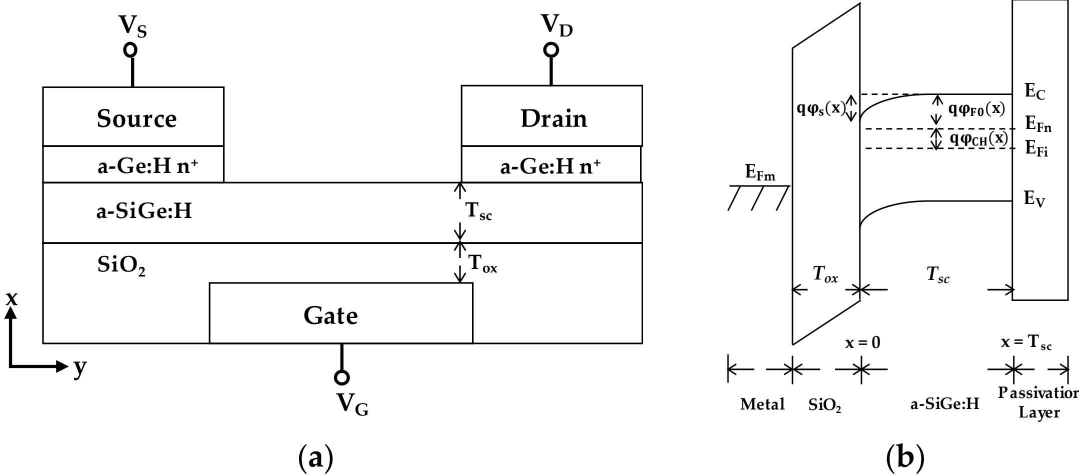

Figure 1. (**a**) Cross-section of a coplanar bottom-gate top-contact a-SiGe:H TFT; (**b**) equivalent energy band diagram of the MIS region of this device.

2.2.1. Derivation of Electric Field

Taking into account the free and localized electron concentration for an n-type amorphous semiconductor, the Poisson's equation in one dimension, along the x direction, can be expressed as:

$$\frac{\partial^2 \phi(\mathrm{x})}{\partial x^2} = -\frac{\rho(\mathrm{x})}{\varepsilon_{sc}} = \frac{q}{\varepsilon_{sc}}\left(n_{free}(\mathrm{x}) + n_{deep}(\mathrm{x}) + +n_{deep}(\mathrm{x})\right) \tag{6}$$

where q is the electron charge, $\phi(x)$ is the potential across the active layer, $\rho(x)$ is the total charge density, ϵ_{sc} is the permittivity constant of the semiconductor layer, $n_{free}(x)$, $n_{deep}(x)$ and $n_{tail}(x)$ are the free, deep and tail electron concentrations, respectively. These concentrations for a-SiGe:H layer can be expressed as:

$$n_{free}(\mathrm{x}) = N_{free}\exp\left[\frac{q(\phi(\mathrm{x}) - \mathrm{V_{CH}} - \phi_{\mathrm{F0}})}{kT_{free}}\right] \tag{7}$$

$$N_{free} = N_C g^{(T/T_{free})} kT \frac{\pi}{sin\left(\pi T/T_{free}\right)} \tag{8}$$

$$n_{deep}(\mathrm{x}) = N_{deep}\exp\left[\frac{q(\phi(\mathrm{x}) - \mathrm{V_{CH}} - \phi_{\mathrm{F0}})}{WGA}\right] \tag{9}$$

$$N_{deep} = g_{GA} g^{(T/T_{deep})} kT \frac{\pi}{sin\left(\pi T/T_{deep}\right)} \tag{10}$$

$$n_{tail}(\mathrm{x}) = N_{tail}\exp\left[\frac{q(\phi(\mathrm{x}) - \mathrm{V_{CH}} - \phi_{\mathrm{F0}})}{WTA}\right] \tag{11}$$

$$N_{tail} = g_{TA} g^{(T/T_{deep})} kT \frac{\pi}{sin\left(\pi T/T_{deep}\right)} \tag{12}$$

where N_C is the free electron concentration, V_{CH} is the potential along the channel, q is the electron charge, k is Boltzmann constant, T is a reference temperature and g is the degeneration factor which depends of the temperature ratio (T/T_{eff}) as exponential expression.

In order to simplify the analysis, an effective carrier concentration (N_{eff}) instead of free, deep or tail carrier concentrations (N_{free}, N_{deep} or N_{tail}), which are computed with Equations (8), (10) or (12) equations, respectively, is proposed. In the same way, an effective characteristic temperature (T_{eff}) instead of free, deep or tail temperature (T_{free}, T_{deep} or T_{tail}), respectively, is used.

To derivate the electric filed as function of electrostatic potential, it is necessary to solve the following Poisson´s equation:

$$\frac{\partial^2 \phi(\mathrm{x})}{\partial x^2} = -\frac{\rho(\mathrm{x})}{\varepsilon_{sc}} = \frac{q}{\varepsilon_{sc}} n_{eff}(\mathrm{x}) \tag{13}$$

By employing the next expression to change the integration variable, from x to $\phi(\mathrm{x})$:

$$\frac{d}{dx}\left[\left(\frac{d\phi(\mathrm{x})}{dx}\right)^2\right] = 2\left(\frac{d\phi(\mathrm{x})}{dx}\right)\left(\frac{d^2\phi(\mathrm{x})}{dx^2}\right) \tag{14}$$

By integrating both sides in Equation (14) and applying the square root, we have:

$$\frac{d\phi(\mathrm{x})}{dx} = \sqrt{2\int\left(\frac{d\phi(\mathrm{x})}{dx}\right)\left(\frac{d^2\phi(\mathrm{x})}{dx^2}\right)dx} = \sqrt{2\int\left(\frac{d^2\phi(\mathrm{x})}{dx^2}\right)d\phi(\mathrm{x})} \tag{15}$$

By substituting Equation (13) into Equation (15) and applying the boundary conditions from x = 0 (ϕ_S (x)) to x = T_{SC} (ϕ_B(x)), the electric field as a function of $\phi(\mathrm{x})$ is expressed as:

$$E(\phi(\mathrm{x})) = -\frac{d\phi(\mathrm{x})}{dx} = \sqrt{2\int_{\phi(\mathrm{x}=T_{sc})=\phi_B}^{\phi(\mathrm{x}=0)=\phi_S} \frac{q}{\varepsilon_{sc}} n_{eff}(\mathrm{x}) d\phi(\mathrm{x})} = \sqrt{\frac{2N_{eff}kT_{eff}}{\varepsilon_{sc}}\left(n_{eff}(\phi_S(\mathrm{x})) - n_{eff}(\phi_B(\mathrm{x}))\right)} \tag{16}$$

where n_{eff} is the effective electron density, T_{eff} is the effective characteristic temperature, ε_{sc} is the semiconductor permittivity, $\phi_S(x)$ is the electrostatic potential in the gate insulator/semiconductor interface, $\phi_B(x)$ is the electrostatic potential in the semiconductor/passivation layer interface, which is neglected because is close to zero. Thus, the transversal electric field through an amorphous semiconductor, at *x* direction, is given by:

$$E(\phi(\mathrm{x})) = \sqrt{\frac{2N_{eff}kT_{eff}}{\varepsilon_{sc}}}\exp\left[\frac{q(\phi_S - \mathrm{V_{CH}} - \phi_{\mathrm{F0}})}{2kT_{eff}}\right] \tag{17}$$

2.2.2. Derivation of Drain to Source Current in Subthreshold Region, I_{DS_sub}

In the subthreshold region operation of a-SiGe:H TFT, that is gate to source voltage, V_{GS}, is less than threshold voltage, V_{TH}, but larger than the flat band voltage, V_{FB}, ($V_{FB} < V_{GS} < V_{TH}$), most of the carriers are free electrons, because of deep and tail localized carriers are trapped into semiconductor defects. Therefore, it is necessary to apply a larger V_{GS} in order to generate a higher transversal electric field to the active layer to set free those charges. In addition, for this semiconductor (see Table 1) the localized energy characteristics (kT_{tail} and kT_{deep}) are higher than the free energy characteristic (kT_{free}). Thus, $\rho(x)$ for an a-SiGe:H TFT at subthreshold operation can be obtained by:

$$\frac{\rho(\mathrm{x})}{-q} = n_{eff}(\mathrm{x}) \approx n_{free}(\mathrm{x}) \tag{18}$$

Table 1. Electrical parameters for a-SiGe:H and SiO_2 layers [20].

Name	Parameter	a-SiGe:H	SiO_2
Permittivity	ϵ	11.8	3.9
Electronic affinity	X	4.01 eV	0.9 eV
Bandgap	E_g	1.4 eV	9 eV
Intrinsic concentration	n_i	1×10^{12} cm^{-3}	- *
Conduction band density	N_c	1×10^{20} cm^{-3}	- *
Valence band density	N_v	1×10^{20} cm^{-3}	- *
Electron band mobility	μ_0	0.56 cm^2/Vs	- *
Bulk Fermi Level	Φ_{F0}	0.56 V	- *
Flat band voltage	V_{FB}	−0.01 V	- *

* Data not available in the literature.

In order to derive the drain to source current in subthreshold regimen, I_{DS_sub}, is employed the gradual channel approximation expression, which is given by:

$$I_{\mathrm{DS_sub}} = W\frac{dV_{CH}(y)}{dy}\int_{x=0}^{x=Tsc}\sigma_n(\mathrm{x})\mathrm{dx} = W\frac{dV_{CH}(\mathrm{y})}{dy}\int_{\phi(\mathrm{x}=t_{sc})}^{\phi(\mathrm{x}=0)} q\mu_0\frac{n_{free}(\phi(\mathrm{x}))}{E(\phi(\mathrm{x}))}d\phi(\mathrm{x}) \quad (19)$$

where W is the channel width of TFT, $\sigma_n(x)$ is the n-type channel conductivity of a-SiGe:H, $E(\varphi(x))$ is the electric field dependent of potential at x direction, and μ_0 is the carrier mobility of semiconductor.

The final expression for drain to source current at region of subthreshold for an a-SiGe:H TFT is computing solving Equation (19), step-by-step at Appendix A, considering $N_{eff} = N_{free}$ and $T_{eff} = T_{free}$, as follows:

$$I_{DS_sub}(N_{free}, T_{free}) = \mu_0\frac{W}{L}\frac{A_{free}}{B_{free}}\left(\frac{C_{OX}}{\sqrt{2\varepsilon_{sc}N_{free}kT_{free}}}\right)^{C_{free}}\left[\frac{1}{C_{free}+1}\left((\delta V_{SD})^{C_{free}+1} - (\delta V_{SS})^{C_{free}+1}\right) + \frac{1}{\mathrm{q}B_{free}}\left((\delta V_{SD})^{C_{free}} - (\delta V_{SS})^{C_{free}}\right)\right] \quad (20)$$

with:

$$A_{free} = \frac{N_c}{\sqrt{\frac{2N_{free}kT_{free}}{\varepsilon_{sc}}}} \quad (21)$$

$$B_{free} = \frac{1}{kT} - \frac{1}{2kT_{free}} \quad (22)$$

$$C_{free} = 2kT_{free}B_{free} \quad (23)$$

$$\delta V_{SD} = V_{GS} - V_{FB} - V_D \quad (24)$$

$$\delta V_{SS} = V_{GS} - V_{FB} - V_S \quad (25)$$

2.2.3. Derivation of Drain Current at Above Threshold Region, I_{DS_abv}

Above threshold region of a-SiGe:H TFT operation, that is when $V_{GS} > V_{TH}$, free and localized charges are taken in to account due to the applied gate to source voltage generates a strong transversal electric field to the active layer which produces an accumulation of both carriers in the semiconductor/gate-insulator interface. However, in this semiconductor $n_{deep}(x) << n_{tail}(x)$. Thus, we obtained the following equation:

$$\frac{\rho(\mathrm{x})}{-q} = n_{eff}(\mathrm{x}) \approx n_{free}(\mathrm{x}) + n_{tail}(\mathrm{x}) \quad (26)$$

Poisson's equation is applied as follows:

$$\frac{\partial^2\phi(\mathrm{x})}{\partial x^2} = -\frac{\rho(\mathrm{x})}{\varepsilon_{sc}} \cong \frac{q}{\varepsilon_{sc}}\left(n_{free}(\mathrm{x}) + n_{tail}(\mathrm{x})\right) \quad (27)$$

By using the gradual channel approximation Equation (19) and the procedure in Appendix A, taking into account free and tail localized charges along the semiconductor, we can derive the drain to source current for the above threshold region, I_{DS_abv}, as follows:

$$\begin{aligned} I_{DS_abv} &= I_{DS}(N_{free}, T_{free}) + \mathrm{I}_{\mathrm{DS}}(N_{tail}, T_{tail}) \\ &= I_{DS}(N_{free}, T_{free}) + \mu_0 \tfrac{W}{L} \tfrac{A_{tail}}{B_{tail}} \left(\frac{C_{OX}}{\sqrt{2\varepsilon_{sc} N_{tail} k T_{tail}}} \right)^{C_{tail}} \left[\tfrac{1}{C_{tail}+1} \left((\delta V_{SD})^{C_{tail}+1} - (\delta V_{SS})^{C_{tail}+1} \right) + \tfrac{1}{qB_{tail}} \left((\delta V_{SD})^{C_{tail}} - (\delta V_{SS})^{C_{tail}} \right) \right] \end{aligned} \tag{28}$$

with

$$A_{tail} = \frac{N_c}{\sqrt{\frac{2N_{tail} k T_{tail}}{\varepsilon_{sc}}}} \tag{29}$$

$$B_{tail} = \frac{1}{kT} - \frac{1}{2kT_{tail}} \tag{30}$$

$$C_{tail} = 2kT_{tail} B_{tail} \tag{31}$$

2.2.4. Total Analytical Drain Current Model

The final unified analytical drain current model for a-SiGe:H TFTs takies into account the sub-threshold and above-threshold regions, which it considers the density of states of such amorphous semiconductor and free electrons, is estimated by adding I_{DS_sub} and I_{DS_abv} with the following expression:

$$I_{DS} = \frac{1}{\left(\frac{1}{I_{DS_sub}} + \frac{1}{I_{DS_abv}} \right)} \tag{32}$$

3. Results and Discussion

In order to compare the results of our analytical drain current model, we develop 2D numerical simulations for bottom-gate top-contact coplanar a-SiGe:H TFTs using Silvaco TCAD software through Atlas and Devedit tools (Santa Clara, CA, USA) [21]. These simulation tools use finite element method to perform the electrostatic analysis. Figure 2 shows a schematic view of the cross-section of the proposed device and its main geometrical parameters. The substrate is silicon oxide with a thickness T_{SUB} = 200 nm. The gate and drain/source electrodes are aluminum with thickness T_G and $T_{D/S}$ of 100 nm, respectively. SiO_2 is used as gate insulator with a thickness T_{OX} = 80 nm. An overlap length between gate and drain/source electrodes of L_{OV} = 10 nm is used. Then, a thin film of a-SiGe:H as active layer or semiconductor with a thickness T_{SC} = 100 nm and a length channel L = 75 µm is used. The width of the active layer W = 30 µm is used for calculation. A layer of high doped germanium as drain/source extension region with thickness T_{EXT} = 40 nm and length $L_{D/S}$ = 2 µm are employed to get a good ohmic contact with the semiconductor. Finally, SiN_4 as passivating dielectric layer with T_{PASS} = 200 nm is used in order to reduce broken bonds of the a-SiGe:H surface and carriers recombination.

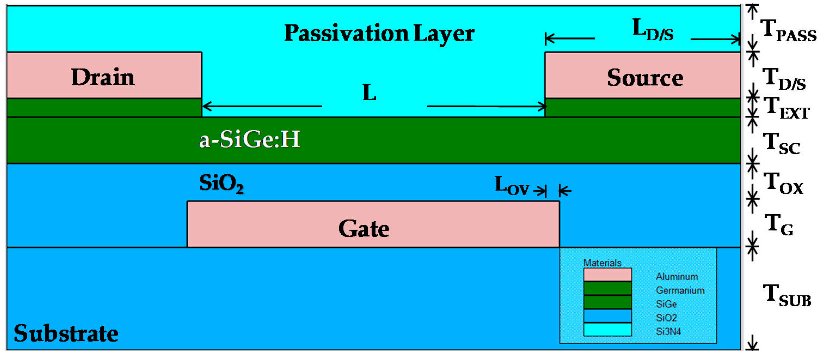

Figure 2. Bottom-gate top-contact coplanar TFT structure and its geometrical parameters used for 2D numerical simulations.

The parameters for semiconductor and gate insulator layers considered in the numerical simulations and analytical drain current model are listed in Table 1. Furthermore, defects parameters that define the density of states of a-SiGe:H layer used for simulations and modeling are shown in Table 2. Some of those values were taken from [20].

Table 2. Defects parameters of a-SiGe:H layer employed in analytical model and numerical simulations [20].

Name	Parameter	Value
Zero bias density of states acceptor for tail state	g_{TA}	1×10^{20}
Zero bias density of states acceptor for deep state	g_{GA}	2×10^{16}
Degeneration factor	G	2
Correlation energy	U=EGA − EGD	0.3 eV
Acceptor characteristic decay energy for deep state	WGA	0.3 eV
Donor characteristic decay energy for deep state	WGD	0.3 eV
Acceptor density distribution for deep state	NGA	2×10^{16} cm^{-3}
Donor density distribution for deep state	NGD	2×10^{16} cm^{-3}
Acceptor density distribution for tail state	NTA	1×10^{20}
Acceptor density distribution for deep state	NTD	1×10^{20}
Reference characteristic temperature	T	182.8 K
Free characteristic temperature	T_{free}	300 K
Deep state characteristic temperature	T_{deep}	649.8 K
Tail state characteristic temperature	T_{tail}	324.92 K
Acceptor characteristic decay energy tail state	WTA	0.028 eV
Donor characteristic decay energy for tail state	WTD	0.056 eV
Electron capture cross-section for the donor gaussian state	SIGGDE	1.3×10^{-14}
Electron capture cross-section for the acceptor gaussian state	SIGGAE	2.7×10^{-14}
Electron capture cross-section for the donor tail state	SIGTDE	5×10^{-15}
Electron capture cross-section for the acceptor tail state	SIGTAE	5×10^{-15}
Hole capture cross-section for the donor gaussian state	SIGGDH	2×10^{-15}
Hole capture cross-section for the acceptor gaussian state	SIGGAH	1.3×10^{-14}
Hole capture cross-section for the donor tail state	SIGTDH	5×10^{-15}
Hole capture cross-section for the acceptor tail state	SIGTAH	5×10^{-15}

Figure 3 shows the comparison of modeled (lines) and simulated (symbols) characteristics I_{DS} *vs* V_{DS} for V_{GS} = 1, 2, 3 and 4 Volts. It can be seen that the model is able to represent the behavior of the drain current at the sub-threshold and above-threshold regions for each curve corresponding to different V_{GS} values with a small error for the whole V_{DS} range.

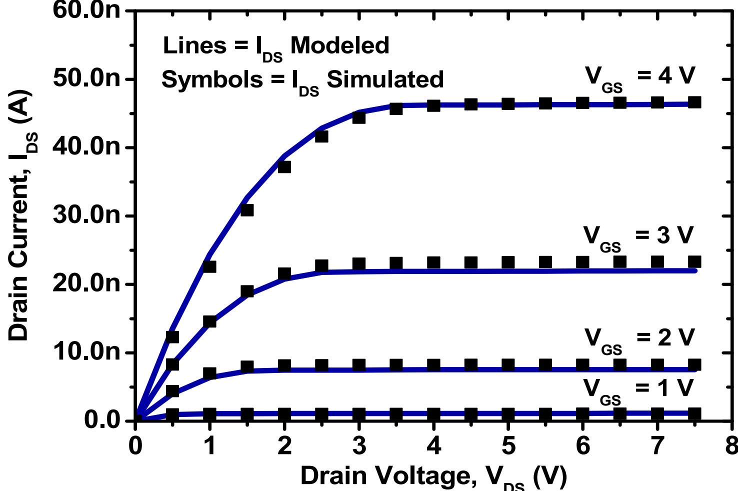

Figure 3. Comparison of modeled and simulated characteristic I_{DS} vs V_{DS} for various values of V_{GS} = 1, 2, 3 and 4 Volts.

Figure 4 shows the absolute and average error between I_{DS} characteristics modeled and simulated presented, which is computed with Equation (33). It can be seen; the maximum absolute error occurs for the I_{DS} curve when V_{DS} = 0.5 V and V_{GS} = 4 V which is 9.8%. In addition, the average absolute error for all values of V_{GS} is 5%, approximately.

$$Error(\%) = 100\left(\frac{abs\left(I_{DS(simulated)} - I_{DS(\text{modeled})}\right)}{I_{DS(\text{modeled})}}\right) \tag{33}$$

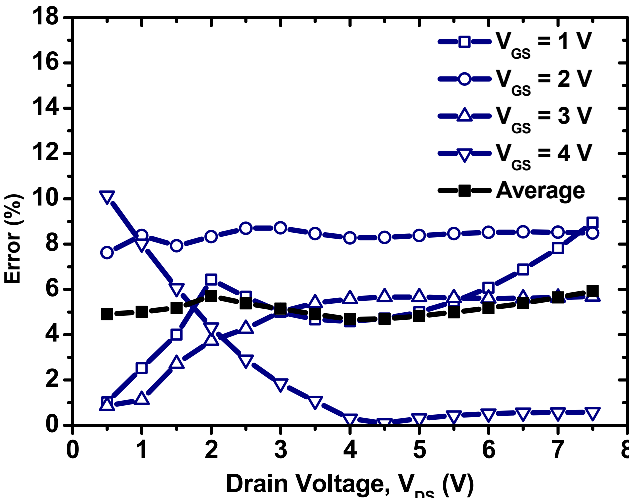

Figure 4. Absolute error computed for each simulated and modeled I_{DS} curve showed in Figure 3 and the average absolute error for all curves.

Figure 5 shows the comparison of the modeled (lines) and simulated (symbols) output characteristics I_{DS} vs V_{GS} for V_{DS} = 0.1, 1, 2, 3 and 4 Volts. It can be seen that there exist a good fit between modeled and simulated I_{DS} curves for both linear (V_{DS} = 0.1 Volts, $V_{GS} > V_{TH}$) and saturation ($V_{DS} > V_{GS} - V_{TH}$, $V_{GS} > V_{TH}$) regions of operation for a-SiGe:H TFT.

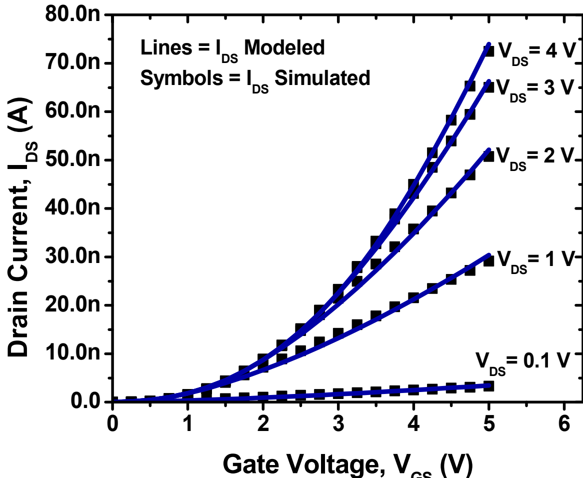

Figure 5. Comparison of modeled and simulated output characteristics I_{DS} vs V_{GS} at V_{DS} = 0.1, 1, 2, 3, and 4 Volts.

4. Conclusions

In this paper, was developed an analytical drain current model for a-SiGe:H TFTs that shows very good agreement with 2D numerical simulations which were used to validate it. The model considers free and localized charges into a-SiGe:H layer, characteristic temperature dependence and is able to work for sub- and above- threshold region of operation with a small absolute average error. In this sense, the proposed model has implication for development and prediction of electrical performance of TFTs at low frequencies based on amorphous semiconductors, such as a-SiGe:H, which is requested for analysis and design of circuits for large area and flexible electronic systems. Future work will include the fabrication and characterization of a-SiGe:H thin films transistors devices.

Author Contributions: S.S.-R., F.L.-H., and J.M.-C. develop the analytic drain current model. S.S.-R. and J.M.-R. made the simulation of thin film transistors using the INAOE fabrication process. S.S.-R., A.L.H.-M., F.L.-H., J.M.-R., and J.M.-C. wrote all the sections of the paper. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

By substituting Equations (7) and (17) in Equation (19), we obtain:

$$I_{\text{DS_sub}} = W\frac{dV_{CH}(\text{y})}{dy}\int_{\phi(\text{x}=t_{sc})=\phi_B}^{\phi(\text{x}=0)=\phi_S} q\mu_0 \frac{N_{free}\exp\left[\frac{q(\phi(\text{x})-\text{V}_{\text{CH}}-\phi_{\text{F0}})}{kT_{free}}\right]}{\sqrt{\frac{2N_{eff}kT_{eff}}{\varepsilon_{sc}}}\cdot\exp\left[\frac{q(\phi(\text{x})-\text{V}_{\text{CH}}-\phi_{\text{F0}})}{2kT_{eff}}\right]} d\phi(\text{x}) \quad \text{(A1)}$$

Then, by integrating for $\phi(\text{x})$ and evaluating from $\phi(\text{x} = 0) = \Phi_S$ to $\phi(\text{x} = T_{SC}) = \Phi_B$, we obtain:

$$I_{DS} = \mu_0 W\frac{dV_{CH}(\text{y})}{dy}\left[\frac{A_{eff}}{B_{eff}}\left[\exp\left[qB_{eff}(\phi_S - \text{V}_{\text{CH}} - \phi_{\text{F0}})\right] - \exp\left[qB_{eff}(\phi_B - \text{V}_{\text{CH}} - \phi_{\text{F0}})\right]\right]\right] \quad \text{(A2)}$$

where:

$$A_{eff} = \frac{N_C}{\sqrt{\frac{2N_{eff}kT_{eff}}{\varepsilon_{sc}}}} \quad \text{(A3)}$$

$$B_{eff} = \frac{1}{kT_{free}} - \frac{1}{2kT_{eff}} \quad \text{(A4)}$$

However, the second term inside of Equation (A2) is neglected ($\phi_B = 0$). Thus, Equation (A2) can be rearranged as follows:

$$I_{DS} = \mu_0 W\frac{dV_{CH}(\text{y})}{dy}\frac{A_{eff}}{B_{eff}}\exp\left[qB_{eff}(\phi_S - \text{V}_{\text{CH}}(\text{y}) - \phi_{\text{F0}})\right] \quad \text{(A5)}$$

By integrating Equation (A5) with respect to y at both sides, and by evaluating the boundary conditions from y = 0 (source voltage, V_S) to y = L (drain voltage, V_D) in order to solve $V_{CH(y)}$, we obtain:

$$\int_{y=0}^{y=L} I_{DS}dy = \mu_0 W\int_{V_{CH}(\text{y}=0)=\text{V}_\text{S}}^{V_{CH}(\text{y}=\text{L})=\text{V}_\text{D}}\left[\frac{A_{eff}}{B_{eff}}\exp\left[qB_{eff}(\phi_S - \text{V}_{\text{CH}}(\text{y}) - \phi_{\text{F0}})\right]\right]dV_{CH}(\text{y}) \quad \text{(A6)}$$

Then, by applying the Gauss's Law along the Metal-Oxide-Semiconductor structure, and by substituting the electric field expression, we obtain:

$$V_{GS} = V_{FB} + \phi_s + \frac{\varepsilon_{sc} \cdot E(\phi(\mathrm{x}))}{C_{ox}} = V_{FB} + \phi_s + \frac{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}{C_{ox}} \cdot \exp\left[\frac{q(\phi_S - \mathrm{V_{CH}(y)} - \phi_{\mathrm{F0}})}{2kT_{eff}}\right] \quad \text{(A7)}$$

where C_{OX} is the capacitance due to gate oxide per area unit, ϕ_s is surface potential at the oxide/semiconductor interface and V_{FB} is flat band voltage.

$$\frac{V_{GS} - V_{FB} - \phi(\mathrm{x})}{\frac{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}{C_{ox}}} = \cdot \exp\left[\frac{q(\phi_S - \mathrm{V_{CH}(y)} - \phi_{\mathrm{F0}})}{2kT_{eff}}\right] \quad \text{(A8)}$$

By rewriting Equation (A8) as function of $\mathrm{V_{CH}(y)}$, we obtain:

$$\log_e\left[\frac{C_{ox}(V_{GS} - V_{FB} - \phi(\mathrm{x}))}{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}\right] = \frac{q(\phi_S - \phi_{F0} - V_{CH}(\mathrm{y}))}{2kT_{eff}} \quad \text{(A9)}$$

$$-\frac{2kT_{eff}}{q} \log_e\left[\frac{C_{OX}}{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}(V_{GS} - V_{FB} - \phi_S)\right] + \phi_S - \phi_{FB} = V_{CH}(\mathrm{y}) \quad \text{(A10)}$$

By differentiating $\mathrm{V_{CH}(y)}$ for $\phi_S(\mathrm{y})$ from Equation (A7), we obtain:

$$\frac{dV_{CH}(\mathrm{y})}{d\phi_S(\mathrm{y})} = \frac{2kT_{eff}}{q} \frac{1}{V_{GS} - V_{FB} - \phi_S} + 1 \quad \text{(A11)}$$

Substituting Equations (A10) and (A11) in Equation (A6), we get:

$$\int_{y=0}^{y=L} I_{DS} dy = \mu_0 W \int_{\mathrm{V_S}}^{\mathrm{V_D}} \left[\frac{A_{eff}}{B_{eff}} \exp\left[q B_{eff}(\phi_S - \mathrm{V_{CH}(y)} - \phi_{\mathrm{F0}})\right]\right] dV_{CH}(\mathrm{y}) \frac{d\phi_S}{d\phi_S} \quad \text{(A12)}$$

$$\int_{y=0}^{y=L} I_{DS} dy = \mu_0 W \int_{\mathrm{V_S}}^{\mathrm{V_D}} \left[\frac{A_{eff}}{B_{eff}} \exp\left[\left(2kT_{eff} \mathrm{B}_{eff} \log_e\left[\frac{C_{OX}}{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}(V_{GS} - V_{FB} - \phi_S)\right]\right)\right]\right]\left(\frac{2kT_{eff}}{q(V_{GS} - V_{FB} - \phi_S)} + 1\right) d\phi_S \quad \text{(A13)}$$

By rewriting Equation (A13), we obtain:

$$I_{DS}(N_{eff}, T_{eff}) = \mu_0 W \frac{A_{eff}}{B_{eff}} \int_{V_{CH}(\mathrm{y=0})=\mathrm{V_S}}^{V_{CH}(\mathrm{y=L})=\mathrm{V_D}} \left[\left[\left[\left(\frac{C_{OX}\sqrt{\varepsilon_{sc}}}{\varepsilon_{sc}\sqrt{2N_{eff} k T_{eff}}}\right)^{2kT_{eff} B_{eff}} (V_{GS} - V_{FB} - \phi_S)^{2kT_{eff} \mathrm{B}_{eff}}\right]\right]\right]\left(\frac{2kT_{eff}}{q(V_{GS} - V_{FB} - \phi_S)} + 1\right) d\phi_S \quad \text{(A14)}$$

Finally, solving Equation (A14), we derive $I_{DS}(N_{eff}, T_{eff})$, which is given by:

$$I_{DS}(N_{eff}, T_{eff}) = \mu_0 W \frac{A_{eff}}{B_{eff}} \left(\frac{C_{OX}\sqrt{\varepsilon_{sc}}}{\varepsilon_{sc}\sqrt{2N_{eff} k T_{eff}}}\right)^{2kTeffB_{eff}} \left[\begin{array}{c} \int_{V_{CH}(\mathrm{y=0})=\mathrm{V_S}}^{V_{CH}(\mathrm{y=L})=\mathrm{V_D}} (V_{GS} - V_{FB} - \phi_S)^{2kT_{eff} \mathrm{B}_{eff}} d\phi_S + \\ \frac{2kT_{eff}}{q} \int_{V_{CH}(\mathrm{y=0})=\mathrm{V_S}}^{V_{CH}(\mathrm{y=L})=\mathrm{V_D}} (V_{GS} - V_{FB} - \phi_S)^{2kT_{eff} \mathrm{B}_{eff} - 1} d\phi_S \end{array}\right] \quad \text{(A15)}$$

$$I_{DS}(N_{eff}, T_{eff}) = \mu_0 \frac{W}{L} \frac{A_{eff}}{B_{eff}} \left(\frac{C_{OX}}{\sqrt{2\varepsilon_{sc} N_{eff} k T_{eff}}}\right)^{C_{eff}} \left[\frac{1}{C_{eff}+1}\left((\delta V_{SD})^{C_{eff}+1} - (\delta V_{SS})^{C_{eff}+1}\right) + \frac{1}{\mathrm{q} \mathrm{B}_{eff}}\left((\delta V_{SD})^{C_{eff}} - (\delta V_{SS})^{C_{eff}}\right)\right] \quad \text{(A16)}$$

where:

$$C_{eff} = 2kT_{eff}B_{eff} \tag{A17}$$

$$\delta V_{SD} = V_{GS} - V_{FB} - V_D \tag{A18}$$

$$\delta V_{SS} = V_{GS} - V_{FB} - V_S \tag{A19}$$

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