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Review

Challenges and Applications of Emerging Nonvolatile Memory Devices

Writam Banerjee

Center for Single Atom-based Semiconductor Device, Department of Material Science and Engineering, Pohang University of Science and Technology (POSTECH), Pohang 790-784, Korea; writam@postech.ac.kr

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Abstract: Emerging nonvolatile memory (eNVM) devices are pushing the limits of emerging applications beyond the scope of silicon-based complementary metal oxide semiconductors (CMOS). Among several alternatives, phase change memory, spin-transfer torque random access memory, and resistive random-access memory (RRAM) are major emerging technologies. This review explains all varieties of prototype and eNVM devices, their challenges, and their applications. A performance comparison shows that it is difficult to achieve a "universal memory" which can fulfill all requirements. Compared to other emerging alternative devices, RRAM technology is showing promise with its highly scalable, cost-effective, simple two-terminal structure, low-voltage and ultra-low-power operation capabilities, high-speed switching with high-endurance, long retention, and the possibility of three-dimensional integration for high-density applications. More precisely, this review explains the journey and device engineering of RRAM with various architectures. The challenges in different prototype and eNVM devices is disused with the conventional and novel application areas. Compare to other technologies, RRAM is the most promising approach which can be applicable as high-density memory, storage class memory, neuromorphic computing, and also in hardware security. In the post-CMOS era, a more efficient, intelligent, and secure computing system is possible to design with the help of eNVM devices.

Keywords: emerging nonvolatile memory; ferroelectric random-access memory; phase change memory; spin-transfer torque random access memory; resistive random-access memory; high-density memory; storage class memory; neuromorphic computing; hardware security

1. Introduction

In the era of advanced technology, electronic memory is an essential element to boost new applications. In general, memory devicesare divided into two broad groups based on the requirement of power to memorize the stored information. One needs constant power to remember the state, referred to as volatile memory (VM). In contrast, another is capable to remember the data without cost of power, referred to as nonvolatile memory (NVM). So far, the need for temporary and permanent data storage is fulfilled by the complementary metal-oxide-semiconductor-based memories, i.e., VM-type dynamic random-access memory (DRAM) and static random-access memory (SRAM) and NVM-type flash memory. The recent progress has experienced the "memory wall", i.e., the speed gap between logic and memory. To overcome the critical system performance bottleneck and fundamental limitations associated with shrinking device size and increased process complexity, emerging NVM (eNVM) with exciting architectures have been proposed. In semiconductor technology innovation, high-performance computing is the driving tool. However, in the era of internet of things (IoT), consumer electronics is moving toward data-centric applications, with new requirements such as ultra-low power operation, low-cost design, high density, highly reliable, longer data storage capability, etc. This review gives an overview of the baseline, prototype, and eNVM devices, with challenges associated with and application

of the same. More precisely, this review explores resistive random-access memory (RRAM) devices with the switching mechanism, device engineering, and applications. Finally, the current-state-of-art eNVMdevices andtheir performance analysis are discussed.

1.1. Background

Figure 1a shows the classification memory devices. Till now, a single memory is not enough to do all things together. In general, SRAM is a fastest one with "*write*"/"*erase*" speed of 100 ps, but the six-transistors-based design takes up a lot of space on wafer. The one-transistor-one-capacitor (1T1C)-based DRAM is an available solution; however, due to the leaky capacitors, the data storage capacity is very much limited. In contrast, the cost-effective, nonvolatile 1T based flash memory is very useful for mass storage applications and holds the biggest share of the semiconductor memory market [1]. Unfortunately, the enormous growth of baseline technologies has experienced the bottleneck of device scaling due to physical limitations. Additionally, flash memory devices suffer with high voltage, low-speed operation, and poor endurance, as compared to DRAM. Highly nonvolatile, scalable, cheap memory technology with ultra-fast, low power, ultra-high endurance and retention capacities are the requirements of next-generation technologies [2]. The need of time has enhanced the research area to find out the suitable alternative NVM [3] which can fulfill the high demand for performance for the regular industrial adoption. As compared to the existing baseline memories, a new technology is expected to be aultra-low-power, high-speed, highly cost-effective scalable device with highly reliable endurance [4]. Apart from the baseline devices, the memories available with prototype test chips or in early production stage is categories as "prototype". In prototype category ferroelectric random-access memory (FeRAM), phase change memory (PCM), magnetic RAM (MRAM), and spin-transfer-torque RAM (STTRAM) are the available options. Figure 2 shows the advantages and disadvantages for all of those baseline and prototype memory technologies from the 2013 International Technology Roadmap for Semiconductors (ITRS) Emerging Research Devices (ERD) chapter [3]. Several factors dominate the adoption of prototype technologies. The performance of the prototype NVM must have to be better if not then at least equivalent to the existing baseline technologies.

Some of the devices from the prototype list are still considered to be emerging technology because of lack of in-depth understanding. The eNVM devices are often explored with novel structure design with new material adoption. In such devices, the novel mechanism is beyond the classical electronic process of silicon devices, which involves quantum mechanical phenomena, redox reaction, phase transition, spin-state, molecular reconfiguration, etc. More importantly, the simple two-terminal eNVM devices provide enough ground to adopt the high-density crossbar architecture.

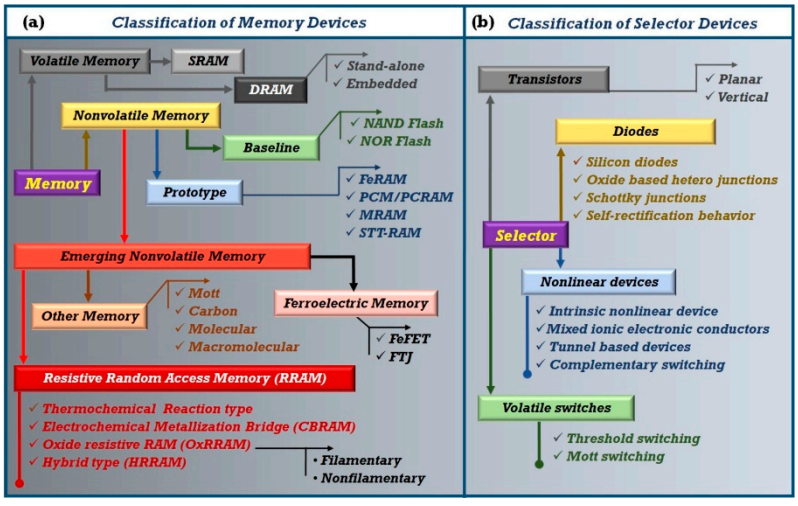

Figure 1. Schematic illustration of the (**a**) classification of memory devices and (**b**) classification of selector devices.

		Baseline technologies					Prototype technologies		
		DRAM		SRAM	Flash		FeRAM	STT-MRAM	PCM
		Stand-alone	Embedded		NOR	NAND			
Memory Type		Volatile Memory			Non-volatile Memory				
Cell Elements		1T1C		6T	1T		1T1C	1(2)T-1R	1T(D)-1R
Feature size F, nm	2013	36	65	45	45	16	180	65	45
	2026	9	20	10	25	> 10	65	16	8
Cell Area	2013	6 F^2	(12-30) F^2	140 F^2	10 F^2	4 F^2	22 F^2	20 F^2	4 F^2
	2026	4 F^2	(12-50) F^2	140 F^2	10 F^2	4 F^2	12 F^2	8 F^2	4 F^2
Read Time	2013	< 10 ns	2 ns	0.2 ns	15 ns	0.1 ms	40 ns	35 ns	12 ns
	2026	< 10 ns	1 ns	70 ps	8 ns	0.1 ms	< 20 ns	< 10 ns	< 10 ns
W/E Time	2013	< 10 ns	2 ns	0.2 ns	1µs/10 ms	1/0.1ms	65 ns	35 ns	100 ns
	2026	< 10 ns	1 ns	70 ps	1µs/10ms	1/0.1 ms	<10 ns	<1 ns	<50 ns
Retention Time	2013	64 ms	4 ms	-	10 y	10 y	10 y	>10 y	>10 y
	2026	64 ms	1 ms	-	10 y	10 y	10 y	>10 y	>10 y
Write Cycles	2013	>1E16	>1E16	>1E16	1E5	1E5	1E14	>1E12	1E9
	2026	>1E16	>1E16	>1E16	1E5	1E5	>1E15	>1E15	1E9
Write Voltage (V)	2013	2.5	2.5	1	8-10	15-20	1.3-3.3	1.8	3
	2026	1.5	1.5	0.7	8	15	0.7-1.5	<1	<3
Read Voltage (V)	2013	1.8	1.7	1	4.5	4.5	1.3-3.3	1.8	1.2
	2026	1.5	1.5	0.7	4.5	4.5	0.7-1.5	<1	<1
T: transistor, C: capacitor, D: diode, R: resistor									

Figure 2. Performance comparison of current baseline and prototype memory technologies [3].

1.2. Prototype Nonvolatile Memory Technology

There are mainly four different kinds of memory devices in this section, i.e., FeRAM, PCM, MRAM, and STT-RAM. Point to note, apart from FeRAM devices, the rest are still very much in research; hence, they can also be considered to be partially prototype or eNVM. However, this review considers all of them as prototype devices, as their prototype chip is well-known. Additionally, all of those technologies are considered to be prototypes by the 2013 ITRS-ERD chapter [3].

1.2.1. Ferroelectric Random-Access Memory

The FeRAM is a prototype nonvolatile NVM based on 1T1C structure [5]. Structurally, both the FeRAM and DRAM designs are very similar. The capacitor material is the major difference among those designs. Unlike the conventional dielectric in DRAM, the nonvolatility of FeRAM mainly depends on the ferroelectric-layer-based capacitor. Generally, as compared to the dielectric constant of DRAM, the dielectric constant of ferroelectric materials is high because of the formation of semi-permanent electrical dipole. The schematic representation of a typical FeRAM cell is shown in Figure 3a. Several types of material engineering have been used to fabricate FeRAM cells. Reports show that there is a huge impact on defect engineering of ferroelectric materials [6]. The switching mechanism of FeRAM devices is driven by the polarization of the ferroelectric capacitor. With an external electric field, the dipoles will be aligned according in the field direction, resulting in a small shift in the atomic positions. Simultaneously, a shift in electronic charge distribution will be obtained in crystal structure. After the removal of the field, the dipoles are memorized by the polarization state, as shown in the schematic hysteresis behavior depicted in Figure 3b.

Digitally, the electric polarization states can be denoted as 0 or 1. Though the basic functionality is similar to DRAM, in FeRAM, destructive reading is the major disadvantage. Compared with DRAM, the FeRAM is highly nonvolatile, as it can retain stored information for 10 years, with long endurance of $>10^{14}$ cycles. As compared to NAND flash memory, FeRAM is faster, with a write and read speed of 65 and 40 ns, respectively. A typical NAND flash can be operated at 15 V to write and 4.5 V to read, but FeRAM can work only at 3.3 V to write and 1.5 V to read. Even after several advantages over the baseline memories, FeRAM has major scalability problems. The smaller the cell size is, the less

space it takes up on the silicon wafer, thus increasing the device yield at a low cost. Several companies, including Ramtron and Texas Instruments, are producing FeRAM at a large scale and also investing in research for the improvement of scalability in FeRAM technology.

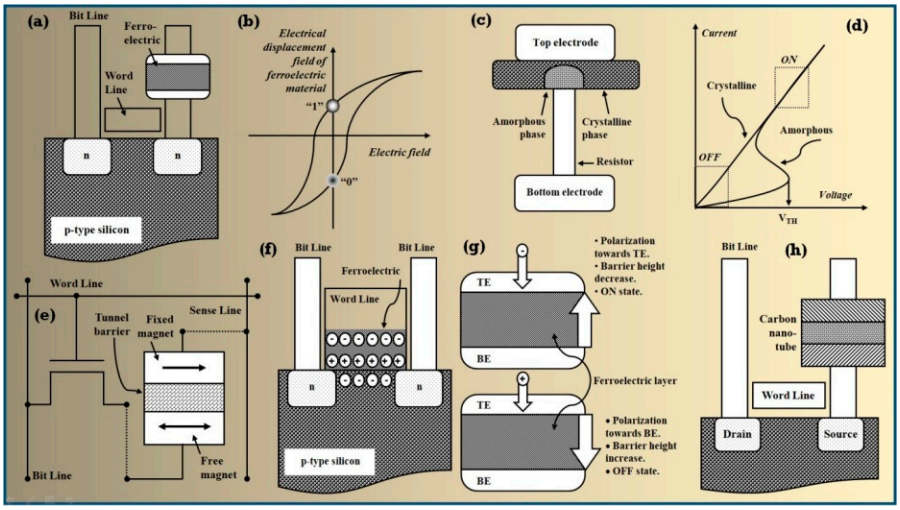

Figure 3. Schematic illustration of the (**a**) ferroelectric random-access memory (FeRAM) device structure and (**b**) the hysteresis behavior; (**c**) the structure of phase change memory (PCM) and (**d**) the I–V switching, (**e**) spin-transfer-torque RAM (STTRAM) structure, (**f**) ferroelectric field effect transistor (FeFET) design, (**g**) ferroelectric tunnel junction (FTJ) structure, and (**h**) carbon nanotube (CNT)-based carbon memory device structure.

1.2.2. Phase Change Memory

PCM is an NVM, mainly based on chalcogenide glass, and is sometimes referred to as CRAM. The switching in PCM is based on the presence of two different solid-state phases, i.e., crystalline and amorphous with different electrical resistivity. The information-storing ability in PCM is provided by the transition between the low resistive crystalline phases to high resistive amorphous phase [7]. The transition from amorphous to crystalline phase is the speed-determining step, known as SET switching. Reverse transition from crystalline to amorphous phase is the power-limiting process which is known as RESET switching. The schematic representation of a simple PCM cell is shown in Figure 3c. Generally, due to high processing temperature, a post-fabrication PCM cell is in crystalline phase with a low resistance state (LRS). The external electrical current pulse for a shorter period of time can RESET to a high resistance state (HRS) and switch the PCM from crystalline to amorphous phase. To restore the crystalline phase by SET switching, a medium electrical current pulse between the crystallization and melting temperature, with a sufficiently longer period of time to crystallization, is needed. Figure 3dshows the typical current–voltage (I–V) curves of the PCM cell. Both the SET and RESET curves are superimposed once the device is ON, whereas a gap is present at the OFF region due to phase transition, which allows a small amount of read voltage to perform read operation. So far, the switching mechanism of Ge-Sb-Te (GST)-based PCM devices has been studied thoroughly.

PCM is a faster device as compared to the flash technology [8]. Typically, a PCM can be operated with high speed of 100 ns, with lower operating voltage and better endurance capabilities than flash memories. Memory giants like IBM, Infineon, Samsung, and Macronix have demonstrated prototypes of PCM chips and have further promoted the mass production with three-dimensional cross-bar arraysby collaborations between Intel and Micron. However, research is ongoing to simplify the processing of PCM, to optimize power efficiency, to reduce RESET current, and to lower the switching power. To date, PCM devices possess a nanometer-scaled phase transition, longer retention and endurance at smaller dimensions, high power efficiency using thinner films, scaling of threshold

voltage (V_{TH}), etc. However, the PCM cell size very much limited by the selector devices such as bipolar junction transistor (BJT), vertical transistor, and even diode.

1.2.3. Spin-Transfer Torque Random Access Memory

STTRAM is a type of MRAM which is based on magnetic tunnel junctions (MTJs) [9], with the configuration of 1T1MTJ, as shown in Figure 3e. In MTJ, two ferromagnetic (FM) layers—one has fixed magnetic orientation, and the other has free magnetic orientation—are usually separated by a tunnel oxide barrier. The parallel magnetic orientation of both FM layers (typically 1–2 nm MgO) is the LRS of the cell, and the anti-parallel magnetic alignment switches the cell in HRS. As compared to typical MRAM design, STTRAM has high scalability, simple architecture, lower power consumption, and faster operation.

The writing speed of STTRAM is faster than flash, FeRAM, and PCM technology. The endurance of STTRAM (>10^{12} cycles) is much better than flash and PCM, with good data retention properties. A 64MB with 90 nm CMOS-process-based STTRAM device is already in its early commercialization stage [10]. Everspin and Buffalo Technology are actively taking part for the production of STTRAM. The STTRAM chip can be used for embedded and standalone devices, as claimed by Avalanche. STTRAM technology is still facing some critical challenges, like small ON/OFF tunneling magneto-resistance ratio, well-designed read scheme, selector dependent critical size, size and current scaling without effecting thermal stability, etc. To improve those critical needs, research in this topic is still in progress. The recent progress in spintronic gives some light to this technology; for instance, a small electric bias induced a large change in magnetic anisotropy, i.e., voltage-controlled magnetic anisotropy in Fe(001)/MgO(001) junction may reduce the switching power of STTRAM, and a giant spin hall effect in heavy metals may improve the reliability of STTRAM.

2. Emerging Nonvolatile Memory Devices

In this group, several devices are available. Generally, the mechanisms of eNVM devices are beyond the conventional mechanism of baseline devices. So far, the performances of the eNVM devices are inbetween storage and memory. A high-performance eNVM can act as storage class memory which can mitigate the gap between storage and memory devices like NAND flash and DRAM. A comparison of eNVM devices is shown in Figure 4.

Memory Type	***Emerging Ferroelectric***		***Carbon***	***Mott***	***Macro-molecular***	***Molecular***
Subclass	***FeFET***	***FTJ***				
Storage mechanism	Remnant polarization on a ferroelectric dielectric	Giant tunnel electro-resistance	Multiple mechanisms	Multiple mechanisms	Multiple mechanisms	Multiple mechanisms
Cell Elements	1T	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device type	FET with FE gate insulator	M-FJT-M M-FJT-Semi-conductor	Nanotube, amorphous carbon, graphene	Mott transition	M-I-M(NC)-I-M	Bi-stable switch
Advantages	Excellent endurance. Scalability.	Large ON/OFF ratio. High speed, low power.	Scalability.	High speed switching. Low write energy.	Control over structure. Simple processing.	High scalability. Low switching energy.

Figure 4. Advantages of different emerging nonvolatile memory (NVM) technologies [3].

2.1. Emerging Ferroelectric Memory

Emerging FeRAM is a major eNVM technology which is subdivided into two categories: ferroelectric field effect transistor (FeFET) [11] and ferroelectric tunnel junction (FTJ) [12,13]. As compare to the conventional 1T1C design of FeRAM, the structural design of FeFET is very simple based on 1T structure with a ferroelectric-material-based gate oxide, as shown in Figure 3f. Under a positive bias on top electrode, the polarization in FeFET devices will be in a downward direction. In such

situation, the channel will be under inversion mode, which leads to the low the resistance and ON state. In reverse action, by applying negative pulse on the top electrode, the upward polarization will make OFF state with high resistance, as the channel will be in depletion mode. Hence, the device is completely field-driven at the transistor gate, with minimal leakage current, leading to low power switching. In a simple way, the concept of FeFET is similar to flash memory, where data storage is performed by ferroelectric polarization. The switching speed of FeFET is as fast as 20 ns. However, several key challenges, like endurance, retention, write/erase disturbs, and CMOS process integrations, are still critical for FeFET technology.

Figure 3g shows the basic structure of an FTJ. An external electric field is essential to polarize the ferroelectric layer. Applied negative voltage on the top electrode will direct the polarization toward the top, and the resulting average barrier height will be lowered, thus producing a high current and ON state. In contrast, the direction of the polarization will be reversed with a positive voltage on the top electrode. In this situation, the average barrier height will be increased and will block the current flow, resulting in an OFF state. As compared to conventional FeRAM devices, the non-destructive readout is a major advantage of the FTJ; however, endurance and retention are still problematic.

2.2. Memory Devices with Various Mechanisms

2.2.1. Carbon Memory

If an eNVM is based on carbon nanotube (CNT), amorphous carbon, and graphene, then, in general, that device refers as carbon memories sometime as nano-RAM (NRAM). The concept of NRAM was first proposed by Nantero [14]. The cell of NRAM consists of 1T1R or 1D1R, as shown in Figure 3h. In the CNT-based devices, the contact between CNTs can define the ON and OFF states of the device. Under suitable biased conditions, the device will be in the ON state if the CNTs are in contact; in reverse, the device will be in the OFF state if the CNTs are not in contact. However, the carbon-based technology is not matured, as the physics behind this technology is not yet understood properly.

2.2.2. Mott Memory

Based on the principle applications of Mott insulators, a Mott Memory is designed. The materials which can go through the metal-to-insulator transitions are especially useful to this kind of applications [15]. The electronic–structural phase changes in the complex oxide thin films can develop the memory phenomena.

The Gibbs-free-energy-modulation-based working principle is the driving force of writing and reading operations of the Mott memory devices, as illustrated in Figure 5. With external stimulation, the initial stable phase, i.e., state "0", can be broken by a phase transition process, and the system goes through to the metastable phase, i.e., state "1". One can consider that the system resistivity can undergo a transition from an insulating to a metallic phase. Hence, the stability of the state depends on the kinetics of the phase transition. If the kinetic energy barrier is higher than the thermodynamic driving force, the device can experience a stable metastable state "1", and the memory behaves as eNVM one (Figure 5d). In reverse, for a small kinetic energy barrier, the memory behaves as VM one (Figure 5e). The behavior is also thermally dependent. It is also possible to realize VM and NVM operations within a single material system in optimized temperatures. As compared to DRAM and SRAM memories, the major advantage of Mott memories is its two-terminal design with cross-point array with $4F^2$ cell area size (F is the minimum chip feature size) with faster Mott transitions than Flash. The demonstrated write energy per transition is sub-100 fJ in a Mott memory, which can be further scaled down with area scaling.

2.2.3. Macromolecular Memory

Macromolecular materials, such as polymers, have a huge impact on the design of eNVM and are generally known as macromolecular memory or organic memory. A macromolecule is a

very large molecule with high atomic density, and it is typically composed of 10^2 to 10^3 atoms or more. In this category, several materials, such as synthetic and biological polymers, polyelectrolytes, etc., are available. Point to be noted, CNTs and graphene also can be considered as macromolecules. In this kind of eNVM device, mainly carbon atoms or sometimes silicon atoms are connected in a chain. By incorporating hydrogen or other hetero atoms, such as oxygen, nitrogen, and sulfur, the chemical structure can be modified. Macromolecular memory can be fabricated by using different structural designs, such as single-layer or multilayer macromolecular memory and defect engineered (with or without nanocrystals (NCs)) macromolecular memory. To reduce fabrication cost, this type of memory can be fabricated by using printing technology and is mechanically very flexible, with the potential for device scaling.

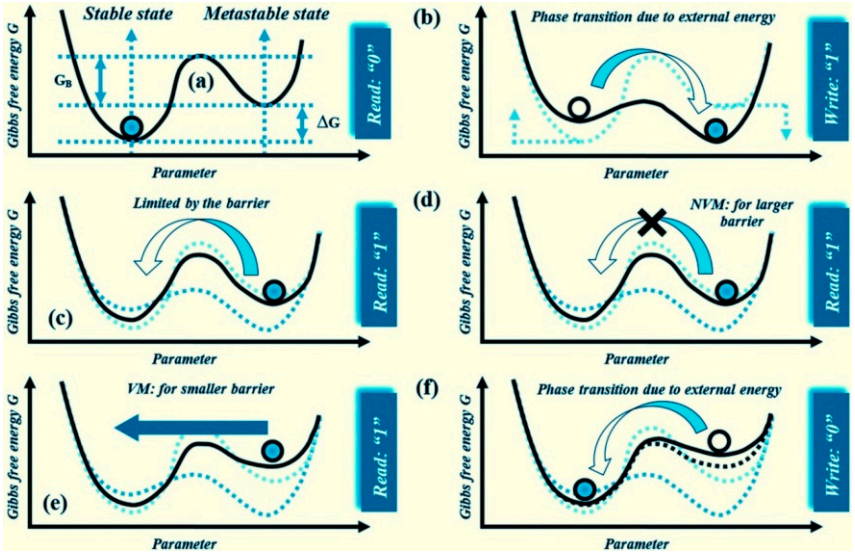

Figure 5. (**a**) Illustration of Gibbs free energy variation of stable phase (state "0") and metastable phase (state "1") of a typical Mott memory under writing and reading operations. Stable phase is at the equilibrium system at constant temperature, where ΔG is the free energy difference between state "0" and state "1". (**b**) The external energy driven phase transition from state "0" to state "1". (**c**) In state "1", after the writing signal removal an energy barrier (G_B) will be faced by the system. (**d**) Before the transition from "1" to "0", the system will behave as NVM if the energy barrier is large. (**e**) If the energy barrier is small, the system can behave like VM. (**f**) For the transition from "1" to "0", another external signal is necessary.

2.2.4. Molecular Memory

In general, a molecular memory is designed with a top electrode/molecule layer/bottom electrode structure. Due to easily understood redox behavior, the redox-active molecules are grabbing much attention to develop this technology. However, the molecular memory devices still need much attention, as the data storage mechanism can be varied with structure design such as redox-active molecular memory, solid-state molecular memory, nano-wire- or nano-tube-based molecular memory, etc.

A performance comparison of emerging FeRAM and other eNVM devices is shown in Figure 4. Although several eNVMs are driving in the research sector, the adoption of new memory is very much depending on several performance factors, such as scalability potential, speed, energy efficiency, ON/OFF ratio, reliability, thermal stability, CMOS technology compatibility, CMOS architectural compatibility, and cost effectiveness. Among those emerging devices, resistive random-access memory (RRAM) is the most promising eNVM for next-generation electronic devices, as shown in Figure 6. The performances of the prototype and emerging NVM are summarized in Figure 7 [16].

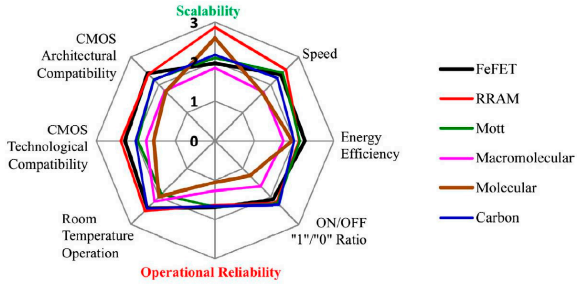

Figure 6. As compared to other devices, RRAM is showing better performance. (Reproduced from [Solid-State Electron. 2016, 125, 25–38], with the permission of Elsevier Publishing [2].)

	Prototypical Memories			*Emerging Memories*					
Parameters	*Fe-RAM*	*STT-MRAM*	*PC-RAM*	*Emerging ferroelectric*	*Nano-mechanical Memory*	*Redox Memory*	*Mott Memory*	*Macromolecular Memory*	*Molecular Memory*
Scalability	☹	😐	☺	😐	☹	☺	?	?	☺
MLC	☹	☹	☺	☹	☹	☺	?	😐	☹
3D Integration	☹	😐	☺	☹	☹	😐	?	☺	☹
Fabrication cost	😐	😐	☺	😐	☹	😐	?	☺	?
Endurance	☺	☺	😐	☺	☹	☺	😐	☹	?

Symbol	*Scalability*	*MLC*	*3D Integration*	*Fabrication cost*	*Endurance*
☹	F_{min} > 45 nm	*Difficult*	*Difficult*	*High*	< 1E5
😐	F_{min} = 10-45 nm	*Feasible*	*Feasible*	*Medium*	< 1E10
☺	F_{min} < 10 nm	*Solution anticipated*	*Difficult*	*Potentially low*	>1E10

Figure 7. Performance comparison of prototype NVM and emerging NVM technologies [16].

3. Resistive Random-Access Memory Devices

As compared to the prototype NVM devices for the next-generation memory applications, the merging RRAM is one of the most promising technologies, as shown in Figure 8a. In RRAM, the repeated change of the internal resistance state allows users to store information. As compared to the other technologies, RRAM devices have several advantages. Due to the high endurance of $>10^{12}$ cycles with speed <1 ns, RRAM is a potential alternative to the DRAM technology [17–19].

As compare to flash devices, RRAM can work with 1 V [20], with a scaled structure down to <5 nm [21]. In a simple form, RRAM is a two-terminal element with metal–insulator–metal (M–I–M) stack in which the resistance state can be varied from a high resistance state (HRS) to a significantly low resistance state (LRS) or viceversa. The two metal layers are top electrode (TE) and bottom electrode (BE) of RRAM. Depending on the design, requirements, and the type of RRAM, the metal layer can be inert or active materials. Verity of materials are being explored as the resistive switching (RS) insulating layer, such as, binary/multinary oxide [22–26], chalcogenides [27,28], and organic compounds [29,30], along with the defect engineering structures (Figure 8c). The basic structure of RRAM with crossbar design is shown in Figure 8b. The two-dimensional crossbar RRAM array with a simple design provides integration facility with a small size of $4F^2$ [31,32]. The three-dimensional (3D) architectures can further increase the density of the RRAM array with increasing stacking layers [33,34], with reduced size to $4F^2/n$, where n is the number of stacking layer. In general, a typical as-prepared RRAM cell maintains an HRS, which can be changed by an initial formation process with applied bias with suitable current compliance (I_{CC}). The forming voltage is usually high as compared to the operating voltage during RS process. The ON transition from HRS to LRS is known as the SET process, and the RESET process is the OFF transition from LRS to HRS.

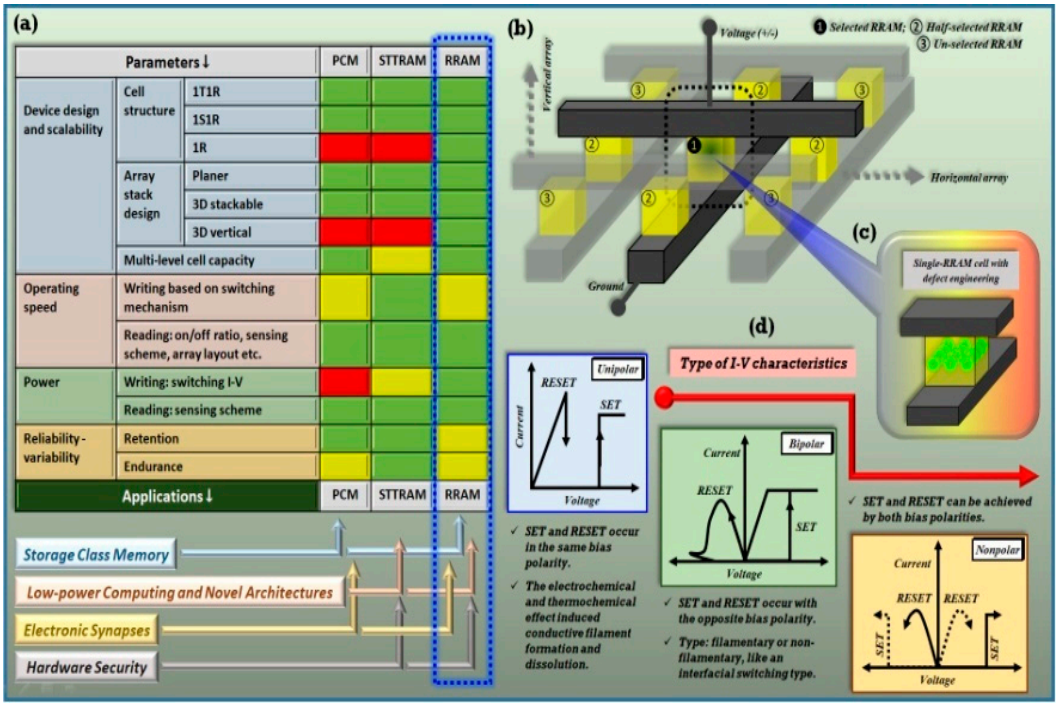

Figure 8. (**a**) Illustration of major emerging nonvolatile memory devices and applications. Major emerging NVM devices are PCM, STT-RAM, and RRAM; however, the PCM and STTRAM technologies are also considered as prototype memory. Among those alternatives, RRAM is a promising candidate in the field of memory, novel architecture, neuromorphic computing, and in security. (**b**) Schematic of a 3 × 3 array of cross-bar RRAM devices, with ① selected one under biasing condition only, ② half-selected cells, and ③ unselected cells. (**c**) A single RRAM cell also can be constructed with defect engineering. (**d**) The general I–V characteristics of RRAM cells.

Depending on I–V characteristics, the RS can be three types, i.e., unipolar switching, bipolar switching, or nonpolar switching, as illustrated in Figure 8d. Unipolar switching is based on the thermochemical-effect-induced conductive filament formation and dissolution process, in which SET and RESET occur under the same direction, with an advantage of high resistance ratio (HRS/LRS). However, high RESET current, poor uniformity, and low reliability are the key challenges of unipolar switching. In bipolar switching, the SET and RESET occur with the opposite bias polarity with the RS process, either filamentary or non-filamentary. The nano-ionic redox effect is the key of RS in filamentary RRAM. So far, a higher endurance (>10^{12}) and higher operation speed (<1 ns) are demonstrated for bipolar RRAM as compared to unipolar devices. In the non-filamentary RRAM device, control of the tunneling barrier is the key parameter, where RS takes place due to the change in tunneling mechanism near the interface of metal and insulator. Generally, non-filamentary RRAM devices are forming-free in nature with uniform switching behavior, as compared to the filamentary device. Though the performance of the RRAM cell is satisfactory, the large-scale array faces several problems, including sneak leakage paths. Device nonlinearity factor "$nonlinearity = \frac{I \times V_R}{I \times \frac{1}{2} V_R}$", which is the ratio of current at read voltage (V_R) to the current at half of V_R, is an important parameter to achieve high-density memory. Selector devices are therefore essential for large-scale crossbar array integration. In general, for the non-filamentary RRAM nonlinearity is good as compared to the filamentary RRAM, but the retention behavior needs further optimizations.

3.1. Journey of Resistive Switching Memory and Evolution of Structural Design

The historic discovery of a large negative differential resistance was observed in five anodic oxide materials, SiO_x, Al_2O_3, Ta_2O_5, ZrO_2, and TiO_2, by T. W. Hickmott, in 1962 [35]. The similar phenomena have been observed in the following years [36,37]. A few years later, in 1967, Simmons et al. [38]

and Varker et al. [39] had indicated the possible application of RS in memory technology. Over time, several materials and systems have been studied to perform RS and to understand the physics behind the switching. PagniaandSotnik [40] has reviewed the development of RS up to the mid-1980s. In the quest of finding an alternative to silicon-based memories, RS technology became the attractive area of research from the late 1990s. In 1998, the first patent of RS based on the active metal ions was published by M. N. Kozickiet al. [41]. Although from late 1960s to the beginning of the 21st century, several reports had identified the possible applications of RS [42], in 2002, Zhuang et al. [43] reported the first practical application of RS in a fabricated 1T1R 64bit RRAM array based on $Pr_{0.7}Ca_{0.3}MnO_3$, using a 0.5 µm CMOS process line. In 2004, Samsung Electronics reported binary transition-metal-oxide-based RRAM integrated with 0.18 µm CMOS process [22]. The RRAM device promises high performance with good SET/RESET cycles of 10^6 and read cycles of 10^{12}, along with the capability to function even at 300 °C. The architectural development of RRAM was started from the same year, by introducing the crossbar design by T. Sakamoto et al. [44]. The simple two-terminal crossbar design became the boost for the RRAM technology. Parallel to the structural development, scientists put efforts to improve the device performance and also to understand the basic device physics. A detail study of $SrTiO_3$-material-based RRAM device was published in 2006, by a group of researchers from ForschungszentrumJulich, Germany [45]. In 2008, the Industrial Technology Research Institute, Taiwan [46], reported the possibility of high temperature multilevel operation in HfO_x-based RS with 1T1R memory cell integrated with 0.18 µm CMOS technology, showing the possibility of high-density memory.

A simple two-terminal structure of RRAM provides a huge opportunity to invent novel and advanced architecture. New structure engineering with 3D horizontal or vertical crossbar design put forward RRAM technology for high-density applications. The crossbar is a useful architecture which is basically the fourth fundamental passive circuit element named as memristor (memory-resistor), which was invented in 1971, by Leon Chua [47]. Later on, in 2008, a group of scientists from HP Labs researched the existence of RS behavior in a simple $Pt/TiO_2/Pt$-based memristor structure [48], which is the most promising design due to its inherent $4F^2$cell size and 3D integration possibilities for mass storage devices. In 2009, ultra-high-density vertical RRAM was reported by H. S. Yoon et al. [49]. In the same year, high-κ Ta_2O_5-based RRAM with an ultra-low current operation of 5 pA was reported [50]. Using an advanced nano-injection lithography technique, in 2010, the National Nano Device Laboratory, Taiwan, addressed the scalability potential of a sub-stoichiometric WO_x-based RRAM below 10 nm [51]. Along with the technological developments of RRAM, the theoretical understanding has been developed equally [52–59].

Technological development of RRAM devices is very limited by proper understanding of the composition, structure, and dimensions of switching filament/s. It is also reported that the scalability potential of active metal-ion-based filament can hit the atomic limit. Previously, SET/RESET characteristics [60], effect of switching parameters [61], switching mechanism [62], filament structure, and growth [63] processes were studied in detail. D. H. Know et al. [64] reported the atomic structure of the conductive nanofilament in TiO_2-based RS devices. The unprecedented development of RRAM scaled down the RESET current to 23 nA for a nitrogen-doped AlO_x RRAM device with 1T1R structure [65], in 2011, and the endurance of RRAM hit over 10^{12}program/erase cycles for a RS device, which was based on a bilayer TaO_x material with a 30×30 nm^2 crossbar structure, reported by Samsung Electronics [18]. The device was equally capable of switching with a 10 ns RESET and SET pulses. In January 2012, "Elpida Memory" announced a prototype RRAM based on 50 nm process technology with a capacity of 64 Mbits [66]. In the same year, Panasonic launched its Ta_2O_5 based 1T1R RRAM cell integrated with 0.18 µm CMOS technology [67]. The scalability of RRAM devices has been demonstrated at the ultimate scalability potential with a feature size of 5 nm [68]. In 2015, 3bit per cell storage capacity was achieved for a TaO_x-based RRAM [69]. Ultra-low-power RRAM for 3D vertical nano-crossbar arrays was reported by Q. Luo et al. in 2016 [33], based on HfO_2/CuGeS structure. In the next few years, graphene and 2D materials grabbed attention to develop the RRAM

technology [70–72]. In recent years, the controllability of metallic-Cu-atom-based filament in RS devices scaled down to single atomic level with 6bits of storage capacity [73]. Moreover, several other effects, like ferromagnetic, optical, and superconducting properties, combined with RRAM have been reported [74–76]. The further development of RRAM technology is boosting the new applications like brain-inspired computing, hardware security, and internet of things (IoTs).

A schematic illustration of material engineering of RRAM devices is shown in Figure 9. The complete stack can be engineered by various methods. For the electrode layer, the consideration of several factors, like work function, free energy of oxidation, thicknesses, etc., is important. The insulating layer can be designed as a single-layer, multiple-layer, or with defect engineering. The impact of unwanted interfacial layer between metal and oxide layers can be avoided by inserting an additional interfacial layer, which can improve the adhesion and mechanical stability and stabilize the local oxygen migration. Several systems are involved in this kind of structure engineering, such as atomic layer deposition (ALD), physical vapor deposition (PVD), pulsed laser deposition (PLD), chemical vapor deposition (CVD), oxidation processes, sol-gel technique, etc.

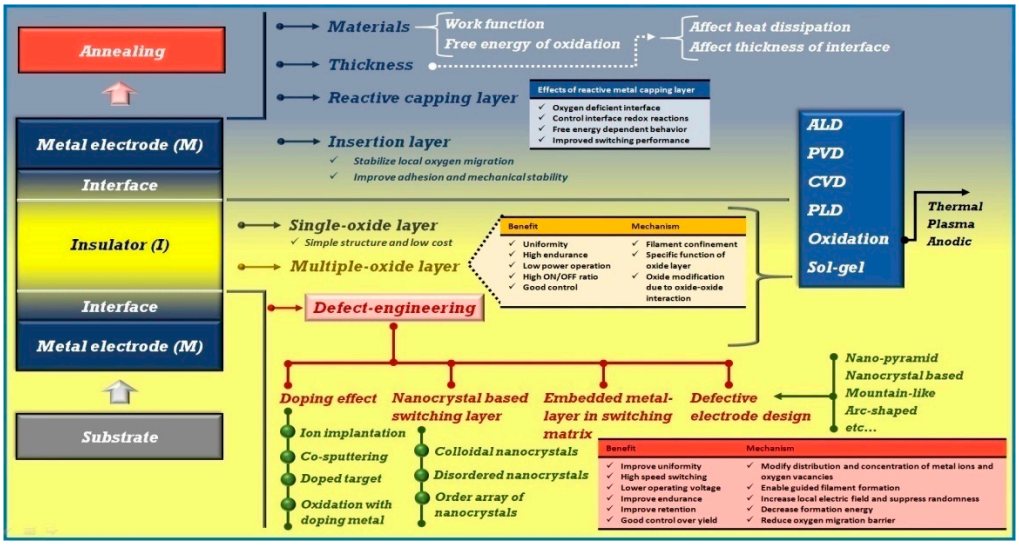

Figure 9. Illustration of material engineering and useful systems to design RRAM devices.

3.2. *Different Types of Switching in RRAM Devices*

Based on switching mechanisms, the RRAM devices can be categorized into several groups [77]. The physics behind the switching process in RRAM not only depends on the materials but also on the device fabrication process, systems, and device operation. Among several types of RRAM devices, the electrochemical metallization (ECM) type, valance change memory (VCM) type, and thermochemical reaction type are mostly investigated. Due to excellent power scaling onto few-pW level, superior scalability of filament up to atomic level, with simple fabrication process steps, the ECM and VCM devices are the center of attraction of research.

3.2.1. Electrochemical Metallization Type

In ECM, one electrode material must be an active electrode (AE), and the other is inert or a counter electrode (CE). Cu and Ag metals are usually used for AE. Based on cation migration process, the formation and rupture of the conductive filament (CF) is the switching principle of ECM devices. Under biased condition, the mobile ions, like Cu^{2+} or Ag^{+} from AE, directly participate in the RS event. The CF forms via electrochemical dissolution process from AE and finally re-deposits on the CE. Due to the metallic-bridge-based filament formation, the ECM device is also known as conductive bridging RAMs (CBRAMs), programmable metallization cells (PMCs), or gapless-type atomic switches [78–82]. In 1976, Y. Hirose et al. [83] reported the optical microscopic evidence of ECM switching. In ECM,

although Cu and Ag are the standard AE materials, there are several other options available such as Ni [84], Al [85], Ti [86], Zn [87], Nb [88], Au [89], etc. However, till now, Ag and Cu have mostly been used as AEs due to their physical advantages, e.g., Ag^+ and Cu^{2+} can electrochemically dissolve very easily because the standard electrode potentials for Ag^+ (0.8 V) and Cu^{2+} (0.34 V) are much smaller as compared to the other metals, like Pt^{2+} (1.19 V), Au^+ (1.83 V), etc. Additionally, the standard Gibbs free energy of formation of oxides for Ag and Cu is much lower than other metals, like Ir, Pt, Ni, etc. According to the classical ECM theory, the growth process of metallic filament depends on three consecutive steps. Considering M as metal atoms and M^{z+} as metal ions, we get the following:

- In AE, i.e., anode side, the oxidation reaction will take place ($M \rightarrow M^{z+} + Ze^-$).
- Electro-migration of M^{z+} ions from anode to cathode, i.e., CE direction.
- On top of CE, the reduction of M^{z+} ions forms metal atoms ($M^{z+} + Ze^- \rightarrow M$). This is the nucleation process followed by the growth mechanism.

After the growth process, the complete formation of metallic-filament can conduct the RS event. However, for different material systems and structure of the ECM cell, the growth direction of filament can be different. Depending on the material of the system, there are several ECM devices, such as solid-electrolyte-based ECM, oxide-electrolyte-based ECM, organic-electrolyte-based ECM, etc.

In the solid-electrolyte-based ECM, the RS follows the classical theory of ECM. The conventional ECM devices can be designed with H_2O [90,91], Ag-Ge-Se [92,93], Ag_2S [94], GeTe [95], GeS [96], etc. In the solid-electrolyte-based ECM devices, the filament growth direction is from CE to AE. The typical I–V characteristics of an ECM device based on Ag/Ag-Ge-Se/Pt structure is shown in Figure 10a. The as-fabricated device is in OFF state. Under a positive bias on AE, an oxidation process will take place at AE, and the Ag^+ ion will start to move toward the CE. The reduction process will take place at CE. The Ag nuclei will start to form on CE, followed by a growth process of the filament from CE to AE side, resulting in ON current. A negative bias on AE will break the filament and RESET the device. As compared to the conventional solid electrolytes, the oxide electrolytes have lower solubility and diffusion coefficients of metal ions. The metal ion flux in a particular electrolyte system is the determining parameter of the ionic conductivity. The Cu ion flux is 10 orders of magnitude lower in the oxide electrolyte, as compared to the solid electrolyte systems; hence, the ionic conductivity in oxide electrolyte is lower than the conventional electrolyte systems. In oxide-electrolyte-based ECM, the growth direction of filament is from AE to CE. The similar filament growth direction can be observed in the organic-electrolyte-based systems [97].

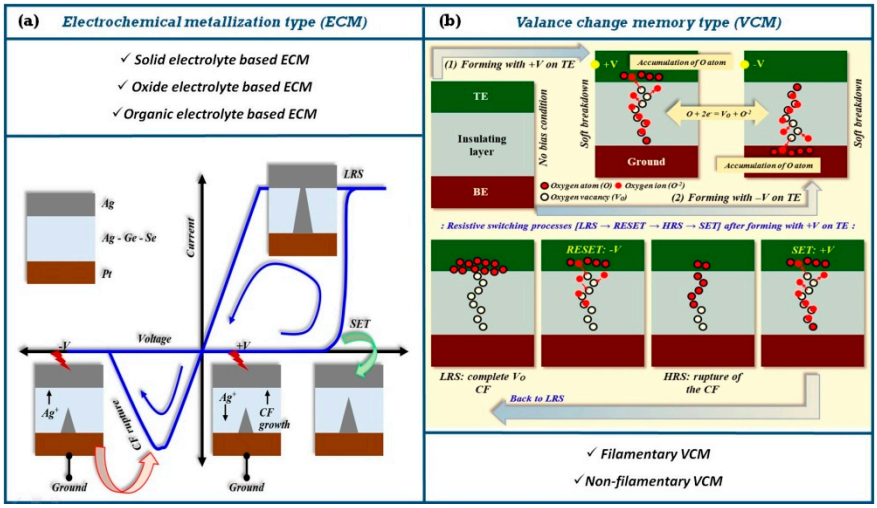

Figure 10. (**a**) Schematic I–V characteristics of electrochemical metallization (ECM) device with switching mechanism in conventional solid-electrolyte-based devices. (**b**) Illustration of the filamentary switching mechanism in VCM devices.

3.2.2. Valance Change Memory Type

Generally, the transition metal oxides with inert type of metal electrode are suitable for VCM type devices. The oxygen vacancy (V_O)-type defects are the driving element of this kind of devices. In the VCM-type system, the inert electrode materials are not easily oxidized, such as Pt, Au, Ir, etc. Usually, the other electrode material is an oxygen-scavenging layer, like Ti. Several oxide materials, like TiO_x [98], NiO_x [99], HfO_x [100], TaO_x [101,102], AlO_x [103,104], WO_x [105], and nitrides such as AlN [106] and NiN [107], have been studied rigorously. In those systems, due to field-driven migration of positively charged V_O or nitrogen vacancies (V_N), the valence of oxides or nitrides will be changed. A VCM system can be can be classified as filamentary switching and interface switching.

In filamentary VCM devices, the RS event takes place due to the formation of vacancy-based filament. Figure 10b shows the schematic illustration of the filamentary switching mechanism in VCM. Under a positive voltage on TE, the oxygen ions drift toward the top interface and accumulate if the TE is made by inert metal like Pt; however, for oxidizable metal like Ti, the non-lattice oxygen ions will form an interfacial oxide layer. In any case, the TE/insulator interface will behave like an oxygen reservoir. The process conducts the initial soft breakdown due to a high electric field, and this is known as the forming process. Generally, the voltage required for the RS event is lower than the forming. The size and thickness of the filament can increase or decrease with the increasing or decreasing current compliance. In non-filamentary-type VCM devices, the tunnel barrier thickness modulation is the key of the switching process [107,108]. In general, the ON/OFF ratio in non-filamentary devices is lower than the filamentary VCM. In contrast, the switching stability is much better in non-filamentary VCM devices.

3.2.3. Defect Engineering of Resistive Memory Devices

The performances of RRAM devices are impressive, with a highly scalable design, low power consumption, and high endurance and retention behavior [109–111]. However, the improvement of performance was not so straightforward. Defect engineering is playing a key role in this development [112]. Defect engineering can be several types, such as doping engineering, nanocrystal-based design, embedded metal layer, defective electrode design, etc. Previously, the improvement of RS properties in Al_2O_3 was done by Cu doping [113], nitrogen (N) doping. The improvement in the uniformity of RS cycles with forming-free structure has been achieved with the N-doping in a Ta/TaO_x/Pt RRAM device [114]. By controlling the doping % of the device, a good RS property has been achieved with a 3–6% N-doped TaO_x RRAM. The doping can effectively confine the filament formation in the localized region and improve the stability of the switching. The Ti-doped improvement of Cu/ZrO_2: Ti/Pt RRAM structure was reported by Q. Liu et al. [115], with a narrow distribution of the SET/RESET voltages and also in HRS/LRS resistances. Previously, a large amount of metal doping in RRAM devices has been reported [116]. The defects can be done by using nanocrystals (NCs). RRAM devices based on different kind of NCs, such as Ru-NC [117], IrO_x-NC [103], TiO_2-NC [118], CdS-NC [119], and Au-NC [120], have shown the improvement over the controlled one. The inserting of NCs can affect the switching mechanism in several ways, e.g., it can improve the internal electric field, which is beneficial for the localized filament formation; the migration of NCs can form conductive filament by mass transfer process [121]; the charge trapping/detrapping mechanism is useful with NCs, the NCs in RS layer can be act as seed layer; and colloidal NCs can act as a complete switching layer. Instead of the NCs layer, a thin metal layer in RS stack can also improve the device performance, as reported previously [122]. The defect engineering process is not only suitable for the switching layer but also for the electrodes. The major advantages of the localized electric field enhancement by NCs can be utilized to design the bottom electrode layer. Several nanostructures-based bottom electrodes are reported to improve the performance of RRAM devices, such as nano-pyramid [123], nano-peak [124], arc-shaped [125], and so on [126]. A detailed review on defect engineering in RRAM is reported in Reference [127].

4. Challenges of Emerging Nonvolatile Memory Devices

So far, as compared to other prototypes and emerging nonvolatile memory devices (Figure 7), RRAM technology promises highly improved performance in device scalability, multilevel-cell (MLC) storage capacity with 6bits/cell, low-cost 3D fabrication possibility, etc. Recently, research also identify the atomic level control of the filament and the possibility to form electrically controllable break junction [73], which also can detect spin-like switching behavior in RRAM [111]. While RRAM devices are useful, there are still several challenges hindering the real applications. The uniformity and reliability of the cell-level resistive switching present a major problem. The stochastic nature of the filament is the main source of variations in RRAM devices. The performance variation is not acceptable for memory applications. To avoid the filamentary switching in RRAM devices, several solutions have been proposed. It is reported that the non-filamentary devices have higher stability. Recently, Maikap et al. [128] identified the possibility to transform the filamentary switching into a non-filamentary, by introducing dual-nanostructure engineering inside the switching matrix. Figure 11a shows the high-resolution transmission electron microscopic image of the dual-nanostructure-engineered RRAM device. The bottom electrode is designed was nano-dome with surface roughness of 8 nm, as shown in the atomic force microscopic image of Figure 11c. In the middle of the resistive switching layer, the presence of nano-crystals with 1 nm in diameter is shown in the plan-view transmission electron microscopic image of Figure 11b. The devices without nanostructure (Figure 11d) and with single nanostructure (Figure 11e) can perform filamentary resistive switching after going through a forming process. However, the devices-switching uniformity is very poor. In contrast, Figure 11f shows non-filamentary forming free highly stable switching in dual-nanostructured RRAM devices. However, though the performance is highly improved with such kind of material engineering, the fabrication process is complicated and not suitable for mass production.

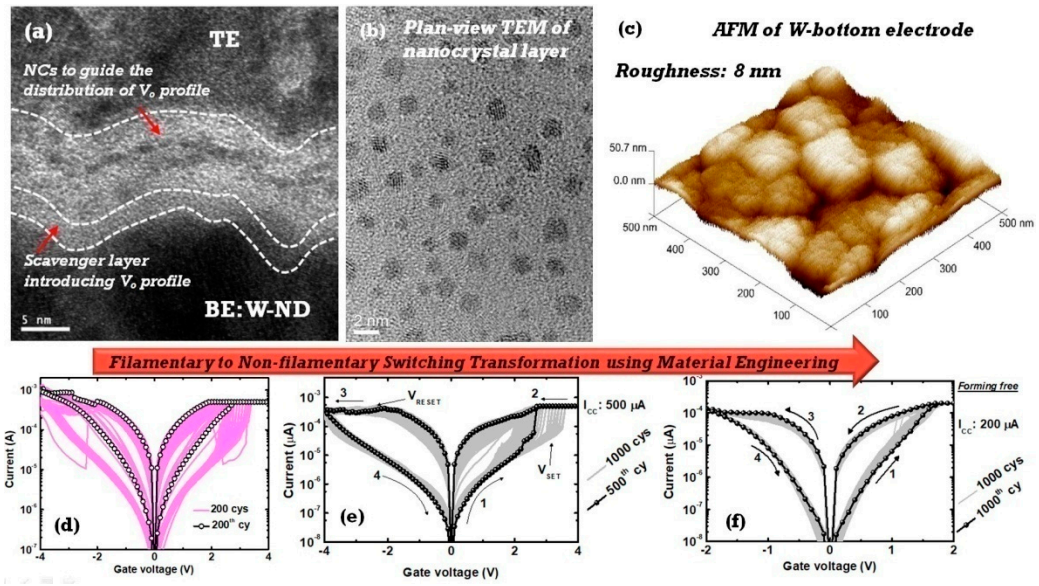

Figure 11. (**a**) The high-resolution transmission electron microscopic image and (**b**) the plan-view transmission electron microscopic image of the W/AlO_x/IrO_x-NCs/AlO_x/IrO_x structures. (**c**) The atomic force microscopic image of the nano-dome W-bottom electrode with 8 nm of surface roughness. The resistive switching performance in devices (**d**) without any nanostructure, (**e**) with single nanostructure, and (**f**) with dualnanostructures. Due to nonfilamentary switching in the dual-nanostructured device, highly reliable resistance states are achieved. (Reproduced from Adv. Electron. Mater. 2020, 2000209, with the permission of John Wiley and Sons Publishing [128].)

To improve the switching stability and endurance of the RRAM devices, a new concept of hybrid RRAM (HRRAM) is also demonstrated [129,130]. In this type of device, the filament is a combination

of metal-interstitials and oxygen vacancies. The formation of this kind of filament is energetically favorable. Under RESET operation, oxygen vacancies can be removed faster than the metal-interstitials; hence, during RESET, a small part of the filament will be broken, and the device can switch with less energy. In this kind of device, the proper balance between the metal-interstitials and oxygen vacancies is essential. In addition, the operation condition of the HRRAM devices is also a critical factor. To improve device performance, defect engineering can be influential; however, it is not easy to control defect distribution from cell-to-cell. As discussed, scalability is one of the major advantages of RRAM which can hit atomic dimension. Therefore, atomic-scale control of NCs in RRAM devices in a vital challenge. A multilayer RRAM may improve the performance; however, the realization of the physics behind the switching process of such a device is complicated.

The high-density RRAM is possible with 3D horizontal or vertical architecture, in which the sneak leakage path is one of the major challenges. For large size array, highly nonlinear I–V is the solution to sneak leakage paths. However, the limited nonlinearity of RRAM is a major challenge which can be overcome with the integration of selector devices. The selector device is very important in NVM technology, as summarized in Figure 1b. There are several selector devices, such as transistors, diodes, nonlinear devices, and volatile switches. A functional NVM cell is fabricated with a nonvolatile ON/OFF-switch-based storage element and a selector device (to control the behavior of the storage element). The FeFET is a 1T structure, like flash memory, which can combine with a 1T selector. The three-terminal devices have limited choice in selector. The two terminal switch elements can work with a 1T1R or 1S1R platform. Integration of a selector device on the sidewall of a 3D vertical structure is a challenging task. A low-temperature two-terminal selector is the key for the 3D stackable memories. The requirement of highly smooth sidewall for high-performance MTJ can limit the 3D design in STTRAM devices; however, theoretically it is possible. The self-rectifying nonlinear 1R RRAM device is suitable for 3D architecture. However, the two-terminal selector is required, as it can utilize either asymmetry or nonlinearity, to suppress sneak leakage paths. In summary, for baseline flash memory, the planar and 3D vertical design is suitable; for FeFET, only a planar structure is suitable; for PCM and STTRAM, both the planar and 3D stackable design are suitable; and for RRAM, all possible structures, like planar, 3D stackable, and 3D vertical, are suitable. The 1T provides better operation control, and in contrast, 1R provides high-density memory. A summary of advantages and major challenges of major eNVM devices is given in Figure 12.

	Main advantages	Key challenges
FeFET	• 1T cell structure • Low-power field-driven • High performance • Ferroelectric doped HfO_x	• Material and processing • FEOL integration • Reliability and parasitic effects (*e.g.*, charge trapping)
PCM	• Maturity • Proven performance	• Reliability • Disturbance • High switching power
STTRAM	• High performance • Well-understood physics • Novel mechanisms (*e.g.*, SHE, VCMA) to extend capabilities	• Reducing I_c/Δ (power-stability tradeoff) • MTJ patterning and etching • BEOL thermal budget
RRAM	• Simplicity and low cost • High density • Versatile materials, structures, and behaviors	• Reliability and failures • Stochastic mechanism and intrinsic variability • Forming

Figure 12. Advantages and challenges of the main emerging NVM technologies. (Reproduced from Solid-State Electron. 2016, 125, 25–38, with the permission of Elsevier Publishing [2].)

5. Applications of Emerging Nonvolatile Memory Devices

The eNVM devices have wide range of applications, as summarized in Figure 8a. The basic objective of an eNVM is the applicability in memory space. For example, STTRAM can replace SRAM

or DRAM, and RRAM can replace flash devices after they fulfill the basic requirements. The successful replacement of existing memory is only possible if new technologies provide significant advantages in terms of device performance and cost-effective scalability. Additionally, the performance of existing devices, product requirements, and business infrastructure are the additional entry-wall of the new technologies. In STTRAM, the speed and endurance are the major advantages; however, in RRAM, the scalability with low power operation is the key advantage which is very much needed in a high-density memory device. The 3D NAND flash is a big challenge to RRAM because of the high density and lower bit-cost. To compete with that the other capabilities of RRAM, such as low voltage operation, faster switching, and longer endurance with MLC performance is impressive. The eNVM provides excellent performance as compared to the capacity of eFlash. However, the reliability of eNVM has to be improved for embedded applications. The highly scalable eNVM candidates are alternative solutions for the embedded applications.

In general, there is a performance gap between storage and memory. For example, a flash device is nonvolatile with compromising the speed and endurance; on the other hand, DRAM device is volatile with compromising of retention. The system performance and cost can be highly affected by the gap between storage and memory. However, finding a "universal memory" to fulfill all the characteristics of different devices is very challenging. It is the need of time to design a device which can fulfill the gap between storage and memory. The concept of storage class memory (SCM) is introduced to fill up the performance gap. The eNVM, which can act as SCM, should be highly scalable and ultra-high density, with preferably MLC capacity. Till now, PCM and RRAM devices have been showing promise to hit the required performance, and they are considered to be the best suitable for SCM application. The eNVM devices can reduce the standby power of computing systems. The power budget of wireless sensor devices and the internet of things (IoT) is much restricted than the mobile devices. In such applications the baseline low-voltage SRAM devices would be suitable but suffers from large area consumption with ten-transistor. Due to the high operating voltages and power, flash memory is not suitable for such applications. Additionally, the conventional von Neumann architecture requires high power consumption and slows down the speed of the computing system. The eNVM devices are suitable in this kind of applications, and by using the simple two-terminal structures (STTRAM and RRAM), it offers advanced architectural options beyond von Neumann scope.

Brain-inspired computing, i.e., neuromorphic computing, is one of the emerging novel functionalities beyond memory space. As compared to today's von Neumann computers, brain can perform complex tasks, such as recognition, inference, etc., with minimal power consumption. The well-known learning rule in neural network is spike-time-dependent plasticity (STDP), which is the synaptic weight modification by the pre- and post-synapse timing difference. In such applications, because of the good scalability and low power consumption, eNVM devices can achieve the synaptic density closer to the density in brain (~ 10^{10}/cm^2). Both the PCM and RRAM are the major eNVMs in this category. In RRAM, the switching can be abrupt or analog type. For neuromorphic computing, a precise change of conductance is essential; hence, analog switching is very useful. Integration of such a device with CMOS technology would be a problem-solver associated with artificial intelligence. For neuromorphic applications, a high-density, low-power device with at least 5bits/cell storage is necessary. A prototype of such RRAM-based neural network of 8×8 1T1R array in the Ag-doped SiO_xN_y structure is shown in Figure 13a–c [131]. The synaptic weight update was demonstrated with special learning protocol and peripheral circuit design (Figure 13d–f). The research also identified the possibility to emulate both the short-term and long-term synaptic plasticity by using Ag-doped RRAM devices based on MgO_x, SiO_xN_y, and HfO_x. Figure 13g shows the paired-pulse measurement, and Figure 13h shows the STDP in such device. However, sometime gradual transition of resistance state is difficult during the SET of RRAM and RESET of PCM. New device engineering with "2-PCM" synapse is also proposed [132].

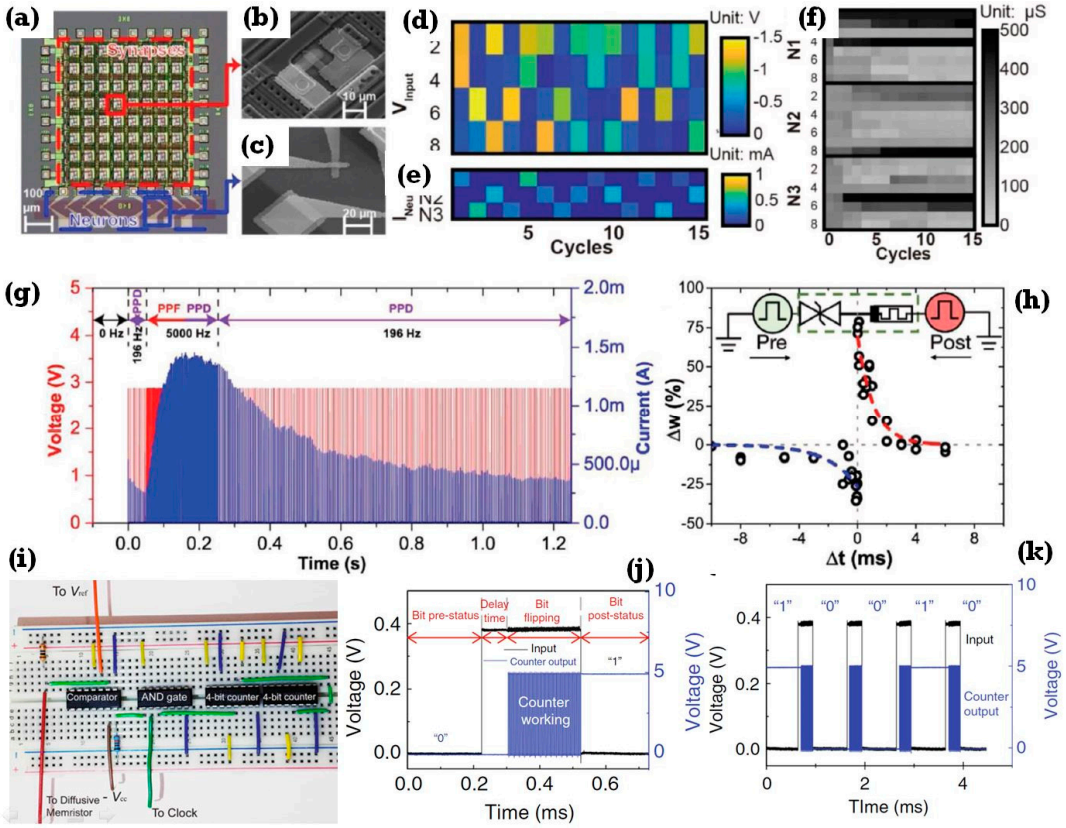

Figure 13. (**a**) The optical image of a typical 8 × 8 1T1R memristive neural network with the scanning electron microscope image of (**b**) a 1T1R device and (**c**) a single 1R device. (**d**) The input pattern, (**e**) peak neural current, and (**f**) synaptic weight at each training cycle. (**g**) The PP and (**h**) spike-time-dependent plasticity (STDP) measurements. (**i**) Image of circuital arrangement of a volatile diffusive memristor device for TRNG application with the (**j**) one counter output in response to 1 kHz input voltage pulse. (**k**) Random binary out flipping states over continuous switching cycles in the TRNG devices. (Reproduced from J. Appl. Phys. 2020, 127 (5), 051101, with the permission of AIP Publishing [127]).

In the era of IoT, hardware security is one of the major areas of applications of eNVM devices. A point to note is that, for memory applications, the stochastic behaviors of eNVMs are undesirable, but the truly random state variations are very much usable as entropy sources for security applications. In security applications, variability of eNVM devices in terms of resistance, switching voltage, random telegraph noise, and switching yield controlled by operation conditions are important. In security applications, STTRAM and RRAM are the key contenders. In RRAM-based security systems, the randomness is useful in security applications such as physical unclonable function (PUF) and true random number generator (TRNG). In such devices, the intrinsic stochasticity is the major source of entropy changes or randomness, which can generate random numbers and is extremely useful for generating cryptographic keys. By using the variation of LRS or HRS from cycle-to-cycle and also device-to-device, variations in a TRNG can be realized. A volatile-type diffusive RRAM based TRNG using the diffusion dynamics of metal atoms in Ag-doped SiO_2 structure is reported [133]. A typical circuital arrangement with an Ag-doped diffusive memristor, a comparator, an AND-gate, and a counter is shown in Figure 13i–k. In this case, the intrinsic stochasticity of the delay time is the source of entropy.

6. Summary

With a wide range of performance, maturity, and device scaling, eNVM devices are broadening the horizon of emerging applications. Among several alternative eNVM devices, FeFET, PCM, STTRAM,

and RRAM are the most promising. Device design, systems, materials, etc., can be influential to control the behavior of the eNVM devices. For example, depending on structure design, the switching mechanism and device operation can be controlled in RRAM. Though the dream of a universal memory is not yet fulfilled, the eNVM devices can minimize the performance gap between storage and memory. There are several challenges associated with eNVM technologies, such as cell-level and device-level reliability, variability, device yield, highly smooth structure design, etc. The eNVM provides opportunities to replace the baseline memories, play the role of SCM, investigate novel architecture, investigate brain-inspired computing systems, and design hardware security systems. The low-power eNVM can also be useful to the sensors and in IoT applications. There are still many challenges to design high-yield eNVM devices, like the manufacturing process, materials, and optimized operation for different kind of applications.

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