


Article

A 920-MHz Dual-Mode Receiver with Energy Harvesting for UHF RFID Tag and IoT[†]

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Abstract: A low-power dual-mode receiver is presented for ultra-high-frequency (UHF) radio frequency identification (RFID) systems. The reconfigurable architecture of the tag is proposed to be compatible with low-power and high-sensitivity operating modes. The read range of RFID system and the lifetime of the tag are increased by photovoltaic, thermoelectric and RF energy-harvesting topology. The receiver is implemented in a 0.18- μm standard CMOS process and occupies an active area of 0.65 mm \times 0.7 mm. For low-power mode, the tag is powered by the rectifier and the sensitivity is -18 dBm. For high-sensitivity mode, the maximum PCE of the fully on-chip energy harvester is 46.5% with over 1- μW output power and the sensitivity is -40 dBm with 880 nW power consumption under the supply voltage of 0.8 V.

Keywords: RFID; receiver; energy harvesting; cross-coupled voltage multiplier; charge pump; ultralow-power circuits and systems

1. Introduction

With the emerging development of the Internet of things (IoT), wireless sensor networks (WSN) are widely used, such as the wearable health monitoring system and environmental monitoring system. Radio frequency identification (RFID) science has the advantages of standardization identification, low cost and small form factor, there is growing interest in combining RFID and on-chip sensors into smart sensor nodes [1–6]. However, read range is a big challenging topic for these applications.

The passive RFID tags, whose maximum read range is limited within 12 m, are powered by the RF energy radiated from the reader [1]. The read range becomes even worse when RFID tags are equipped with sensors [2,3]. Semi-passive and active RFID tags powered by the external battery; therefore, they are suitable for long read range and sensing. By using the same envelope detector and backscatter topology as the passive tags, the conventional battery-assisted ultra-high-frequency (UHF) RFID tags achieve maximum sensitivity of -26 dBm and the read range is around 30 m [4]. The receiver is always-on or turned on in each duty cycle. The power consumption of the receiver is several microwatts; hence, the lifetime of the battery is limited.

In these years, the high-performance transceivers are proposed and implemented in RFID tags to further extend the read range up to over 100 m [5–8]. However, the heterodyne receiver includes a passive mixer and a local oscillator (LO) which consumes several hundred microwatts power [9]. The lifetime of the tag would be decreased to several weeks. To solve the power consumption issue and avoid the use of LO, the direct envelope detector based receiver (ED-Rx) is a viable technique to scale down the average current and to meet the system power requirement.

For ED-Rx, there are tradeoffs between power consumption, sensitivity and data rate. In [7], the ED-Rx consumes 1 μ W at 930 MHz carrier frequency with a sensitivity of -55 dBm and a data rate of 10 kbps. However, the high-Q impedance matching technique leads to a narrow frequency band of these receivers, which will increase the design difficulty of the antenna. In addition, these receivers are incompatible with the UHF RFID protocol. When implemented with backscatter circuits and transmitter, the Q factor and passive gain will be decreased, and the sensitivity of the receiver will be decreased to -30 dBm.

On the other hand, to break the limitation of the lifetime and eliminate the use of battery, photovoltaic (PV) and thermoelectric (TE) are promising energy sources for RFID tags. For millimeter-sized PV and TE cells, the output power is several microwatts and the output voltage is 0.2 V to 0.4 V in typical. To address these issues, recent efforts have been focused on the fully integrated DC–DC boost converters that can undertake a tiny input voltage (V_{IN}), while offering a high output voltage (V_{OUT}) and a high power conversion efficiency (PCE) [10–14].

In this study, a dual-mode UHF RFID tag is proposed. The PV and TE energy-harvesting topology is adopted along with RF energy harvesting to eliminate the external battery. The reconfigurable architecture of the receiver is introduced to be compatible with conventional passive RFID tags. The receiver can operate in low-power (LP) and high-sensitivity (HS) modes according to the input signal power. The proposed RFID system achieves low power consumption, long read range and high integration.

This study is an extended version of our study published in the IEEE 13th International Conference on ASIC, 2019, Chongqing, China [15]. The chip is taped-out and the measurement results and comparison table are added to this article. The study is organized as follows: Section 2 describes the principle of the proposed RFID system. Sections 3 and 4 shows the circuits and simulation results of energy harvester and receiver. Section 5 is the measurement results. Finally, the conclusion is drawn in Section 6.

2. Proposed UHF RFID System

2.1. Link Budget

For passive RFID tags, the sensitivity and read range are mainly decided by the input RF power which is delivered to the antenna. The input power could be calculated using the Friis equation and the relationship of tag input power and distance between tag and reader is shown in Figure 1.

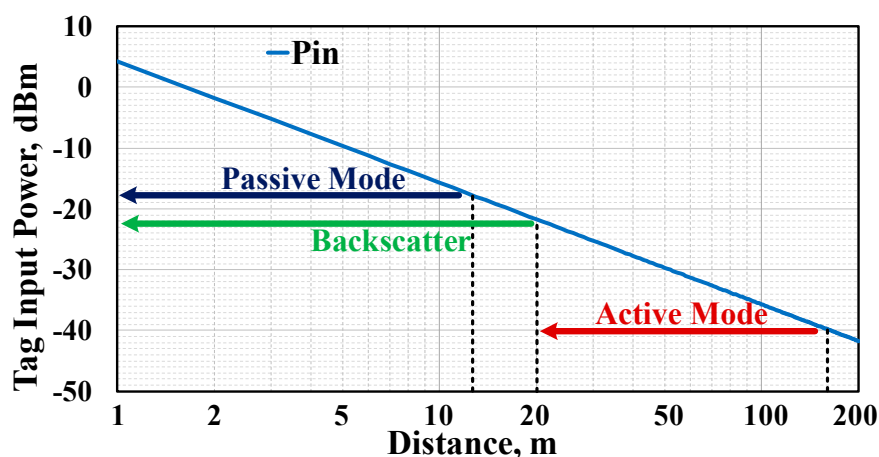


Figure 1. Read range and operating modes of ultra-high-frequency (UHF) radio frequency identification (RFID) system.

The maximum read range of passive-receiving mode is determined by the power consumption of the tag and the sensitivity is typically between -15 dBm and -20 dBm. For backscatter operating

mode, the RF signal is modulated and reflected back to reader. Typically, the output power of the reader is 36 dBm and the maximum sensitivity of the reader is -80 dBm. Hence, the tag could operate in backscatter-mode when input power is larger than -22 dBm by calculation.

For active-operating mode, the read range is increased by the active transmitter. The maximum output power of the transmitter can be selected as -10 dBm by the tradeoff between read range and power consumption. Therefore, the sensitivity of active-receiving mode should be -40 dBm and the read range can achieve more than 150 m.

2.2. Architecture of RFID Tag

The architecture of the proposed self-powered RFID tag is shown in Figure 2. The dual-mode ED-Rx, RF energy harvester, backscatter circuit and transmitter are connected to the RF port and the input impedance is conjugate matched with a dipole antenna. The fully on-chip DC-DC boost converter is connected to the off-chip PV and TE cell and harvests energy from the environment or the human body.

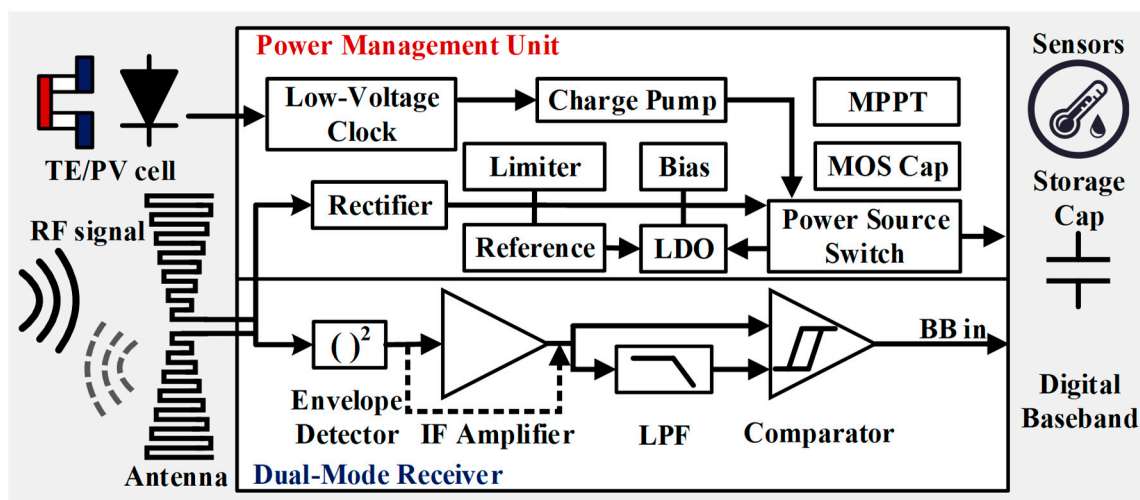


Figure 2. Proposed self-powered RFID tag architecture.

Depending on the power-supply mode, the ED-Rx can operate in high-sensitivity and low-power-receiving modes, and the maximum sensitivity is over -40 dBm. It operates in high-sensitivity receiving and active-transmitting mode in default when powered by PV and TE harvester. Considering the energy is not sufficient during the night and for indoor environment, the RF energy-harvesting topology is also adopted [14]. It powers the chip when the input RF signal is larger than -20 dBm and the tag could switch to backscatter mode and low-power-receiving mode by detecting the strength of received RF carrier. The low-power-receiving mode is fully compatible with conventional passive RFID tags.

Due to the small amount of transmitting data, the operating time of active transmitter is within 1 ms. The microwatt energy harvester charges the off-chip storage capacitor and enables the milliwatt transmitter in duty-cycle [16–18]. The power management circuits such as current source and voltage references are designed in the subthreshold region and the power consumption is several nanowatts [18–20].

3. Proposed Energy Harvesting Topology

3.1. Photovoltaic and Thermoelectric Energy Harvesting

The low-power photovoltaic and thermoelectric energy-harvesting topology is proposed to eliminate the external battery. The fully integrated DC-DC boost converter is based on a 3-stage

differential charge pump scheme as shown in Figure 3, which can deliver a high V_{OUT} to power-up other circuits. The charge pump is driven by a ring-oscillator-based clock generator when V_{IN} is in the range of 0.2 V to 0.3 V.

Due to the threshold voltage of MOSFETs is larger than V_{IN} , the bootstrapped inverter is adopted in the oscillator as the delay cell. The swing of the output clock signal is tripled ($-V_{IN}$ to $2V_{IN}$) and the output drivability is enhanced at low supply voltage. Then, the output voltage can be boosted to over 1 V by the 3-stage charge pump.

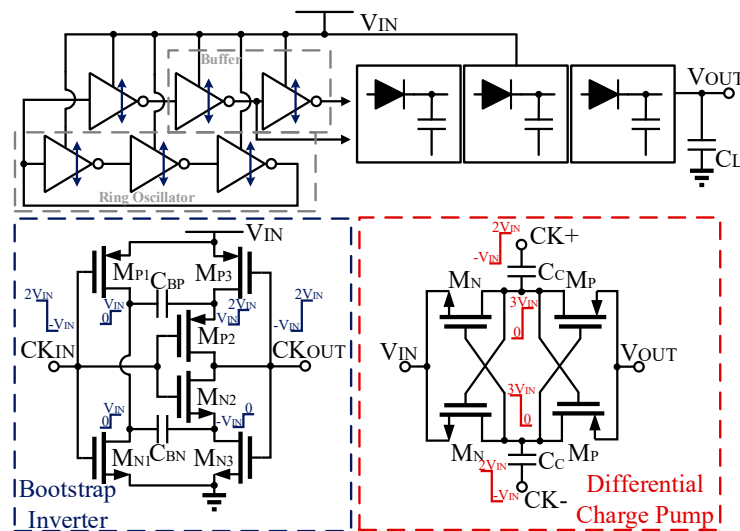


Figure 3. Schematic of proposed photovoltaic and thermoelectric energy-harvesting circuit.

For the switched capacitor charge pump, the clock is used to control the MOSFET switch M_P and M_N to charge and discharge the capacitor C_C in each cycle. The voltage is increased by $3V_{IN}$ for each boost stage due to the bootstrapped clock. For the proposed 3-stage boost charge pump, the output voltage V_{OUT} is derived in

$$V_{OUT} = 10V_{IN} - 3(V_{MOS} + 3V_L) \tag{1}$$

$$V_L = \frac{I_{clk}}{2f_{OSC}C_B} + \frac{I_{OUT}}{2f_{OSC}C_C} \tag{2}$$

where the V_L is the voltage drop on the bootstrap capacitor C_B and charge pump capacitor C_C due to the current of delay cell I_{clk} and the output current I_{OUT} . f_{OSC} is the frequency of clock signal, V_{MOS} is the total voltage drop on the transistors. The PCE is defined by the ratio of the output DC power P_{OUT} to the total input power P_{IN} , which is derived in

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}^2}{V_{IN}I_{IN}R_L} \tag{3}$$

and the high PCE can be achieved by selecting a larger $f_{OSC}C_C$ product to reduce the voltage drop V_L across the capacitor. In this design, $C_C = 20$ pF and $f_{OSC} = 2.5$ MHz are selected considering chip area and PCE. The V_L and V_{MOS} are 20 mV and 100 mV by simulation. When V_{IN} is 0.2 V and the load is in the range from 0.5 M Ω to 1.7 M Ω , the total PCE can reach more than 40%.

3.2. RF Energy Harvesting

The core of RF energy harvester is the rectifier which supplies DC power by rectifying the input RF signal from the antenna. The 3-stage differential cross-coupled rectifier is adopted, and the circuit is shown in Figure 4.

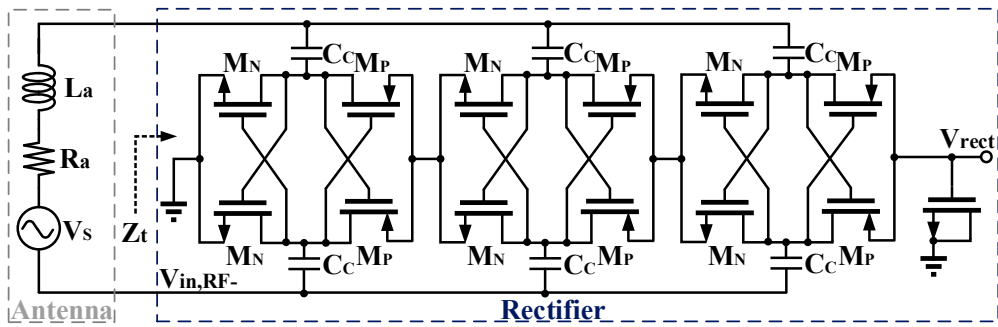


Figure 4. Schematic of proposed radio frequency identification (RF) energy-harvesting circuit.

The rectifier performance is evaluated by the term of sensitivity and power conversion efficiency (PCE). Sensitivity is defined as the minimum input RF power required to generate a specific DC output voltage, and PCE is the ratio of the DC output power to the RF input power [16]. Circuit topology, device parameters, carrier frequency, the amplitude of input RF signal, and the output loading conditions affect the PCE and sensitivity of the rectifier. The input impedance of receiver Z_t is mainly decided by the rectifier. Z_t is capacitive and should be conjugate matched with the inductive impedance of RFID tag’s dipole antenna.

When operating in LP mode, the receiver is powered by the rectifier with the on-chip MOSFET capacitor. Assuming the power consumption of the whole system is several microwatts, the simulation of output voltage and PCE versus input power for different stages and load resistance is adopted and the results are shown in Figure 5. When the output voltage is larger than 1 V, the 3-stage scheme achieves -18.5 dBm and -17 dBm sensitivity for $5\text{-}\mu\text{W}$ and $10\text{-}\mu\text{W}$ output power, respectively. The maximum PCE is more than 40% for LP mode according to simulation results.

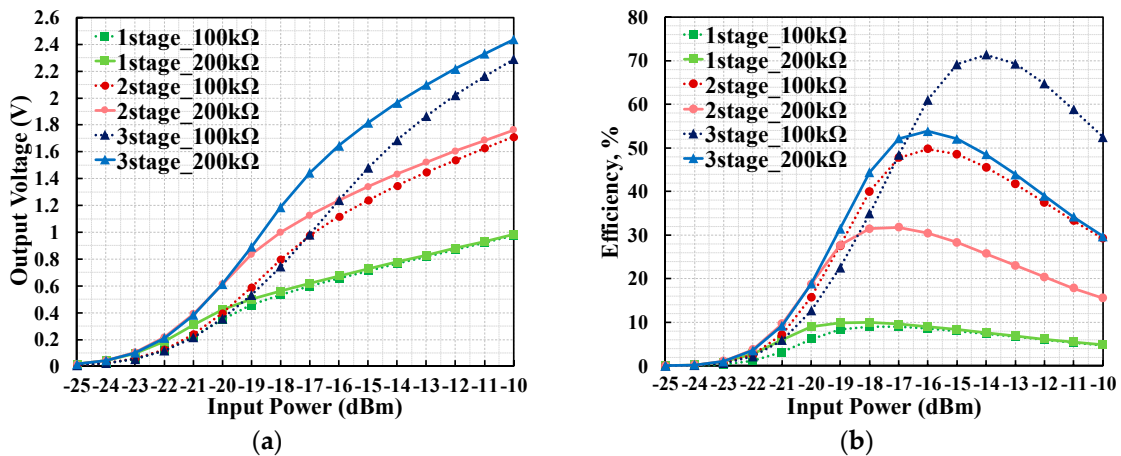


Figure 5. Simulation results of the rectifier, (a) output voltage versus input power for different stages and load resistance; (b) efficiency versus input power for different stages and load resistance.

4. Proposed Dual-Mode Receiver

4.1. Architecture of Proposed Dual-Mode Receiver

The architecture of the proposed receiver is shown in Figure 6. The receiver can operate in low-power (LP) mode and high-sensitivity (HS) mode. When operating in LP mode, the circuit is powered by the 3-stage rectifier with an on-chip MOSFET capacitor. When the energy provided by the PV/TE energy harvester is sufficient, the receiver operates in HS mode and the receiver’s sensitivity is increased.

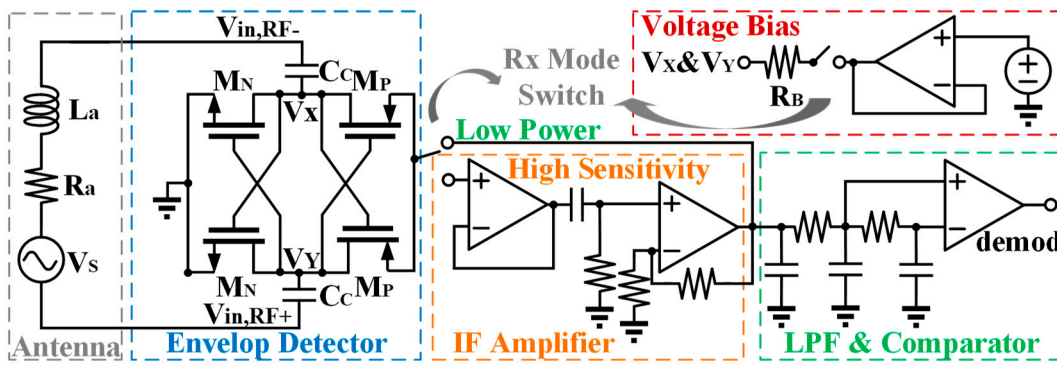


Figure 6. Architecture of proposed dual-mode direct envelope detector based receiver (ED-Rx).

The MOSFETs of the RF detector are operating in the sub-threshold region in order to reduce power consumption. It detects the envelope from the incident RF signal due to the exponential transfer function of M_N and M_P . Then, the envelope is switched to the intermediate frequency (IF) amplifier. The first stage is buffer with high pass filter (HPF), and the gain of the second stage amplifier is 20 dB and the bandwidth is 150 kHz which is from 5 kHz to 200 kHz. The demodulator circuit is based on low-pass filter (LPF) and comparator, the hysteresis value of comparator is optimized considering mismatch and noise [9].

4.2. Envelop Detector with Voltage Bias

The proposed envelop detector is shown in Figure 7. The voltage bias is turned off and the circuit can extract the envelope of the received OOK modulated RF signal without power consumption in LP mode.

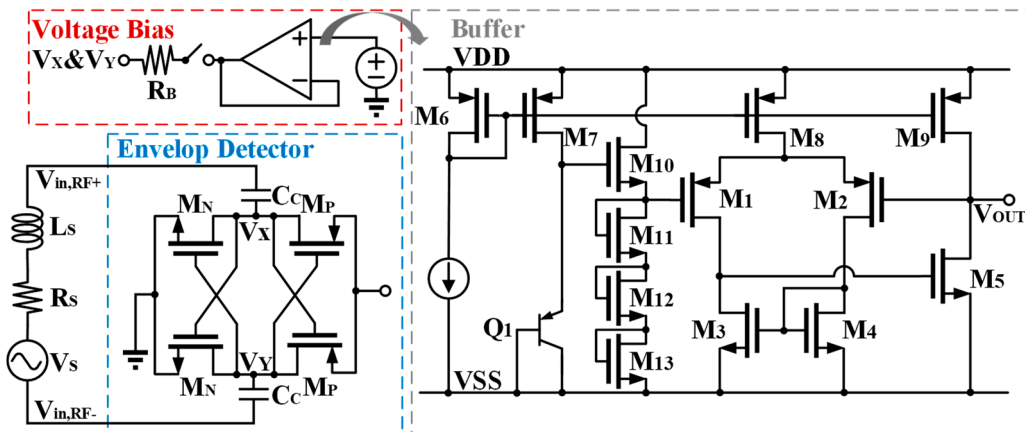


Figure 7. Schematic of proposed dual-mode envelope detector circuit.

The amplitude of the input RF signal and the amplitude of the envelope detector's output signal versus input RF power are shown in Figure 8. The output amplitude of the passive envelope detector is over 100 mV when the input power of RF signal is larger than -18 dBm, which is easy to demodulate. But for input power less than -18 dBm, the amplitude of the output envelope signal is almost zero [20].

When operating in HS mode, the envelope detector is biased by an internal voltage reference and buffer. The sensitivity is improved, and it becomes more suitable for operating at low input power. With an input power from -40 dBm to -20 dBm, the amplitude of the output envelope signal is from 10 mV to 100 mV, which cannot meet the needs of the demodulation circuit in the subsequent stage. The signal is appropriately amplified and then demodulated. The bias voltage is generated by V_{BE} of a BJT device Q_1 and voltage divider ($M_{10}\sim M_{13}$). The CTAT type bias voltage can compensate the worse sensitivity of the envelope detector at low temperature.

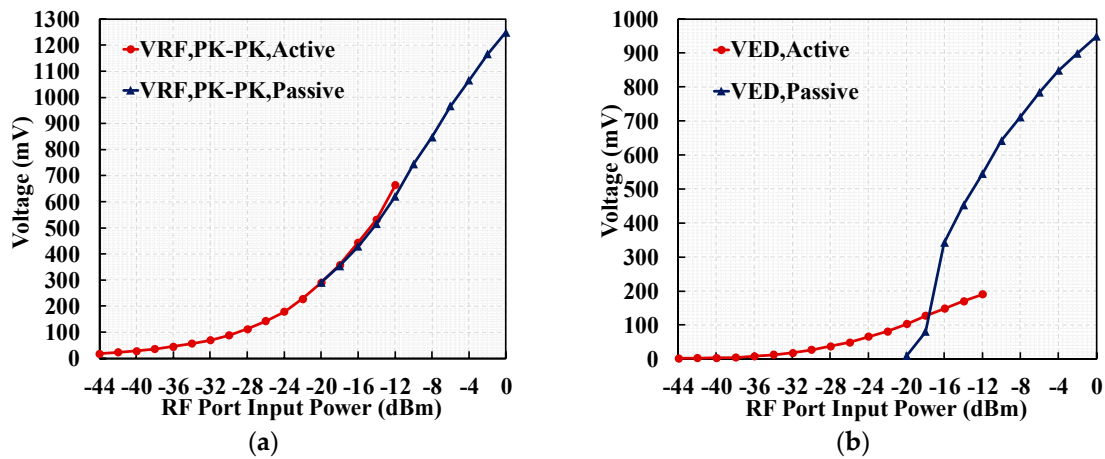


Figure 8. (a) Amplitude of the input RF signal versus input RF power; (b) amplitude of the envelope detector’s output signal versus input RF power.

The output noise of the envelope detector is shown in Figure 9. By calculating the signal-to-noise ratio of the output port of the envelope detection circuit, the sensitivity of the receiver can be estimated in the most direct way [8]. The output signal-to-noise ratio can be calculated by

$$SNR_{OUT,ED} = S_{ED,OUT}^2 / \sigma_{EO,BB}^2 \tag{4}$$

$$P_{Sensitivity\ by\ SNR} = \sqrt{2 \cdot SNR_{min} \cdot \sigma_{EO,BB}^2} / K_v^2 \tag{5}$$

For a 200 kHz baseband signal bandwidth, the output port noise power of the envelope detection circuit $\sigma_{EO,BB}^2$ is approximately $9 \times 10^{-8} V^2$, K_v is the amplitude ratio of envelope detector’s output and input signal. Assuming the minimum amplitude of the output envelope signal is 10 mV, then the SNR is calculated to be about 30 dB, and the receiver sensitivity estimated from the SNR is -35 dBm. Considering the passive gain of impedance matching, the sensitivity of the receiver in HS mode is estimated to achieve -45 dBm.

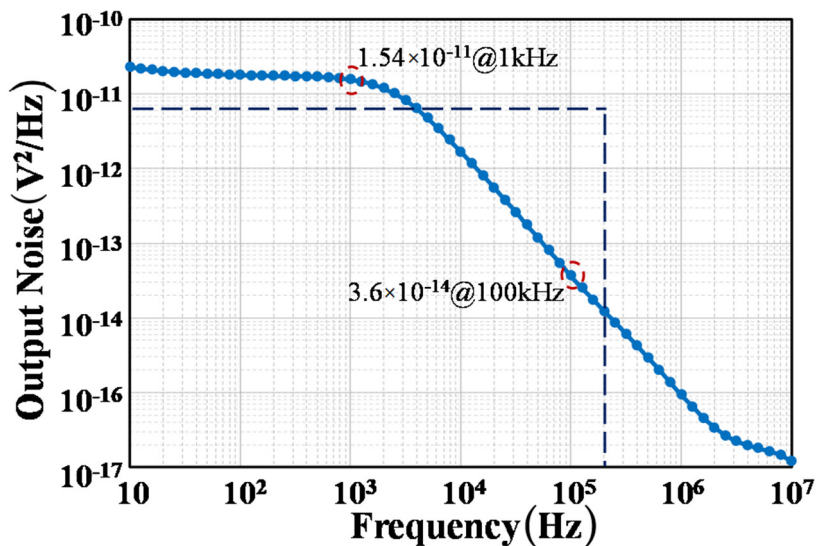


Figure 9. Output noise of proposed envelope detector in high-sensitivity (HS) mode.

4.3. IF Amplifier

The proposed envelope detector has high output impedance, the unity gain buffer is adopted to drive high pass filter (HPF) in HS mode. Then, the IF signal is further amplified by the baseband amplifier (BB Amp). The unity gain buffer circuit and baseband amplifier are shown in Figure 10.

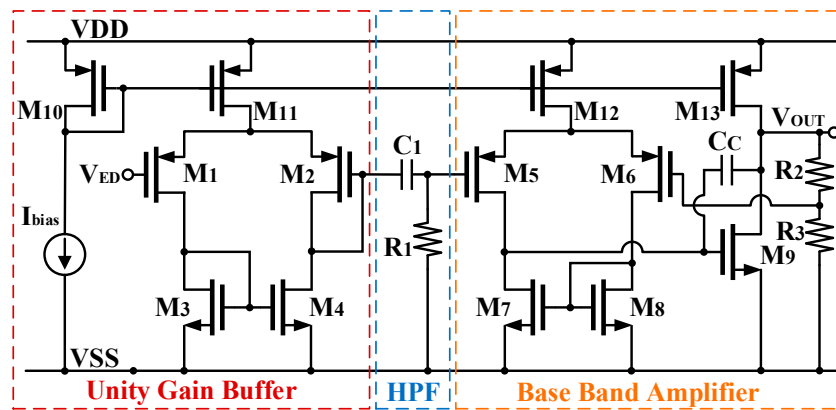


Figure 10. Schematic of proposed IF amplifier.

The input MOSFETs M_1 and M_2 of the buffer are designed in minimum size to reduce the parasitic capacitance. The PMOS input baseband amplifier is adopted because the DC output voltage of HPF is zero [20].

The simulation results of the gain and phase margin of the proposed IF amplifier is shown in Figures 11 and 12. As shown in Figure 11a, the high pass cutoff frequency is decided by C_1 and R_1 , $f_c = 1/(2\pi R_1 C_1)$ which is 5 kHz. The open-loop gain of second stage amplifier is 30 dB. The simulation result at tt corner shows that the phase margin is larger than 60° when gain reduced to 0. Moreover, the phase margin can guarantee the stability of the IF amplifier with corner and temperature variation. The closed-loop gain is decided by the ratio of R_2 and R_3 , $A_{V, close loop} = 1 + R_2/R_3$ which is 20 dB as shown in Figure 12a. The cascade scheme of HPF and baseband amplifier results in a band pass filter feature. The 3-dB frequency of baseband amplifier is 200 kHz.

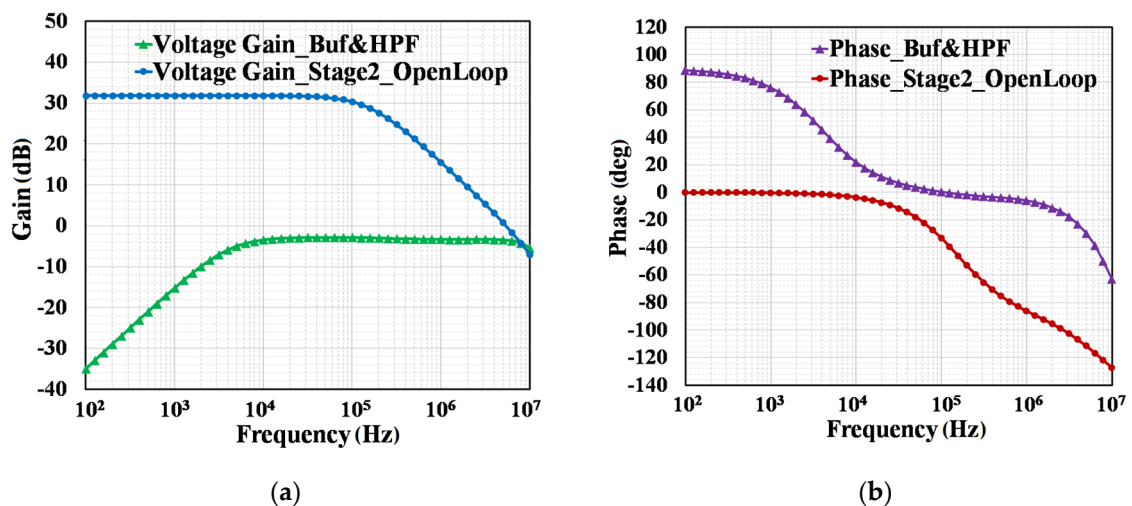


Figure 11. Simulation results of first stage and second stage in IF amplifier: (a) gain; (b) phase.

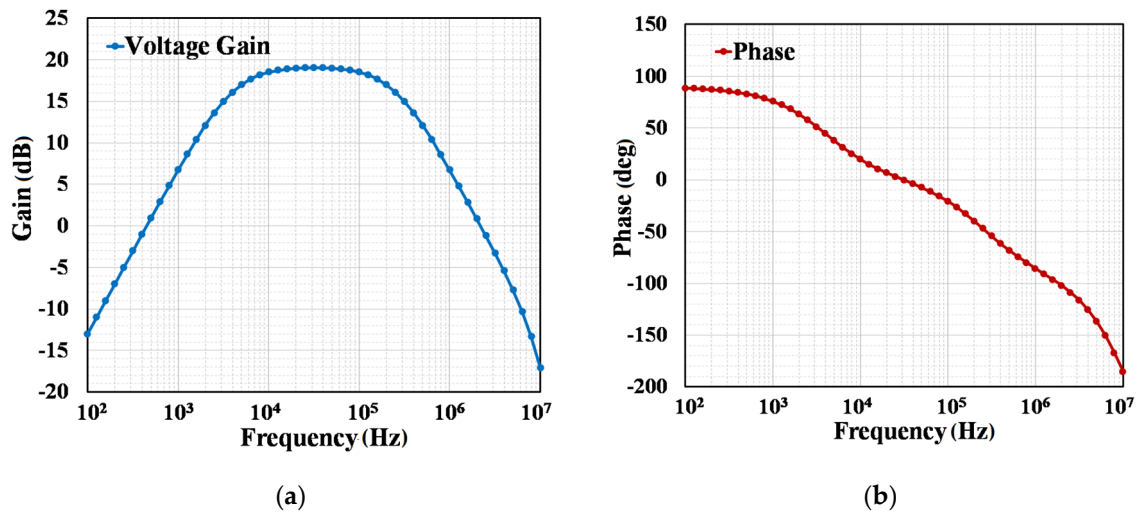


Figure 12. Simulation results of IF amplifier: (a) gain; (b) phase.

4.4. Demodulator

The demodulator circuit is based on a low-pass filter (LPF) and a hysteresis comparator, as shown in Figure 13. Because the low-pass filter has a smaller cutoff frequency, and in order to reduce the area of the circuit, the MOS capacitor with larger unit capacitance is used instead of the conventional MIM capacitor. The calculation of the low-pass filter cutoff frequency is $f_c = 1/(2\pi RC_{MOS})$. In this design, the typical values of total resistance and capacitance are 500 kΩ and 10 pF.

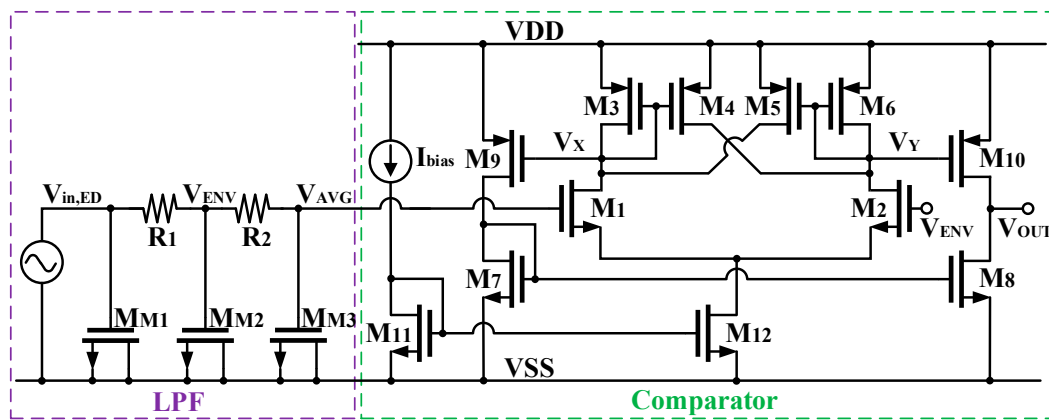


Figure 13. Schematic of proposed demodulator including low-pass filter and comparator.

The demodulation and digitization of the signal is achieved by the comparator. Therefore, the comparator needs to be designed as a hysteretic comparator structure because of the slowly changing input signals and noisy environments. As shown in Figure 13, positive feedback is introduced in the circuit through the source-level cross-coupling structure of the M_4 and M_5 [21].

Due to the fully differential structure of the hysteretic comparator, the second-stage amplifier is added and realizes the differential to single-ended output function through a current mirror M_7 . At the same time, the gain of the comparator is further improved. The hysteresis range is designed as 40 mV to provide good immunity to the fluctuations of noise and glitches.

5. Measurement Results

The dual-mode receiver and energy harvester were fabricated in standard 180 nm CMOS process with a 0.455 mm² active area, as shown in Figure 14. The chip was dominated by capacitors of the rectifier and charge pump circuit.

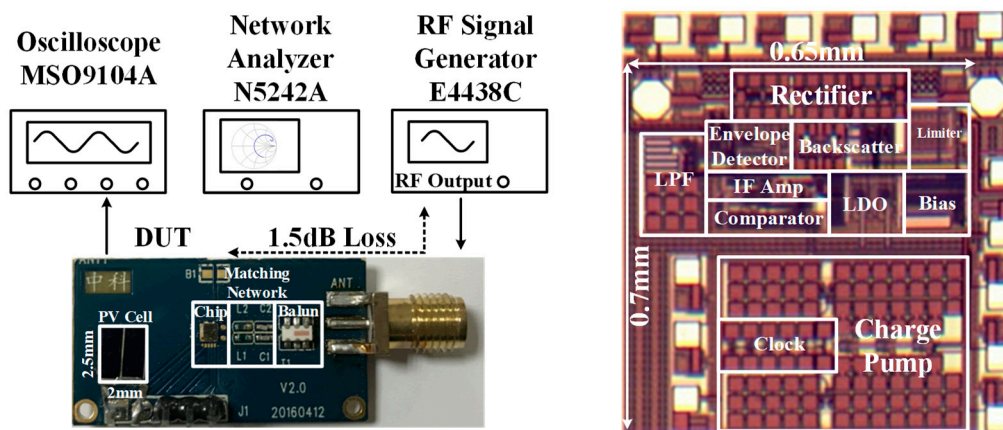


Figure 14. Measurement setup and microphotograph of the implemented chip.

The chip was connected to the PCB using bond wires. The measurement setup included an Agilent signal generator (E4438C), Agilent oscilloscope (MSO9104A), network analyzer (N5242A) and a digital multimeter (FLUKE). The losses caused by parasitic capacitance and inductance of cable, balun, matching components ($L_{1,2} = 23 \text{ nH}$ with $Q = 35$) and bond wire were measured and calculated as 1.5 dB.

Figures 15 and 16 show the measured output voltage and PCE of the on-chip switched-capacitor charge pump for variable input voltage (180 mV to 300 mV) and loads (0.5 MΩ to 2 MΩ). When the load $R_L = 1 \text{ M}\Omega$ and input voltage $V_{IN} > 210 \text{ mV}$, the output voltage $V_{OUT} > 1 \text{ V}$ and the output power was more than $1 \mu\text{W}$. At $V_{IN} = 0.2 \text{ V}$, the maximum PCE increased to 46.5%.

Figure 17 shows the measured results of the rectifier’s output voltage and PCE for variable loads $R_L = 100 \text{ k}\Omega$ and $200 \text{ k}\Omega$. The measured S11 with frequency in 850 MHz to 1 GHz is shown in Figure 18b. The value of S11 was smaller than -10 dB in range of 900 MHz to 940 MHz, which means the RF port was impedance matched with the antenna. The sensitivity for 1 V output was -18 dBm @ $200 \text{ k}\Omega$, and the maximum PCE was over 57% @ $100 \text{ k}\Omega$.

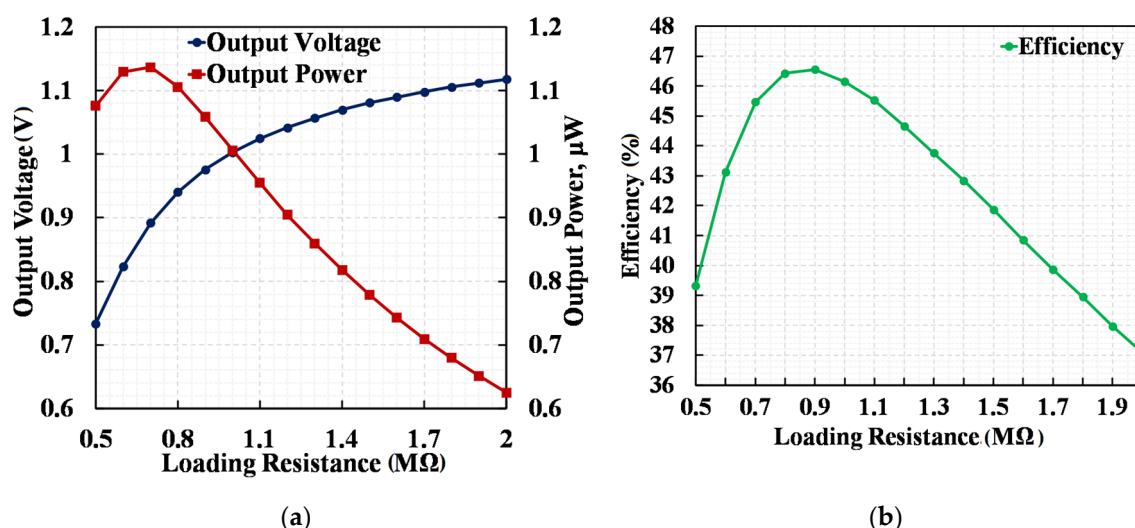


Figure 15. (a) Measured V_{OUT} and P_{OUT} versus R_L @ $V_{IN} = 0.2 \text{ V}$; (b) measured efficiency versus R_L .

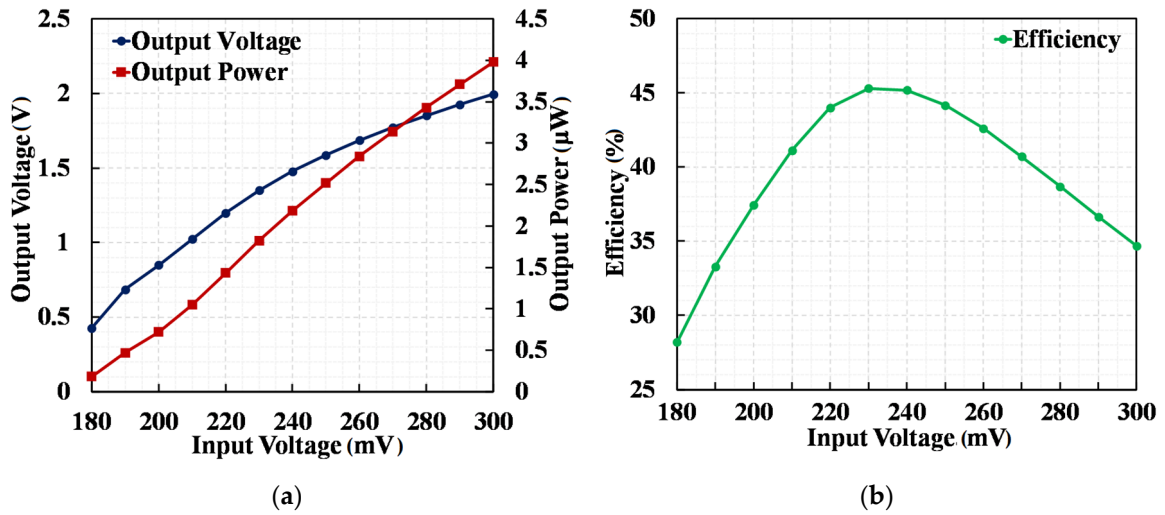


Figure 16. (a) Measured V_{OUT} and P_{OUT} versus V_{IN} @ $R_L = 1\text{ M}\Omega$; (b) measured efficiency versus V_{IN} .

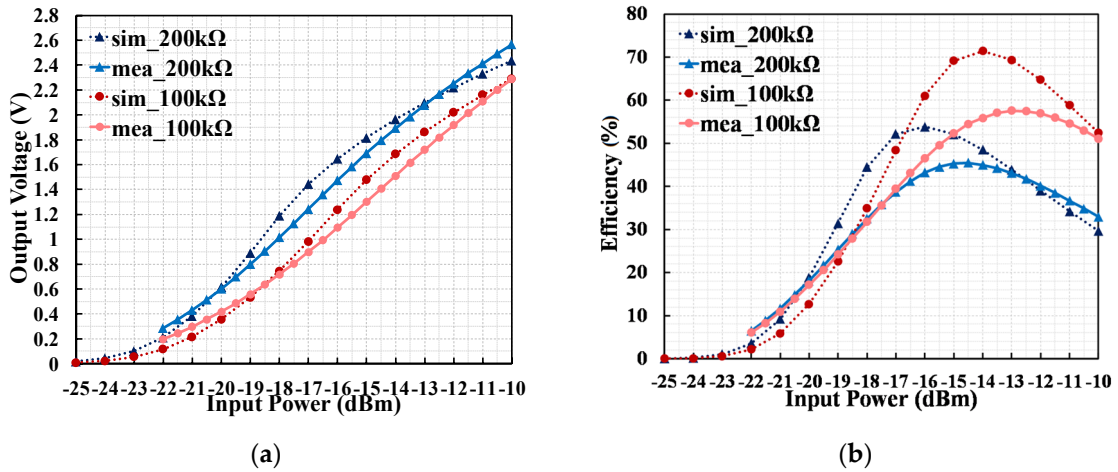


Figure 17. Measurement results of the rectifier, (a) output voltage versus input power for $R_L = 100\text{ k}\Omega$ and $200\text{ k}\Omega$; (b) efficiency versus input power for $R_L = 100\text{ k}\Omega$ and $200\text{ k}\Omega$.

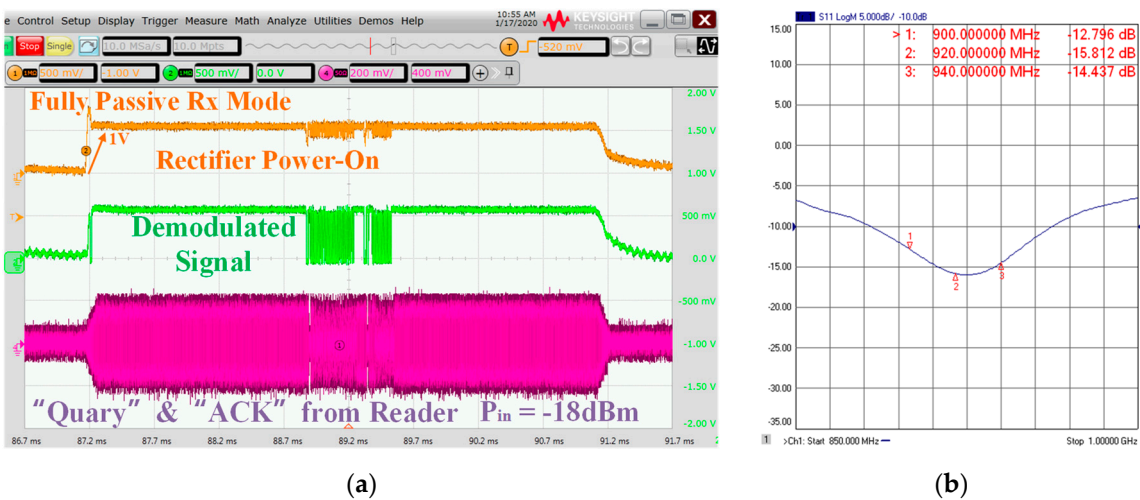


Figure 18. (a) Measured input signal and demodulated signal in low-power (LP) mode; (b) measured S11.

The measured waveforms of the dual-mode receiver are shown in Figures 18a and 19a. The transient waveforms of the input RF signal and demodulated baseband output in the minimum incident power demonstrate the sensitivities were -18 dBm and -40 dBm for LP and HS mode, respectively.

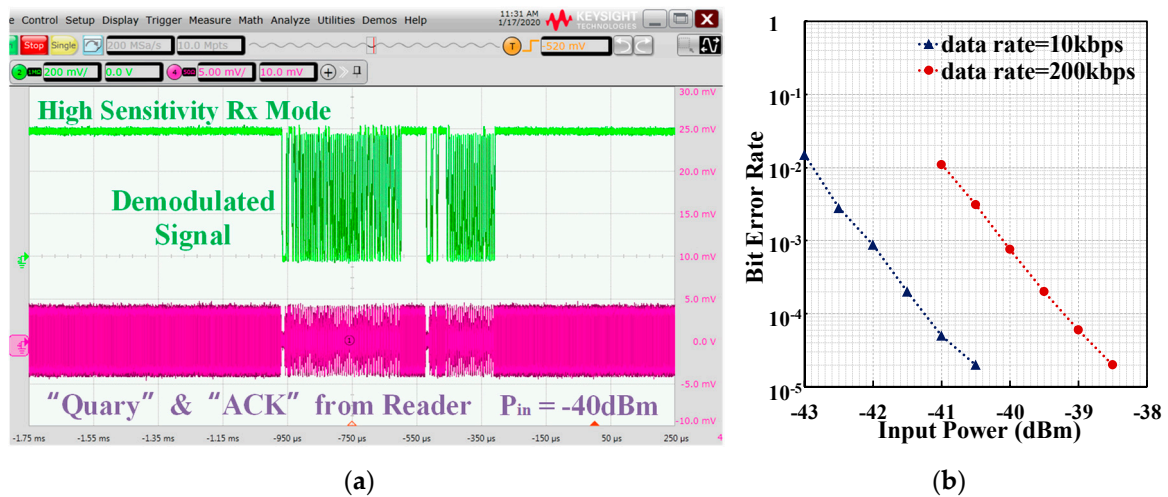


Figure 19. (a) Measured input signal and demodulated signal in HS mode; (b) bit error rate (BER) in HS mode.

In the HS mode with 10 kbps and 200 kbps data rate, the receiver achieved -42 dBm and -40 dBm sensitivity for the bit error rate (BER) <0.001 in 920 MHz as shown in Figure 19b.

The power consumption of each block is shown in Figure 20. The receiver’s total power consumption were 230 nW and 880 nW for LP mode and HS mode, respectively. The energy harvester could provide more than 1μ W of energy in an indoor environment according to the measurement resulted, so the energy was sufficient to the dual-mode receiver.

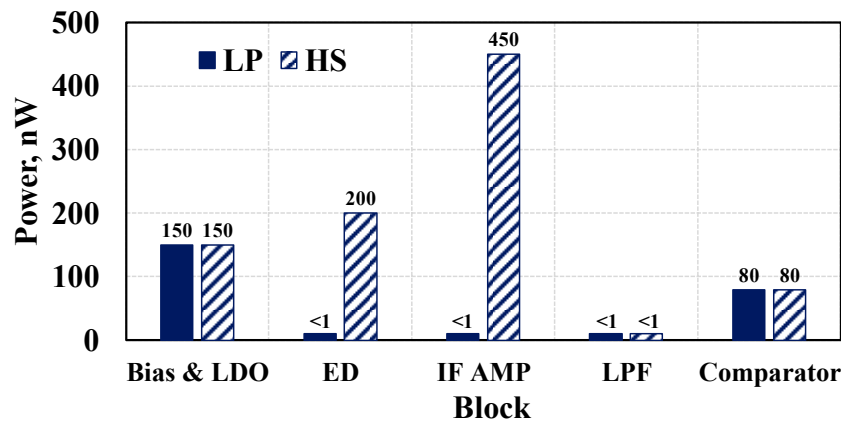


Figure 20. Measured power consumption of each block.

The performance summary is shown in Table 1. The proposed dual-mode receiver achieved relatively high sensitivity without high-Q topology and the proposed architecture was compatible with fully passive operating mode. Furthermore, the RF/PV/TE energy-harvesting approach could eliminate the requirement of battery and extend the lifetime effectively. In this design, small active area, low power consumption and low voltage operation were obtained.

Table 1. Performance summary and comparison with related works.

Parameter	This Work	[6] TIE' 18	[8] Sensors J.' 18	[9] ISSCC' 18
Modulation	OOK	OOK	OOK	OOK
Carrier Frequency	920 MHz	920 MHz	900 MHz	433 MHz
Process	180 nm CMOS	Discrete	95 nm CMOS	130 nm CMOS
Area	0.455 mm ²	>100 mm ²	0.18 mm ²	1.95 mm ²
Energy Harvesting	RF/PV/TE	None	None	None
Receiver Architecture	Passive/Active ED + IF Amp	Envelope Detector	High-Q + Active ED + IF Amp	High-Q + Passive ED + Offset Control
Passive Voltage Gain	8 dB	Not Reported	25 dB	27 dB
Sensitivity	−40 dBm @200 kbps −42 dBm @10 kbps	−39.5 dBm	−55 dBm @10 kbps	−71 dBm @200 bps
Power Consumption	880 nW	>1 mW	1 μW	7.6 nW

6. Conclusions

A self-powered dual-mode receiver is proposed for UHF RFID system, achieving −18 dBm sensitivity for low-power mode and −40 dBm/−42 dBm sensitivity with 200 kbps/10 kbps data rate for high-sensitivity mode, respectively. The integration of tag is increased, and the battery is eliminated due to PV and TE-energy-harvesting topology. It is suitable for low-voltage low-power wireless sensors and implantable devices.

Author Contributions: Conceptualization, P.H. and Z.Z.; supervision, N.M. and Z.Z.; validation, Y.X. and N.M.; writing—original draft, P.H. and N.M.; writing—review and editing, Z.Z. and Y.X. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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