electronics

MDPI

Article

A CMOS Data Transfer System Based on Planar RF Coupling for Reinforced Galvanic Isolation with 25-kV Surge Voltage and 250-kV/µs CMTI

Egidio Ragonese [1,*], Nunzio Spina [2], Alessandro Parisi [2] and Giuseppe Palmisano [1]

[1] Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), University of Catania, 95125 Catania, Italy; giuseppe.palmisano@unict.it

[2] STMicroelectronics, 95121 Catania, Italy; nunzio.spina@st.com (N.S.); alessandro.parisi@st.com (A.P.)

* Correspondence: egidio.ragonese@unict.it; Tel.: +39-095-7382331

Received: 9 May 2020; Accepted: 29 May 2020; Published: 5 June 2020

Abstract: This paper exploits an effective approach to overcome the breakdown limitations of traditional galvanic isolators based on chip-scale isolation barriers, thus achieving a very high isolation rating (i.e., compliant with the reinforced isolation requirements). Such an approach is based on radio frequency (RF) planar coupling between two side-by-side co-packaged chips. Standard packaging along with proper assembling techniques can be profitably used to go beyond 20-kV surge voltage without using expensive or exotic isolation components. As a proof of concept, a bidirectional data transfer system based on RF planar coupling able to withstand an isolation rating as high as 25 kV has been designed in a low-cost standard 0.35-µm CMOS technology. Experimental measurements demonstrated a maximum data rate of 40 Mbit/s using a carrier frequency of about 1 GHz. The adopted approach also guarantees a common mode transient immunity (CMTI) of 250 kV/µs, which is a first-rate performance in view of next generation galvanic isolators for wide-bandgap power semiconductor devices, such as gallium nitride high-electron mobility transistors (GaN HEMTs) and silicon carbide (SiC) MOSFETs.

Keywords: CMOS technology; galvanic isolation; integrated circuits; on-chip inductors; electromagnetic coupling; surge voltage; package; wide-bandgap power semiconductors

1. Introduction

In the last decade, several applications take advantage of galvanic isolation to improve safety and reliability, especially in harsh environments. Galvanic isolation is required in the automotive applications (i.e., electric and hybrid vehicles), in the industrial environment (i.e., motor control, automation, etc.), in medical equipment, in consumer products (i.e., home appliance, inductive cooking, etc.) and even in communication networks. A galvanic isolator guarantees data transfer across a galvanic barrier and enables bidirectional communication between two isolated interfaces. A typical galvanically isolated system is depicted in Figure 1. Data communication must be assured not only in the presence of the static difference of potential between the ground references, but also when a rapid shift of grounds occurs. Therefore, a key performance parameter of a galvanic isolator is the common mode transient immunity (CMTI), whose typical values range from 50 to 100 kV/µs. However, the CMTI requirements are becoming more demanding (i.e., >200 kV/µs) due to the higher switching frequencies allowed by wideband power devices, such as gallium nitride high-electron mobility transistors (GaN HEMT) and silicon carbide (SiC) MOSFETs.

According to recent standardization [1], semiconductor galvanic isolators must withstand high voltages not only for short periods of time (i.e., namely the maximum transient isolation voltage), but

also throughout the device lifetime (i.e., namely the maximum repetitive voltage). However, the most stringent specification is represented by the maximum surge isolation voltage, V_{SURGE}, that quantifies the capability of the isolator to withstand very high voltage impulses of a certain transient profile, which can arise from indirect lightning strikes or faults. At the component level, the reinforced isolation level is achieved if the V_{SURGE} is higher than 10 kV. At the present time, both industrial and automotive applications are moving towards 10 kV, some applications. (e.g., patient monitoring systems) already require a V_{SURGE} higher than 15 kV, while galvanic isolation up to 20 kV will be required very soon. State-of-the-art galvanic isolators are based on electromagnetic (EM) coupling (i.e., capacitive or inductive) across a dielectric layer (i.e., the galvanic barrier). Such isolators use either integrated SiO_2 or a post-processed polyimide layer. They present inherent limitations in terms of isolation that have been improved only by means of expensive and time-consuming technological arrangements. Moreover, traditional isolation barriers are hardily compliant with CMTI better than 150 kV/µs, thus preventing the highest switching speed operation of wide-bandgap power transistors.

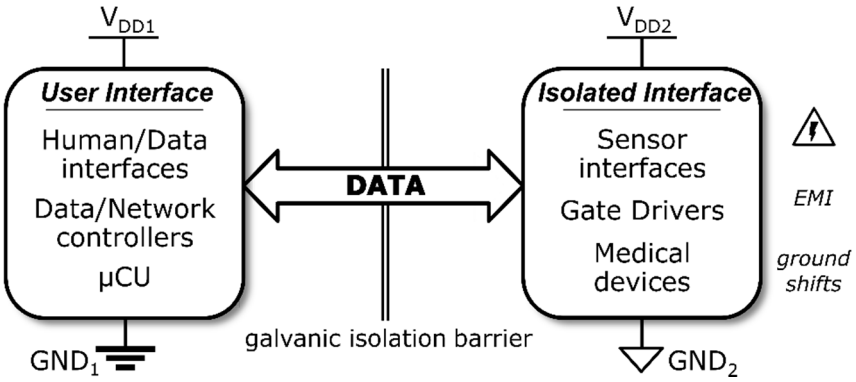

Figure 1. Simplified block diagram of a galvanically isolated system.

This paper explores an alternative approach to overcome both breakdown voltage (BV) and CMTI limitations of semiconductor isolators without reducing the level of integration (i.e., a two dice system-in-package). The approach is based on radio frequency (RF) planar coupling between two side-by-side co-packaged chips [2]. The paper is organized as follows. A brief overview of the main isolation technologies is reported in Section 2, while the RF planar isolation approach is discussed in Section 3 along with the circuit design of the data transfer system. The experimental performance is detailed in Section 4 along with the comparison with the state-of-the-art, and final conclusions are drawn in Section 5.

2. Technologies for Chip-Scale Galvanic Isolators

An integrated galvanic barrier can be implemented by using silicon dioxide (SiO_2), which exhibits a breakdown voltage (BV) of about 1000 V/µm [3], sometimes in combination with silicon nitride (Si_3N_4) and oxynitride (SiON) to further improve its isolation rating [4]. Oxide galvanic isolation has been successfully exploited in recent years for highly integrated isolated data [5–7] and power transfer interfaces [8–12] by means of on-chip capacitors or stacked transformers. However, oxide insulation can reliably provide a limited surge capability (typically 5–6 kV), since increasing the oxide thickness produces wafer mechanical stress and second order BV effects. The use of two series-connected galvanic isolation barriers, namely double isolation, can be exploited to improve the overall isolation rating. This is a viable solution for digital isolators (i.e., only data transfer) [13], with a maximum V_{SURGE} around 13 kV by using a couple of isolation capacitors [14].

The galvanic barrier can be also implemented with other dielectric layers, such as the polyimide, traditionally used in semiconductor industry for stress relief. In this case, the isolation device (typically

a stacked transformer) is built as a stand-alone chip by using a custom technology at the cost of reducing the integration level (i.e., from two to three chips per each isolated channel).

This approach guarantees high data rates with a very good isolation rating and CMTI performance [15], while being also suited to a power transfer up to several hundreds of mW [16]. Due to a poorer polyimide BV, typically the isolation layer is about 3x thicker to sustain the same surge voltage of an oxide barrier. On the other hand, very thick polyimide layers can be manufactured with a record of 32.5-µm thickness able to withstand 20 kV [15], which is not feasible using silicon dioxide layers. In any case, isolation approaches, based either on integrated SiO_2 barriers or post-processed polyimide transformers, have inherent limitations in terms of isolation due to the maximum dielectric thickness that can be reliably manufactured. Little improvements can be achieved at the cost of expensive and time-consuming technological advances.

However, galvanic isolation can be also provided by substituting chip-scale isolation barriers (i.e., SiO_2 or polyimide capacitors and transformers) with a package-scale isolation one. In other terms, packaging/assembling techniques and RF coupling between micro-antennas can be properly used to provide isolation and data communication. Some RF galvanic isolators exploit wireless transmission between two stacked chips by means of silicon integrated near-field antennas [17]. To reduce the distance between stacked antennas, the dice can be also assembled face-to-face at the cost of fabricating through holes vias to have a rear side connection [18,19]. A very high isolation rating can be achieved by using proper dielectric isolator films between the dice (i.e., glass, polyimide die attach film etc.). However, the chip assembling complexity and package cost have hindered a widespread adoption of this isolation technology. These drawbacks can be avoided if dice are placed side by side on the package substrate exploiting the magnetic coupling between coplanar antennas. In this case, the physical channel for data communication exploits the weak near-field coupling between two micro-antennas integrated on two side-by-side co-packaged chips (i.e., chip 1 and chip 2), as shown in Figure 2. In this approach, the distance through insulation (DTI), which is responsible for the isolation rating, can be properly increased to guarantee the required V_{SURGE}. Standard molding compounds have a dielectric strength (E_M) of at least 50 V/µm, and therefore with a DTI of about 400–500 µm, an isolation rating higher than 20 kV can be achieved [20,21]. Moreover, the intrinsic parasitic capacitance of the isolated channel is extremely low if compared with the ones of traditional chip-scale barriers (i.e., isolation capacitors or stacked transformers), thus reducing common mode (CM) currents produced by rapid ground shifts (i.e., CM transients).

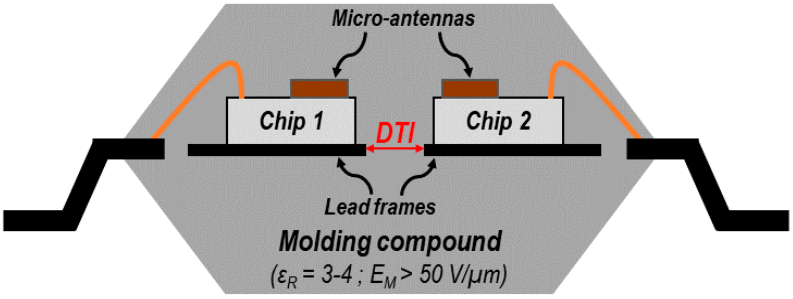

Figure 2. Side-by-side co-packaged chips with RF coupled planar micro-antennas.

3. Fabrication Technology and System Description

The proposed isolated data transfer system is made up of two chips integrated in a low-cost 0.35-µm CMOS technology provided by STMicroelectronics to be packaged in a standard plastic package on two separated lead frames. The distance between the lead frames (i.e., the DTI in Figure 2) was set to 500 µm to guarantee an isolation rating well above 20 kV. The simplified block diagram of an isolated data transfer channel is shown in Figure 3. Each communication channel exploits two dedicated micro-antennas integrated on chips 1 and 2 for data transmission (TX) and reception (RX), respectively. The EM coupling between the planar antennas through the package molding compound

determines the attenuation of the isolated channel, which must be minimized by a proper design of the antenna geometries, as discussed in Section 3.1. Due to the weak EM coupling, the system is designed for narrowband RF operation with both TX and RX antennas in the resonant mode, which are properly tuned at the working frequency. Data transmission exploits the on-off keying (OOK) pulse width modulation (PWM) of an RF carrier (see Figure 4), since it also provides an easy way for clock recovering. Typically, the value of the carrier frequency, f_{RF}, is a tradeoff among contrasting performance parameters, such as antenna coupling and silicon area from one side and current consumption to the other. In this work, an RF carrier frequency of about 1 GHz was chosen, being in some extent also limited by the poor f_T performance of the adopted 0.35-µm CMOS node (i.e., about 27 GHz). The voltage supply, V_{DD}, was set to 3.3 V. As shown in Figure 3, chip 1 also includes a TX front-end driven by a base-band interface (i.e., PWM modulator), while chip 2 consists of an RX front-end with a base-band interface for data demodulation (i.e., PWM demodulator). The following subsections will detail the design of the overall isolated data transfer system, i.e., the micro-antennas, the TX front-end, the RF-front-end and the PWM modulator/demodulator.

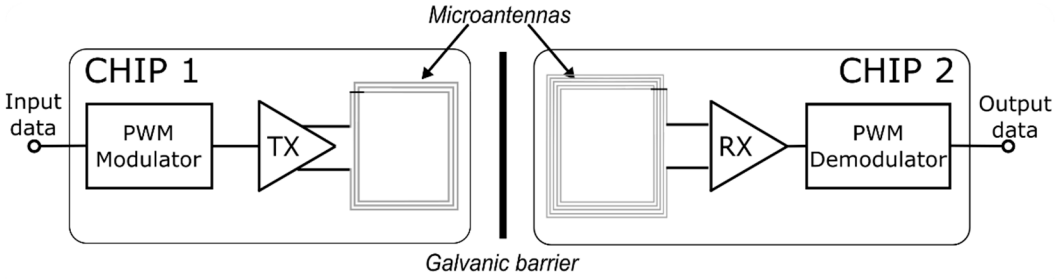

Figure 3. Block diagram of the isolated data channel based on RF planar coupling.

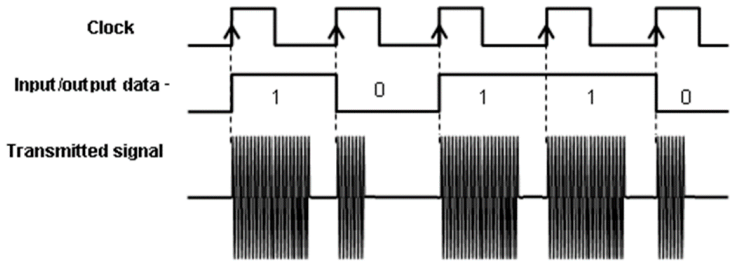

Figure 4. Simplified waveforms for clock, data and pulse width modulation (PWM) modulated RF carrier.

3.1. On-Chip Micro-Antennas

The key point of the proposed isolation approach is the maximization of the EM coupling between the TX and RX antennas. To this aim, it is of utmost importance to reduce the energy loss occurring into both the metal spirals and silicon substrate, which turns in a higher quality factor (*Q*-factor) of the antennas and better EM coupling between them. In particular, the antenna coupling is considerably affected by the substrate conductivity, σ_S, mainly due to the magnetically induced substrate eddy currents [22]. In this work, the antennas were designed by taking advantage of the top Al layers of the adopted CMOS technology (i.e., 3-µm metal 4 and 1-µm metal 3). The design was carried out by using EM simulations and to this aim the simulator set-up was preliminary verified by taking advantage of the *S*-parameter measurements of both the on-wafer single antennas and coupled antennas mounted on a testing PCB, as shown in Figure 5 [23]. The first step of the design was the definition of the antenna geometry in terms of shape, number of turns (n), metal width (w), metal spacing (s) and outer diameter (d_{OUT}). It was mainly accomplished by means of extensive 2D EM simulations in Keysight ADS Momentum, while the time-consuming 3D EM simulations (i.e., Ansoft HFSS) were exploited in the final phase to obtain more precise results. To guarantee more than a 20-kV isolation rating, the DTI

between the lead frames was set to 500 µm, which turned in 650 and 730 µm between the chips and the antennas, respectively. Although circular or polygonal spirals achieve a better *Q*-factor performance, the square shape was preferred for both the TX and RX antennas since this allows optimizing the inductance/area ratio while improving the planar coupling between coils. The minimum metal spacing allowed by the technology was adopted (i.e., 2.75 µm) to maximize coil self-inductance. The number of turns, n, and diameter, d_{out}, were chosen to tradeoff the inductance value and the coil area, while the metal width, w, was set to tune the *Q*-factor and the self-resonance frequency (*SRF*). Moreover, a turn ratio (i.e., n_{RX}/n_{TX}) of about 1.7 was exploited to step up the signal received by chip 2. The result of the antenna design optimization is reported in Table 1 which summarizes the geometrical parameters of the TX and RX antennas, while Figure 6a shows the antenna layout. Figure 6b shows the antenna 3D simulations carried out in HFSS. A standard molding compound with a dielectric constant, ε_R, equal to 3 was included to account for the package capacitive effects, which are fundamental to estimate the CMTI performance of the isolated channel.

To fully understand the impact of the most important design and process parameters on the antenna performance, some EM parametric simulations are reported hereinafter. Figure 7 shows the EM coupling in terms of insertion loss (i.e., $IL = -20\log S_{21}$) between the TX/RX antennas that are spaced by 730 µm (i.e., 500 µm between lead frames). *IL* is given for the different substrate conductivities, σ_S, which range from 0.1 to 10^4 S/m (i.e., from very low to very high conductivity substrate). At low values of σ_S, *IL* is quite constant, while it rises for σ_S higher than 10^3 with a coupling degradation of 13 dB at $\sigma_S = 10^4$ S/m. Therefore, typical substrate conductivity values of standard CMOS and BiCMOS technologies are fully compatible with the proposed RF planar isolation approach, whereas those of standard BCD technologies (in the order of 10^4 S/m) are critical values and require more complex implementations. Figure 8 represents the variation of *IL* at increasing values of DTI and hence at increasing values of the isolation rating, for a molding compound dielectric strength, E_M, of about 50 V/µm. The *IL* curve at 1 GHz exhibits a slope of about 0.6 dB/kV and at 500-µm DTI, corresponding to an isolation rating of 25 kV, the *IL* is about 54 dB. Finally, Figures 9 and 10 show the simulated inductance and *Q*-factor of the TX and RX antennas at 500-µm DTI, respectively, while *IL* as a function of frequency is reported in Figure 11.

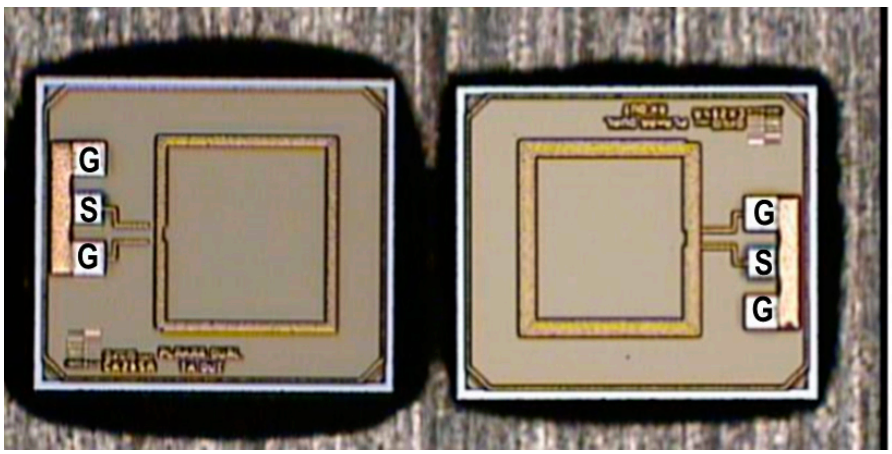

Figure 5. On-chip planar antennas mounted on a testing PCB for the *S*-parameter measurements.

Table 1. Geometrical parameters of transmission (TX) and reception (RX) antennas.

Antenna	n	s [µm]	w [µm]	d_{OUT} [µm]
TX (chip 1)	3	2.75	9.6	550/650
RX (chip 2)	5	2.75	6	550/650

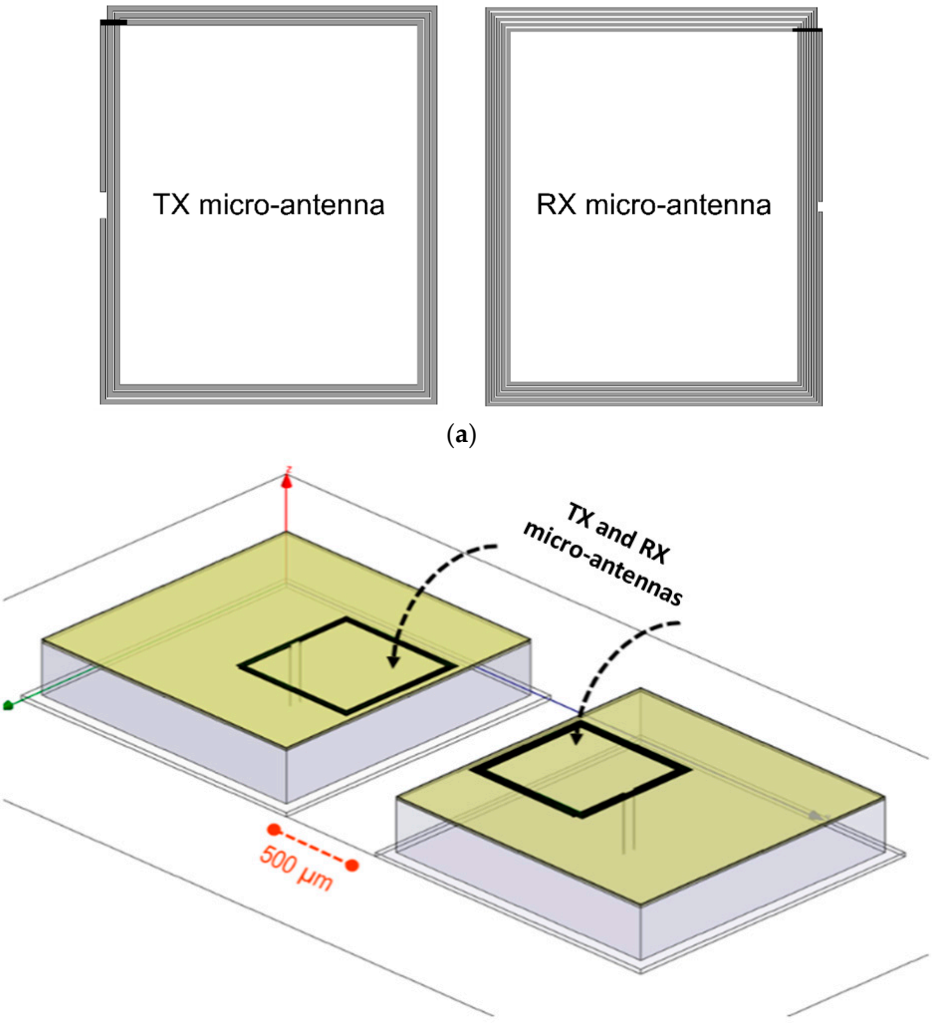

Figure 6. (**a**) Layout of the micro-antennas of Table 1; (**b**) 3D EM simulations of the micro-antennas.

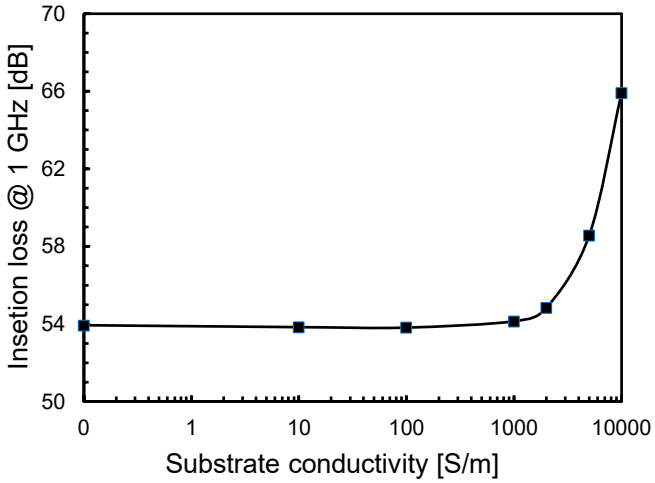

Figure 7. Antenna coupling insertion loss at 1 GHz as a function of the substrate conductivity, σ_S, for a distance through insulation (DTI) of 500 µm (i.e., antenna distance of 730 µm).

Although *IL* is usually used to account for the loss of a passive component, it does not represent the actual coupling loss between the TX and RX antennas since it is calculated with 50-Ω terminations, whereas the RX input impedance, Z_{IN_RX}, is usually quite high. Moreover, the antennas are operated in the resonant mode in the actual application. A suitable parameter is instead the TX-to-RX coupling loss, *TRX*, in open-circuit (or high-impedance) conditions. For the designed antennas, the TX-to-RX coupling loss in an open-circuit condition, TRX_{OC}, at 1 GHz is about 43 dB (i.e., 11 dB lower than the *IL*), which is further reduced in the resonant mode down to 25 dB (i.e., 29 dB lower than the *IL*). In a more real condition, with a finite value of Z_{IN_RX} of about 10 kΩ, *TRX* at 1 GHz in the resonant mode is about 27 dB (instead of 25 dB). This last value represents the starting point for the design of the isolated data transfer channel according to the block diagram in Figure 3. For the sake of completeness, the inductance, the *Q*-factor, the *IL* and the magnetic coupling factor at 1 GHz (L_{1GHz}, Q_{1GHz}, IL_{1GHz}, k_{1GHz}) are reported in Table 2 for both the TX and RX antennas, along with the *SRF* and the TX-to-RX coupling losses at 1 GHz in the resonant mode in open-circuit (TRX_{OC}) and 10-kΩ ($TRX\_{10k\Omega}$) conditions.

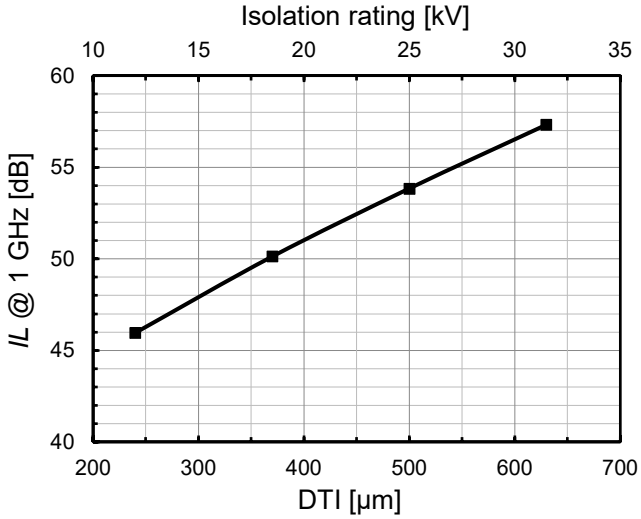

Figure 8. Antenna coupling *IL* at 1 GHz as a function of the DTI and corresponding galvanic isolation rating in the adopted 0.35-µm CMOS technology (σ_S = 10 S/m; E_M = 50 V/µm).

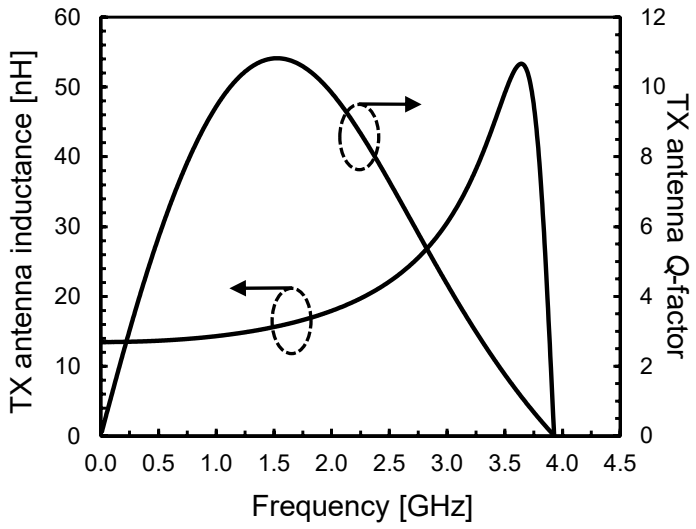

Figure 9. Inductance and *Q*-factor of the TX antenna as a function of frequency.

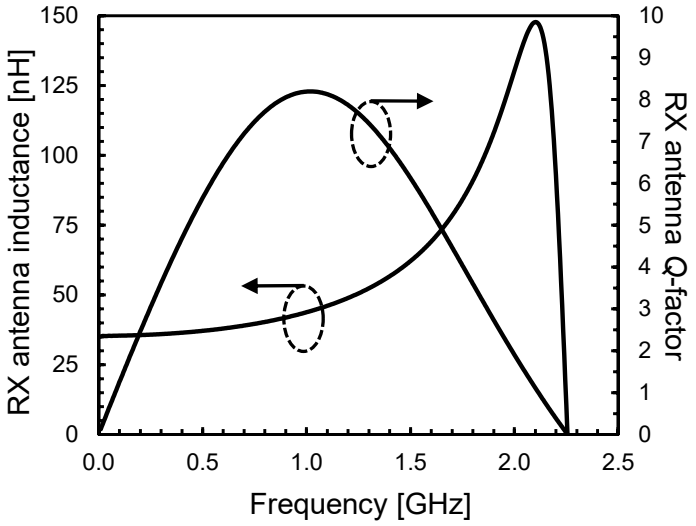

Figure 10. Inductance and *Q*-factor of the RX antenna as a function of frequency.

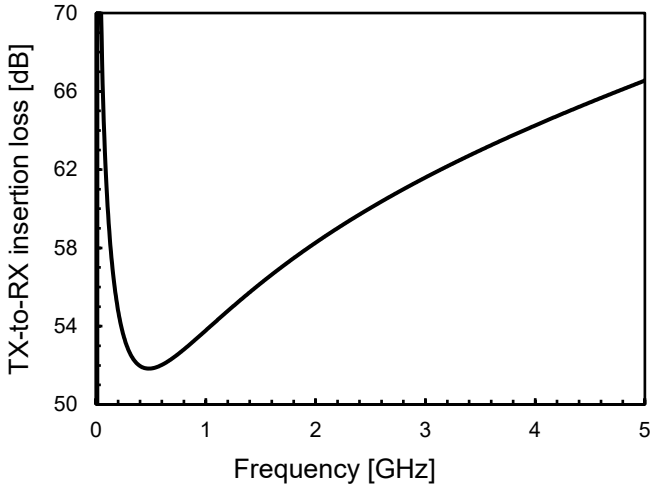

Figure 11. TX-to-RX coupling *IL* as a function of frequency.

Table 2. Electrical parameters of TX and RX antennas.

Antenna	L_{1GHz} [nH]	Q_{1GHz}	SRF [GHz]	k_{1GHz}	IL_{1GHz} [dB]	$TRX_{\_OC}$ [dB]	$TRX_{\_10k\Omega}$ [dB]
TX (chip 1)	14.3	9.4	3.93	0.004	54	25	27
RX (chip 2)	43.8	8.2	2.25				

3.2. TX Front-End

For a better robustness, a PWM technique with an RF carrier was adopted. A baseband PWM modulator is used to generate the PWM signal, PWM_{IN}, which drives the transmitter, TX, as shown in Figure 3. In this work, the PWM modulator is implemented by means of a simple digital scheme, as depicted in Figure 12. The input data, D_{IN}, is first synchronized with the input clock, CK_{IN}, by means of the D flip-flop, DFF1. The synchronized input data, D_{SYNC}, and the elongated version of the clock signal, CK_L, are used to produce the data signal, D_1, which differs from D_{SYNC} for a reduced bit time duration. Finally, D_0 is generated by the D flip-flop, DFF2, driven by the voltage supply, V_{DD}, clocked by CK_{IN} and reset by the delayed clock signal, CK_D. The resulting PWM signal is easily obtained as the sum of D_0 and D_1 and consists of pulse train at the data rate frequency, f_D, with the bit time durations T_0 and T_1 for bits "0" and "1", respectively. As an example, for an f_D of 40 Mbit/s, the bit

time durations T_0 and T_1 are 18 ns and 8 ns, respectively, with a minimum time guard between a falling edge and the next rising edge of 7 ns. By varying f_D, both T_0 and T_1 change accordingly, but the minimum time guard remains fixed at 7 ns. For the sake of completeness, Figure 13 displays the PWM modulator signals for an f_D of 40 Mbit/s and the bit sequence "110101".

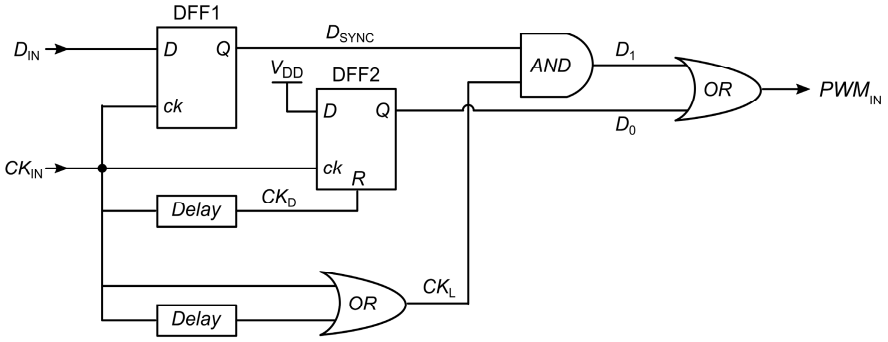

Figure 12. Simplified schematic of the TX baseband PWM modulator.

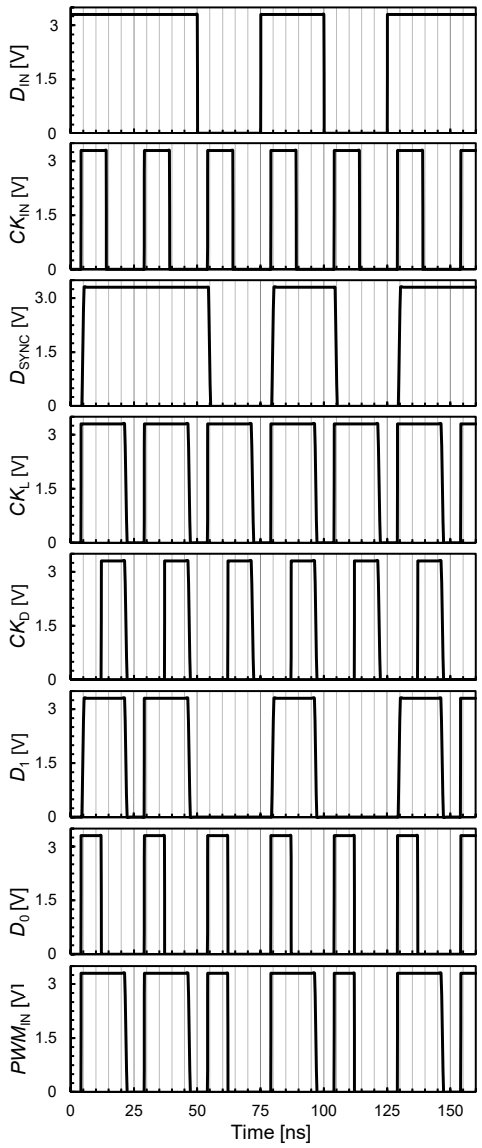

Figure 13. PWM modulator signals for a data rate frequency (f_D) of 40 Mbit/s and bit sequence "110101".

The TX front-end was implemented by means of an RF oscillator by exploiting the TX spiral antenna inductance for the resonant tank. Indeed, the oscillator can be properly turned on and off by using MOS switches controlled by the PWM signal. The main design issues are related to the co-design between the RF oscillator and the TX antenna, as well as the reduction in the current consumption for a given oscillation voltage and the minimization of the start-up time. In this work, an inductor-loaded complementary cross-coupled oscillator was adopted, as shown in Figure 14. Compared with the traditional NMOS cross-coupled oscillator, this topology maximizes the oscillation amplitude within the supply voltage, thus avoiding the need for special thick oxide/lateral transistors with high breakdown voltages [11,12], which are not usually available in standard CMOS technologies. On the other hand, the use of complementary MOS transistor couple pairs give the advantage of nearly double the transconductance at the same current level compared with a simple cross-coupled oscillator, also minimizing the startup-time. An additional capacitor, C_2, of about 800 fF was added to tune the oscillator at about 1 GHz. The TX oscillator produces a full swing oscillation (i.e., amplitude about equal to V_{DD}) with a current consumption of 4.5 mA. The total current consumption of the TX section is dominated by the oscillator contribution, which is also a critical parameter of the overall system.

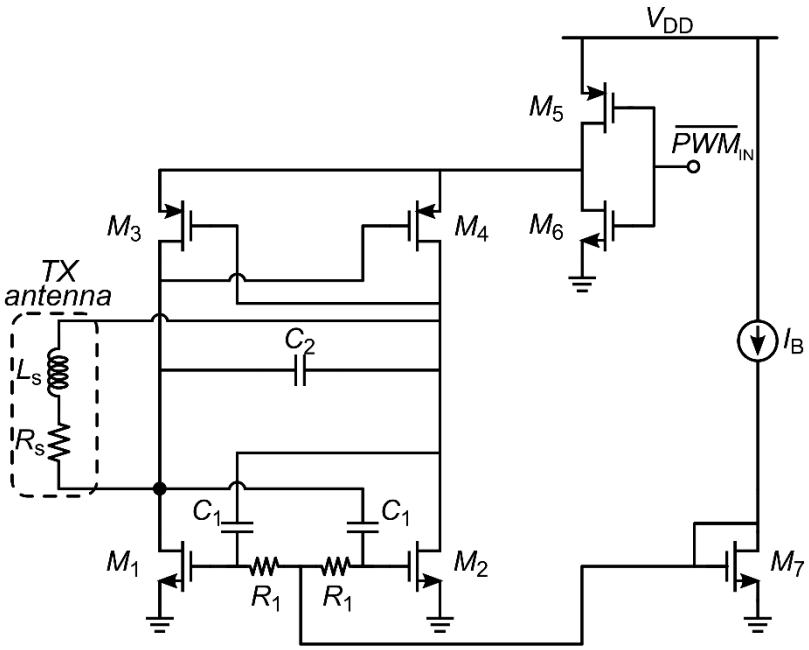

Figure 14. Simplified schematic of the RF oscillator of the TX front-end.

3.3. RX Front-End

The rail-to-rail TX signal is greatly attenuated (of about 27 dB) through the isolated channel and therefore the RX front-end must raise it before the rectification and data demodulation. Figure 15 shows the simplified schematic of the RX front-end. It consists of a differential amplifier with resistive load to minimize the silicon area. The signal at the RX antenna is around 140 mV, and the amplifier stage raises up it to around 400 mV (i.e., 8.4-dB voltage gain) with a current consumption of 1 mA. Then, a double-balanced mixer based on a Gilbert cell is exploited as rectifier stage. The output RC load of the mixer guarantees a low-pass filtering to clean the RX signal envelope. The rectification stage provides an additional gain of about 8 dB with a current consumption of 0.6 mA. Finally, the rectified signal is compared with a threshold level to recover the original TX PWM signal. The choice of the threshold determines the RX immunity to noise. In worst case conditions, the minimum amplitude of the rectified signal is higher than 500 mV and thus a 450-mV threshold was adopted. Figure 16 shows the amplified RX signal (i.e., mixer input voltage) and the RX envelope voltage (i.e., the mixer output voltage) along with the threshold voltage adopted for the reconstruction of the PWM signal.

Finally, Figure 17 shows the base-band circuit used for the PWM demodulator, which recovers clock, CK_{OUT}, and data, D_{OUT}, from the PWM_{OUT} signal, as displayed in Figure 18.

The adopted planar isolation approach is very effective also in terms of CMTI since the isolated channel exhibits a very low parasitic capacitance (i.e., below 5 fF) compared with typical values of traditional isolators. Of course, the adoption of a fully differential architecture is mandatory to reject the induced CM transients. However, a correct estimation of the CMTI performance needs to accurately account for process mismatches by means of Montecarlo (MC) simulations. Figure 19 shows the MC simulation of the isolated data link at 40 Mb/s in the presence of a 250-kV/µs CM disturbance. As is apparent, the OOK-modulated signal at the RX antenna is not significantly affected by the CM disturbance and accurate data, D_{OUT}, and clock, CK_{OUT}, demodulation are obtained.

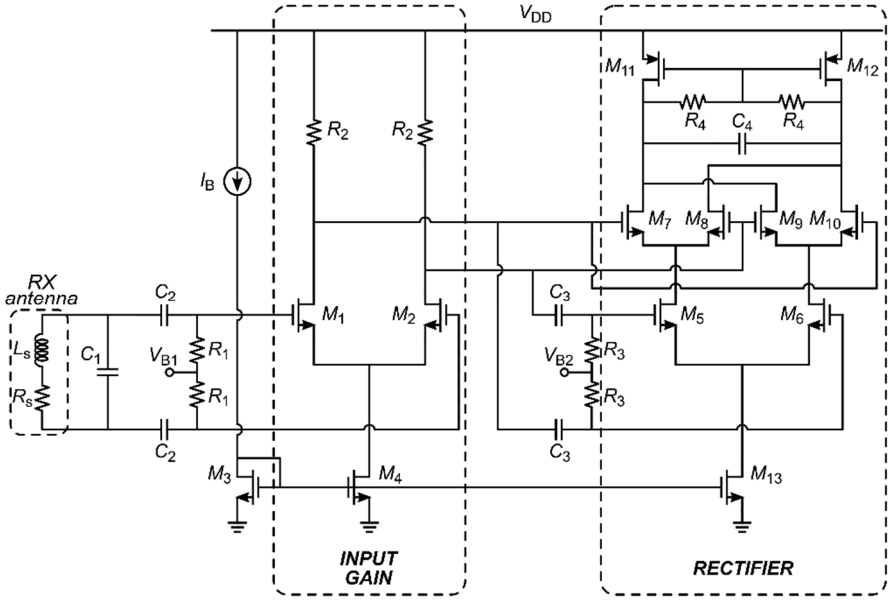

Figure 15. Simplified circuit of the RX RF front-end.

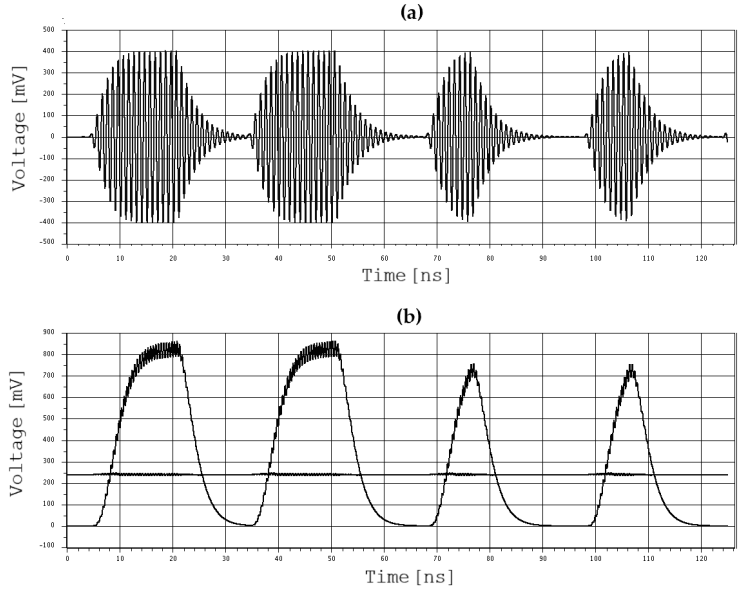

Figure 16. (**a**) Mixer input voltage; (**b**) RX envelope voltage and threshold voltage for PMW reconstruction (f_D = 33 MHz).

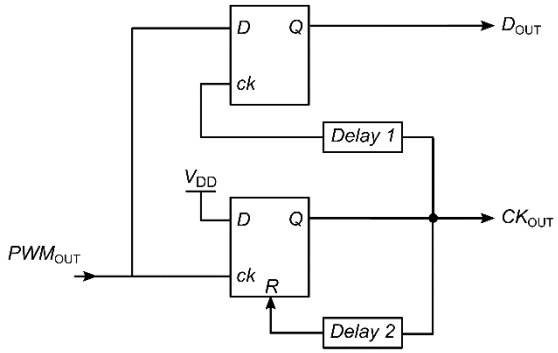

Figure 17. Simplified schematic of the RX base-band PWM demodulator.

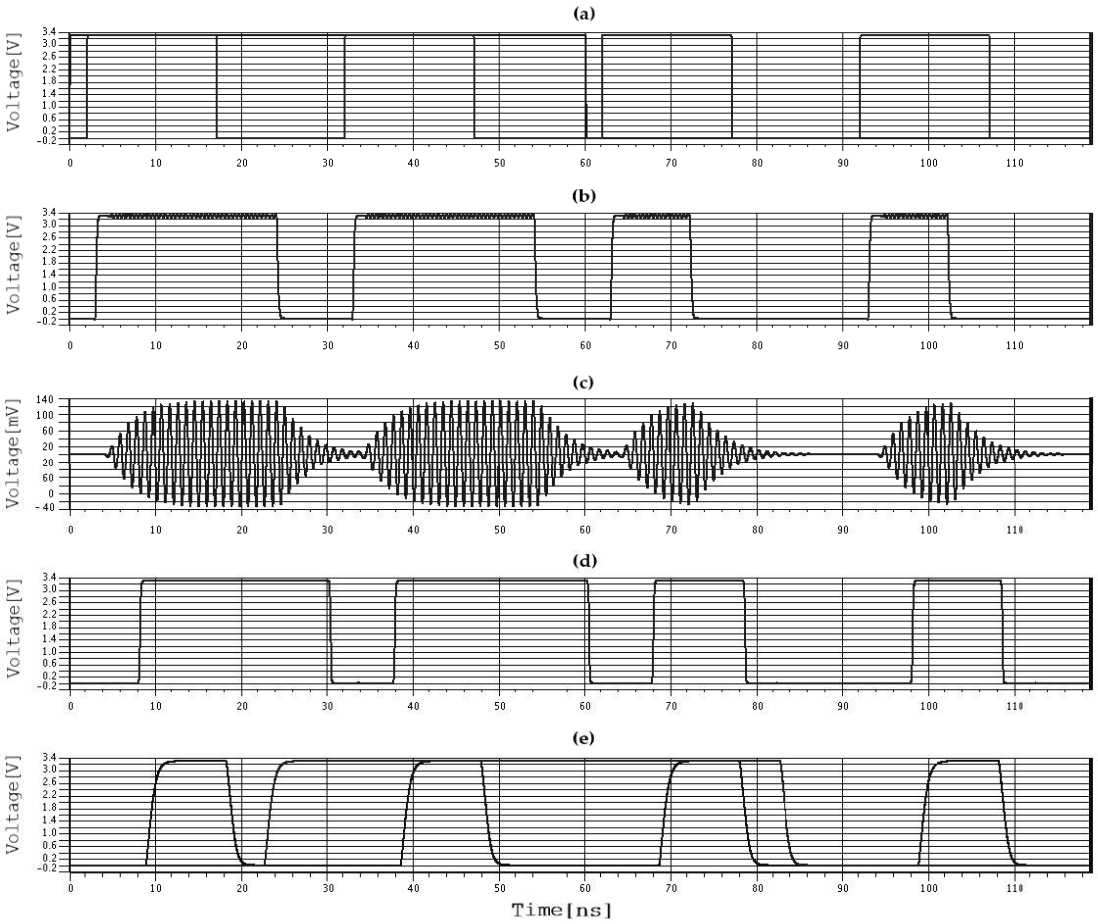

Figure 18. (**a**) CK_{IN} and D_{IN}; (**b**) PWM_{IN}; (**c**) RX antenna signal; (**d**) PWM_{OUT}; (**e**) CK_{OUT} and D_{OUT} (f_D = 33 Mb/s).

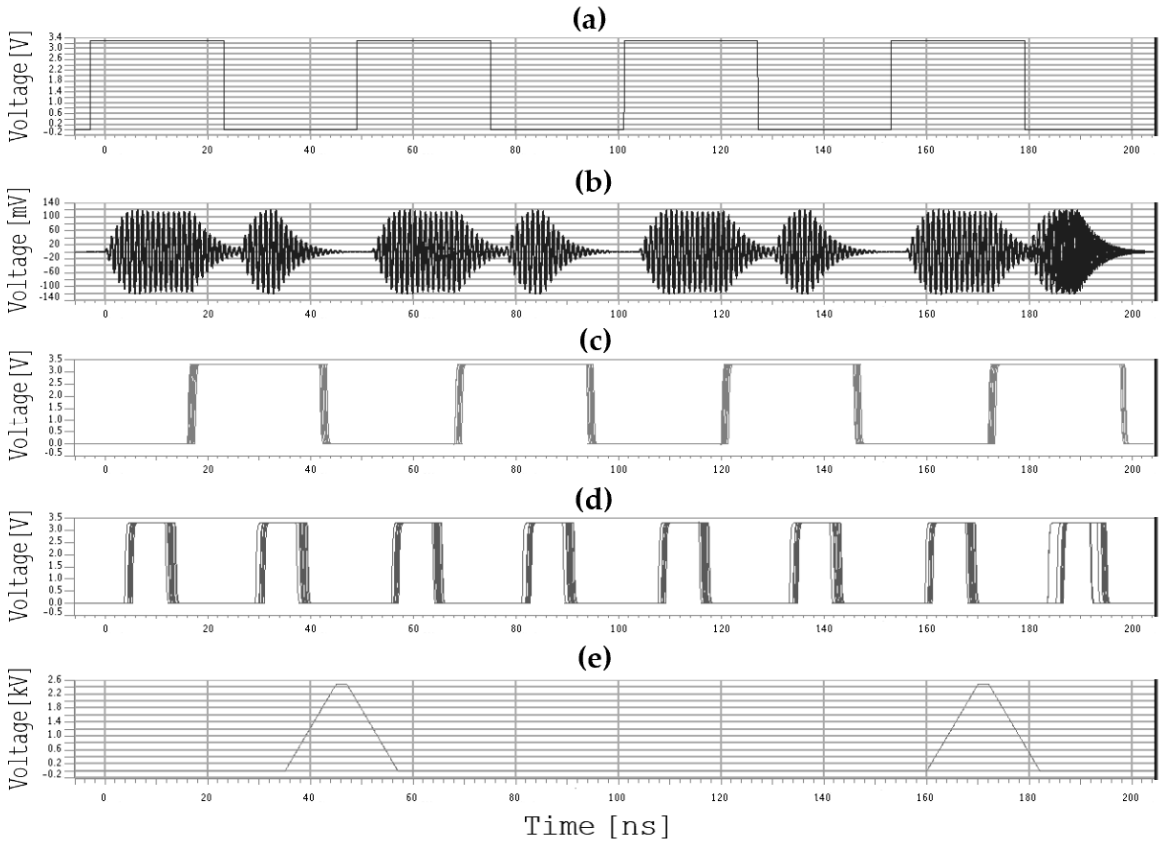

Figure 19. Isolated data link simulations in the presence of a 250-kV/µs common mode (CM) disturbance (f_D = 40 Mb/s, Montecarlo (MC) runs = 200, σ = 4). (**a**) D_{IN}; (**b**) RX antenna voltage; (**c**) D_{OUT}; (**d**) CK_{OUT}; (**e**) common mode transients (CMTs).

4. Experimental Results

The bidirectional isolated data transfer system was implemented by using two identical dice, each including both TX and RX circuitry, as shown in the photograph of Figure 20. The overall die size is 2820 µm × 1340 µm. However, the TX active area including the antenna is only 700 µm × 550 µm, while the RX area is 960 µm × 550 µm. As depicted in Figure 21, the chips were assembled side-by-side on the metal frame with a DTI of 500 µm, thus obtaining a bidirectional data transfer system with very high galvanic isolation, provided that a standard molding compound with the dielectric strength, E_M, of about 50 V/µm will be used for packaging. A distance between the isolated channels of about 1700 µm was adopted to reduce the cross-talk at the expense of a higher area consumption. Experimental measurements were carried out at 3.3-V voltage supply up to a data rate of 40 Mbit/s and confirmed the simulated performance.

Table 3 summarizes the measured performance of the proposed galvanically isolated data transfer system in comparison with the state-of-the-art of galvanic isolators. The comparison is carried out with the best-in-class transformer-based isolator in terms of isolation rating and CMTI [15], as well as with a chip-scale isolator in a standard technology in [24] and package-scale isolators based on stacked or planar coupling [19,25]. The work in [15] achieves a first-rate 20-kV isolation rating and 200-kV/µs CMTI thanks to a dedicated thick polyimide transformer (i.e., 32.5-µm thickness). However, such a performance is guaranteed only at a very low data rate (i.e., 1 Mb/s) and hence quite high energy per bit, E_{BIT}, (i.e., 4.8 nJ/ns). On the other hand, the implementation of a very thick polyimide layer is not trivial in terms of the process complexity and costs. A package-scale isolation barrier implemented by means of face-to-face stacked chips bonded with a die attach film (DAF) (as previously claimed by patent [18]) is exploited in [19] to attain an isolation rating of nearly 10 kV in a 0.25-µm SOI BiCDMOS technology. However, this package-scale galvanic isolator exhibits poor performance

in terms of both data rate, f_D, propagation delay, t_p, and energy per bit, E_{BIT}, while no CMTI value is provided. Moreover, the isolator performance is extremely sensitive to chip alignment, which increases the complexity and cost of the solution. The work in [24], which explores lateral coupled resonators with gap silicon oxide isolation, has the advantage of providing more than 4.5-kV galvanic isolation in a standard 0.25-µm BCD technology without any dedicated isolation component (i.e., thick oxide/polyimide capacitors/transformers). Despite the very good data rate and propagation delay performance, it suffers from the highest current per channel, I_{DD_CH}, and high E_{BIT}, as [15] and [19]. Moreover, no CMTI performance is given, which could be considerably degraded by the high parasitic fringing capacitances of the adopted laterally coupled isolation structures due to the narrow oxide gaps (i.e., 3-µm).

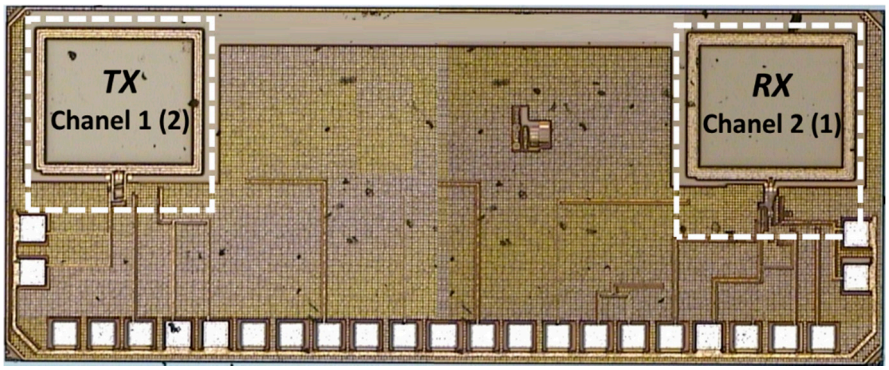

Figure 20. Die photograph of the isolated data transfer system chip.

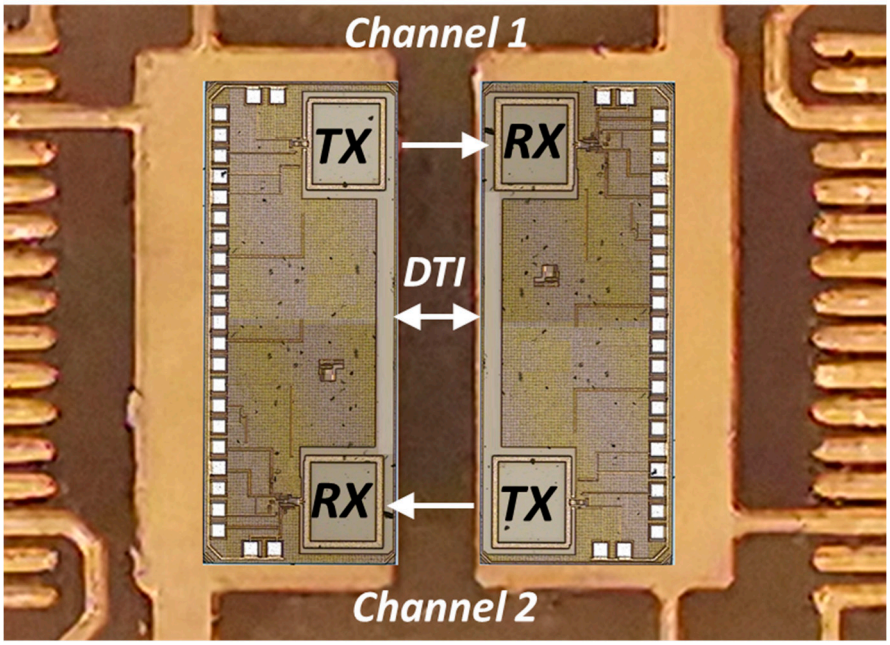

Figure 21. Bidirectional isolated data transfer system assembled on metal frame with 500-µm DTI.

Table 3. Performance summary and comparison with the state-of-the-art of galvanic isolators.

Parameters	[15]	[19]	[24]	[25]	This Work
Supply voltage, V_{DD} [V]	1.7–5.5	3.3	3.5/5[(1)]	1.8	3.3
Isolation voltage, V_{SURGE} [kV]	20	7[(2)]	3.3[(2)]	24	25
Carrier frequency, f_{RF} [GHz]	0.7	n.a.	2.8	1.3/2	1
Modulation	OOK	n.a.	OOK	OOK (edge-triggered)	OOK (PWM)
Max data rate, f_{DMAX} [Mb/s]	1	1	80	500	40
No. of channels	1	4	1	2	2
CMTI [kV/µs]	200	n.a.	n.a.	50	250
Propagation delay, t_p [ns]	11	42	17.6	n.a.	16–20
Energy per bit, E_{BIT} [nJ/bit]	4.8[(3)]	5.5	4.2	0.15/0.2[(4)]	0.5
I_{DD} per channel, I_{DD_CH} [mA]	2.8[(3)]	1.65	96	0.4/0.6[(4)]	6.5
Isolation coupling	Polyimide transformer	Face-to-face stacked antennas	Lateral	Coplanar antennas	Coplanar antennas
Silicon technology	0.18-µm CMOS	0.25-µm SOI BiCDMOS	0.25-µm BCD	0.18-µm CMOS	0.35-µm CMOS
Si area per channel, A_{CH} [mm^2]	n.a.	n.a.	0.94	7[(5)]	3.8/0.9[(6)]
Assembling/Package	Standard	Stacked chips with DAF[(7)]	Standard	Standard	Standard
FoM_1 [(8)]	130	–	–	n.a.	2404
FoM_2 [(9)]	286	–	–	6000	11682
FoM_3 [(10)]	26	–	–	–	730

[(1)] Low/high side; [(2)] rms; [(3)] V_{DD} = 5 V; [(4)] 1.3/2 GHz; [(5)] From micrographs in [25,26]; [(6)] Total area/active area; [(7)] Die attach film (DAF);[(8)] $FoM_1 = (V_{SURGE} \cdot CMTI \cdot f_{DMAX})/(t_p \cdot I_{DD\_CH})$; [(9)] $FoM_2 = (V_{SURGE} \cdot CMTI)/E_{BIT}$; [(10)] $FoM_3 = (V_{SURGE} \cdot CMTI)/(t_p \cdot E_{BIT})$.

The best comparison is with the die-to-die isolated link reported in [25], which exploits an isolation approach based on planar coupling between side-by-side co-packaged chips, thus achieving almost the same isolation rating of our system. Among the papers in Table 3, it also reports the highest f_D and the lowest E_{BIT}, but such a performance is mainly enabled by the adopted 0.18-µm CMOS technology and consequently higher f_{RF} with respect to our work in 0.35-µm CMOS. On the other hand, a CMTI of only 50 kV/µs is claimed, which is already now inadequate for most current applications, while no propagation delay performance is provided, although it is a fundamental parameter, especially for gate-driver applications. Finally, the silicon area per channel, A_{CH}, is nearly double compared with the proposed work. Indeed, differently from our approach, peripherical TX/RX antennas (i.e., with a very large diameter and low number of turns) are used, including all circuitry inside them.

Table 3 contains three figures of merits (FoMs) to better evaluate and compare the reported works. All adopted FoMs account for the isolation rating, V_{SURGE}, and the CMTI. The first figure of merit, FoM_1, was the already defined in [15] and here it is properly weighted by the data rate, f_{DMAX}. On the other hand, both FoM_2 and FoM_3 exploit the energy per bit, E_{BIT}, in the place of I_{DD_CH} to better weigh both the data rate and power consumption, while they differ from the presence of the propagation delay, t_d. Reported values in Table 3 clearly highlight that the proposed work outperforms the state-of-the-art in terms of all the adopted FoMs.

5. Conclusions

A 0.35-µm CMOS bidirectional data transfer system based on RF planar coupling for reinforced galvanic isolators has been presented. With a standard molding compound, it achieves an isolation rating as high as 25 kV and guarantees 250-kV/µs CMTI at a maximum data rate of 40 Mb/s, thus outperforming traditional silicon-integrated isolators. The proposed package-scale isolation is also a low-cost solution since it can be implemented by using standard CMOS and package technologies, while providing an integration level comparable with state-of-the-art chip-scale solutions. The isolation

rating and CMTI performance enable high-voltage/high-switching frequency applications based on wide-bandgap power semiconductor devices, such as GaN HEMTs and SiC MOSFETs.

Author Contributions: Conceptualization, E.R. and G.P.; Investigation, N.S. and A.P.; Methodology, E.R., N.S. and G.P.; Project administration, G.P.; Supervision, E.R. and G.P.; Writing—original draft, E.R.; Writing—review and editing, E.R., A.P. and G.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: The authors would like to thank Alessandro Castorina of STMicroelectronics, Catania for experimental characterization support.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Devices-Magnetic, D.V.S. *DIN VDE Semiconductor Devices-Magnetic and Capacitive Coupler for Basic and Reinforced Isolation*; VDE Verlag VDE V 0884-11: Berlin, Germany, 1 January 2017.
2. Ragonese, E.; Parisi, A.; Spina, N.; Palmisano, G. Reinforced Galvanic Isolation: Integrated Approaches to Go Beyond. In *Applications in Electronics Pervading Industry, Environment and Society ApplePies 2019 Lecture Notes in Electrical Engineering*; Springer International Publishing: Cham, Switzerland, 2020; Volume 627, pp. 277–283.
3. Palumbo, V.; Ghidini, G.; Carollo, E.; Toia, F. Integrated Transformer. U.S. Patent App. 14733009, 8 June 2015.
4. Mahalingam, P.; Guiling, D.; Lee, S. Manufacturing challenges and method of fabrication of on-chip capacitive digital isolators. In Proceedings of the 2007 International Symposium on Semiconductor Manufacturing, Santa Clara, CA, USA, 15–17 October 2007; pp. 1–4.
5. Krone, A.; Tuttle, T.; Scott, J.; Hein, J.; Dupuis, T.; Sooch, N. A CMOS direct access arrangement using digital capacitive isolation. In Proceedings of the 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, USA, 7 February 2001; pp. 300–301.
6. Moghe, Y.; Terry, A.; Luzon, D. Monolithic 2.5kV RMS, 1.8V–3.3V dual-channel 640Mbps digital isolator in 0.5µm SOS. In Proceedings of the 2012 IEEE International SOI Conference (SOI), NAPA, CA, USA, 1–4 October 2012; pp. 1–2.
7. Kaeriyama, S.; Uchida, S.; Furumiya, M.; Okada, M.; Maeda, T.; Mizuno, M. A 2.5 kV isolation 35 kV/us CMR 250 Mbps digital isolator in standard CMOS with a small transformer driving technique. *IEEE J. Solid-State Circuits* **2012**, *47*, 435–443. [CrossRef]
8. Spina, N.; Fiore, V.; Lombardo, P.; Ragonese, E.; Palmisano, G. Current-reuse transformer coupled oscillators with output power combining for galvanically isolated power transfer systems. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2015**, *62*, 2940–2948. [CrossRef]
9. Lombardo, P.; Fiore, V.; Ragonese, E.; Palmisano, G. A fully-integrated half-duplex data/power transfer system with up to 40Mbps data rate, 23mW output power and on-chip 5kV galvanic isolation. In Proceedings of the 2016 IEEE International Solid-State Circuits Conference (ISSCC): Digest of Technical Papers, San Francisco, CA, USA, 31 January–4 February 2016; pp. 300–301.
10. Greco, N.; Spina, N.; Fiore, V.; Ragonese, E.; Palmisano, G. A galvanically isolated dc-dc converter based on current-reuse hybrid coupled oscillators. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2017**, *64*, 56–60. [CrossRef]
11. Fiore, V.; Ragonese, E.; Palmisano, G. A fully-integrated watt-level power transfer system with on-chip galvanic isolation in silicon technology. *IEEE Trans. Power Electron.* **2017**, *32*, 1984–1995. [CrossRef]
12. Ragonese, E.; Spina, N.; Castorina, A.; Lombardo, P.; Greco, N.; Parisi, A.; Palmisano, G. A fully integrated galvanically isolated DC-DC converter with data communication. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2018**, *65*, 1432–1441. [CrossRef]
13. Javid, M.; Ptacek, K.; Burton, R.; Kitchen, J. CMOS bi-directional ultra-wideband galvanically isolated die-to-die communication utilizing a double-isolated transformer. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 88–91.
14. Texas Instruments. ISO7841x High-Performance, 8000-VPK Reinforced Quad-Channel Digital Isolator. Available online: www.ti.com/lit/gpn/ISO7841 (accessed on 4 June 2020).

15. Yun, R.; Sun, J.; Gaalaas, E.; Chen, B. A transformer-based digital isolator with 20kV$_{PK}$ surge capability and >200kV/μS common mode transient immunity. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.
16. Qin, W.; Yang, X.; Ma, S.; Liu, F.; Zhao, Y.; Zhao, T.; Chen, B. An 800 mW fully integrated galvanic isolated power transfer system meeting CISPR 22 Class-B emission levels with 6dB margin. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference-(ISSCC): Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2019; pp. 246–248.
17. Spina, N.; Girlando, G.; Smerzi, S.A.; Palmisano, G. Integrated Galvanic Isolator Using Wireless Transmission. U.S. Patent 8364195 B2, 29 January 2013.
18. Renna, C.M.A.; Scuderi, A.; Magro, C.; Spina, N.; Ragonese, E.; Marano, B.; Palmisano, G. Microstructure Device Comprising a Face to Face electromagnetic Near Field Coupling between Stacked Device Portions and Method of Forming the Device. U.S. Patent 9018730 B2, 28 April 2015.
19. Uchida, S.; Kaeriyama, S.; Nagase, H.; Takeda, K.; Nakashiba, Y.; Maeda, T.; Ishihara, K. A face-to-face chip stacking 7kV RMS digital isolator for automotive and industrial motor drive applications. In Proceedings of the 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 442–445.
20. Paye, J.; Claudi, V.; Stecher, M. High voltage robustness of mold compounds under different environmental conditions. In Proceedings of the 2015 IEEE International Reliability Physics Symposium, Monterey, CA, USA, 19–23 April 2015; pp. CP.5.1–CP.5.6.
21. Paye, J.; Claudi, V.; Stecher, M. High voltage robustness of mold compounds after different treatments. In Proceedings of the 2016 IEEE Electrical Insulation Conference (EIC), Montreal, QC, USA, 19–22 June 2016; pp. 162–165.
22. Guo, J.; Tan, T. A broadband and scalable on-chip inductor model appropriate for operation modes of varying substrate resistivities. *IEEE Trans. Electron Devices* **2007**, *54*, 3018–3029. [CrossRef]
23. Biondi, T.; Scuderi, A.; Ragonese, E.; Palmisano, G. Characterization and modeling of silicon integrated spiral inductors for high-frequency applications. *Analog Integr. Circuits Signal Process.* **2007**, *51*, 89–100. [CrossRef]
24. Javid, M.; Burton, R.; Ptacek, K.; Kitchen, J. CMOS integrated galvanically isolated RF chip-to-chip communication utilizing lateral resonant coupling. In Proceedings of the 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest, Honolulu, HI, USA, 4–6 June 2017; pp. 252–255.
25. Mukherjee, S.; Bhat, A.N.; Shrivastava, K.A.; Bonu, M.; Sutton, B.; Gopinathan, V.; Thiagarajan, G.; Patki, A.; Malakar, J.; Krishnapura, N. A 500Mb/s 200pJ/b die-to-die bidirectional link with 24kV surge isolation and 50kV/μs CMR using resonant inductive coupling in 0.18μm CMOS. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC): Digest of Technical Papers, San Francisco, CA, USA, 5–9 February 2017; pp. 434–435.
26. Krishnapura, N.; Bhat, A.N.; Mukherjee, S.; Shrivastava, K.A.; Bonu, M. Maximizing the data rate of an inductively coupled chip-to-chip link by resetting the channel state variables. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3531–3543. [CrossRef]