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# Full Range Capacitor Voltage Balance PWM Strategy for Diode-Clamped Multilevel Inverter

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**Abstract:** This paper briefly reviews virtual space vector pulse width modulation (VSVPWM) for the diode-clamped multilevel inverter (DCMLI). Based on the universal modulation model of the DCMLI with N-level, a modulation strategy named as full range capacitor voltage balance PWM (FRCVBPWM) is proposed, which has similar capacitor voltage balance characteristics as VSVPWM. The characteristic of FRCVBPWM is that there are respectively zero, N − 1 and N − 2 switching actions for the three phases of the DCMLI. Therefore, the total switching actions are greatly decreased compared with VSVPWM. The switching loss comparison between FRCVBPWM and VSVPWM is conducted by comprehensive simulations. Finally, the feasibility and superiority of FRCVBPWM over VSVPWM is verified by experiments.

**Keywords:** diode-clamped multilevel inverter (DCMLI); modulation strategy; full range capacitor voltage balance; switching loss

## 1. Introduction

Recently, power electronic technology has rapidly developed in large capacity and low loss applications. The diode clamped multilevel inverter (DCMLI) was proposed [1,2], due to the advantages of lower output voltage distortion, lower electromagnetic interference and lower voltage stress [3]. This topology has received much attention and is widely used in the fields of new energy power generation, motor drives, and power quality and compensation [4,5]. Among DCMLIs, the diode clamped three-level inverter, also known as a neutral point clamped three-level inverter (NPC TLI), has been widely applied.

Capacitor voltage balance is a key issue for the DCMLI's safe and stable operation. For an NPC TLI, some PWM strategies have been suggested for capacitor voltage control, where the carrier-based PWM (CBPWM) and space vector PWM (SVPWM) [6–9] are the two important types. It is revealed in literatures [10,11] that the relationship between a CBPWM and an SVPWM is essentially equivalent, since SVPWM can be achieved by injecting a specific zero-sequence voltage into the modulation wave of the CBPWM. However, the disadvantage of all the above methods is the low frequency oscillation on the capacitor voltage under high modulation index (MI) and low power factor (PF) operating conditions.

When the level number of the DCMLI is more than three, there are few PWM strategies for capacitor voltage control. Based on the predictive current control, an approach for a five-level DCMLI is presented [12,13], which can control both the output current and capacitor voltage. In [14,15], the passive front-end capacitor voltage balance control for a DCMLI is proposed. In [16,17], the SVPWM modulation strategy for a DCMLI is studied, but there is a problem of capacitor voltage fluctuation. For a five-level DCMLI, improved PWM strategies or an additional capacitor voltage control circuit can

be adopted to control the capacitor voltage balance [18,19]. However, the increased complexity and cost of the system are the main drawbacks when applying an additional capacitor voltage control circuit.

To achieve capacitor voltage balance over the full range of the PF and the MI, a virtual SVPWM (VSVPWM) strategy is proposed [20]. This modulation strategy exhibits excellent characteristics in capacitor voltage balance control. An improved VSVPWM was presented in [21,22] to meet the other requirements of the system, such as low switching loss and reduced common-mode voltage. In addition, VSVPWM can be extended from three-phase three-level to N-level [23]; the total number of switching actions is 3N − 5. Compared to CBPWM and SVPWM, VSVPWM has the disadvantage of large switching losses, especially when the PF is low.

A PWM strategy for a DCMLI that achieves the same goals as VSVPWM, but overcomes the shortcoming of VSVPWM, is presented in this paper. Under this strategy, the full range capacitor voltage balance control can be realized. It is called a full range capacitor voltage balance PWM (FRCVBPWM), which is characterized by one phase without switching action, one phase with N − 1 switching actions, and one phase with N − 2 switching actions. In total, there are 2N − 3 switching actions for the three phases, which significantly reduce the switching losses compared to VSVPWM.

## 2. DCMLI and its Modulation Model

### 2.1. DCMLI

The topology of an N-level DCMLI is shown in Figure 1. There are 2N – switching devices with an anti-parallel diode and 2N – 4 clamping diodes in each phase. The capacitors $C_1$ to $C_{N-1}$ divide the DC side voltage equally when the capacitor voltage maintains balance, i.e., $U_{c1} = ... = U_{cn-1} = 2u_{dc}/(N - 1)$. Level N − 1 is defined as when switches $S_1 - S_{N-1}$ are turned on and the DCMLI's output voltage is $u_{dc}$; Level N − 2 is defined as when switches $S_2 - S_N$ are turned on and the output voltage is $u_{dc}\times$ (N − 3)/(N − 1), etc. Level 0 is defined as when switches $S_N - S_{2N-2}$ are turned on and the output voltage is $-u_{dc}$. Hereafter, $u_{dc} = 1$ is assumed for simplicity and the positive current direction is considered as flowing from the inverter to the load. The normalized three-phase output voltages $u_a$, $u_b$ and $u_c$ can be expressed as:

$$\begin{cases} u_a = m\cos\omega t \\ u_b = m\cos(\omega t - 2\pi/3) \\ u_c = m\cos(\omega t - 4\pi/3) \end{cases} \quad (1)$$

where, $m \in [0, 1.1547]$ stands for the MI and $\omega t$ stands for the phase angle of phase A. The three-phase currents $i_a$, $i_b$ and $i_c$ can be expressed as:

$$\begin{cases} i_a = I_m\cos(\omega t - \varphi) \\ i_b = I_m\cos(\omega t - 2\pi/3 - \varphi) \\ i_c = I_m\cos(\omega t - 4\pi/3 - \varphi) \end{cases} \quad (2)$$

where, $I_m$ stands for the peak value of the phase current and $\varphi \in [0, 2\pi]$ stands for the PF angle of the load.

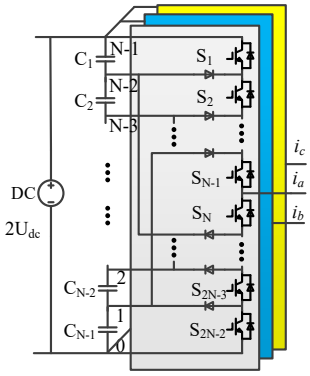



**Figure 1.** The topology of the diode-clamped multilevel inverter (DCMLI).

### *2.2. The PWM Model for DCMLI*

The three-phase voltages given by (1) can be rearranged as:

$$\begin{cases} u_{\max} &= \max(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}) \\ u_{\mathrm{mid}} &= \mathrm{mid}(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}) \\ u_{\min} &= \min(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}) \end{cases} \tag{3}$$

where, the maximum, middle and minimum phase voltages are denoted as $u_{\max}$, $u_{\mathrm{mid}}$ and $u_{\min}$, respectively. The phase currents corresponding to $u_{\max}$, $u_{\mathrm{mid}}$ and $u_{\min}$ are denoted as $i_{\max}$, $i_{\mathrm{mid}}$ and $i_{\min}$, respectively. The general modulation model of the DCMLI, based on volt-second equilibrium is give as follows:

$$\mathbf{Gd} \;=\; \mathbf{H}, \tag{4}$$

where,

$$\mathbf{G} \;=\; \begin{bmatrix} (N-1) & \cdots & 0 & -(N-1) & \cdots & 0 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & (N-1) & \cdots & 0 & -(N-1) & \cdots & 0 \\ 1 & \cdots & 1 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 1 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 0 & \cdots & 0 & 1 & \cdots & 1 \end{bmatrix}_{5\times 3N} \tag{5}$$

$\mathbf{d} \;=\; [d_{\mathrm{max,N-1}}, \cdots, d_{\mathrm{max,0}}, d_{\mathrm{mid,N-1}}, d_{\mathrm{mid,0}}, d_{\mathrm{min,N-1}}, \cdots, d_{\mathrm{min,0}}]^T$, and $\mathbf{H} \;=\; [u_{\max} - u_{\mathrm{mid}}, u_{\mathrm{mid}} - u_{\min}, 1, 1, 1]^T$. The term $d_{kn}$ is the duty ratio of level $n$ of phase $k$ ($k$ = max, min, mid and $n = 0, 1, \ldots, \mathrm{N}-1$). From (4), it can be seen that the relationship between the outputted line-to-line voltages and the duty ratios is revealed by the first two equations and the sum of all duty ratios of each phase must be equal to one, which is revealed by the latter three equations. The restrictive condition of $d_{kn}$ can be expressed as:

$$0 \le d_{kn} \le 1. \tag{6}$$

A specific modulation strategy can be determined by solving for the unknowns $d_{kn}$ given by (4). According to (4), the number of unknowns $d_{kn}$ is 3N but there are only five equations, therefore the specific solution of $d_{kn}$ cannot be obtained. For the purpose of the specific solution of $d_{kn}$, additional restrictive conditions are required. In one switching cycle, the three-phase currents are assumed to be constant. To maintain each capacitor voltage balance in one switching cycle, the sum of the currents injected into each capacitor should be zero. The mathematical expression is written as:

$$i_{\max} d_{\mathrm{max,n}} + i_{\mathrm{mid}} d_{\mathrm{mid,n}} + i_{\min} d_{\mathrm{min,n}} \;=\; 0 \;(n \;=\; 1, \cdots, \mathrm{N}-2), \tag{7}$$

Combining (4) with (6), the capacitor voltage balance model for the DCMLI can be further obtained. Although there are N − 2 equations based on (6), the specific solution of all duty ratios cannot be obtained, and the additional restrictive conditions are still required.

### *2.3. Review of VSVPWM for DCMLI*

Since $i_a + i_b + i_c = 0$ is always satisfied with the star-connected load, the simplest solution for (6) is:

$$d_{\mathrm{max,n}} = d_{\mathrm{mid,n}} = d_{\mathrm{min,n}} \, (n = 1, \cdots, \mathrm{N}-2), \tag{8}$$

assuming that:

$$d_{\mathrm{k},1} = \cdots = d_{\mathrm{k},N-2} \, (k = \mathrm{max},\ \mathrm{min},\ \mathrm{mid}). \tag{9}$$

The characteristics of VSVPWM can be described as follows. The phase corresponding to $u_{\max}$ has the switching sequence composed of levels 1, … , N − 1; the phase corresponding to $u_{\min}$ has the switching sequence composed of levels 0, … , N − 2; and the phase corresponding to $u_{\mathrm{mid}}$ has the switching sequence composed of levels 0, … , N − 1. According to the above characteristics, (9) can be obtained:

$$d_{\max,0} = d_{\min,N-1} = 0. \tag{10}$$

A complete calculation model of VSVPWM for a DCMLI can be acquired by combining (4), (8), (9) and (10), and the specific solution of all duty ratios is obtained as following:

$$\begin{cases} d_{\max,0} = 0 \\ d_{\max,1} = \cdots = d_{\max,N-2} = \frac{(N-1)-u_{\max}+u_{\min}}{(N-2)(N-1)} \\ d_{\max,N-1} = \frac{u_{\max}-u_{\min}}{(N-1)} \end{cases}$$
$$\begin{cases} d_{\mathrm{mid},0} = \frac{u_{\max}-u_{\mathrm{mid}}}{(N-1)} \\ d_{\mathrm{mid},1} = \cdots = d_{\mathrm{mid},N-2} = \frac{(N-1)-u_{\max}+u_{\min}}{(N-2)(N-1)} \\ d_{\mathrm{mid},N-1} = \frac{u_{\mathrm{mid}}-u_{\min}}{(N-1)} \end{cases} \tag{11}$$
$$\begin{cases} d_{\min,0} = \frac{u_{\max}-u_{\min}}{(N-1)} \\ d_{\min,1} = \cdots = d_{\min,N-2} = \frac{(N-1)-u_{\max}+u_{\min}}{(N-2)(N-1)} \\ d_{\min,N-1} = 0 \end{cases}$$

The following conclusion can be obtained from (11). (i) All duty ratios are independent of the phase currents. (ii) When $m \in [0, 1.1547]$, (5) is satisfied for all duty ratios. (iii) The condition for maintaining the voltage balance of each capacitor in one switching cycle given by (6) is satisfied. Although VSVPWM exhibits excellent capacitor voltage balance performance over the full range of PFs and MIs, the total of 3N − 5 switching actions results in large switching losses, which is a major drawback.

## 3. The Proposed FRCVBPWM for DCMLI

### *3.1. The Proposed FRCVBPWM*

In this paper, FRCVBPWM is proposed to solve the problem of the large switching losses of VSVPWM. Assume that one phase has no switching action, one phase has N − 1 switching actions, and one phase has N − 2 switching actions; then there are only 2N – 3 switching actions for the three phases in one switching cycle. This is the basic idea for FRCVBPWM proposed in this paper. There are four cases, as listed in Table 1.

**Table 1.** The switching number under different modes of full range capacitor voltage balance PWM (FRCVBPWM).

| | **MAX_PB/MID_N − 1/MIN_N − 2** | **MAX_PB/MIN_N − 1/MID_N − 2** | **MIN_NB/MAX_N − 1/MID_N − 2** | **MIN_NB/MID_N − 1/MAX_N − 2** |
|---|---|---|---|---|
| $u_{\max}$ | 0 | 0 | N − 1 | N − 2 |
| $u_{\mathrm{mid}}$ | N − 1 | N − 2 | N − 2 | N − 1 |
| $u_{\min}$ | N − 2 | N − 1 | 0 | 0 |

### *3.2. The Duty Ratio Calculation under Different Modes in One Switching Cycle*

(a). Mode 1: MAX_PB/MID_N − 1/MIN_N − 2

In this mode, the phase corresponding to $u_{\max}$ is clamped to level N − 1 (i.e., positive bus) without a switching action. Therefore, the duty ratios with respect to $u_{\max}$ are written as

$$d_{\max,N-1} = 1,\ d_{\max,N-2}\cdots = d_{\max,0} = 0. \tag{12}$$

For $u_{\mathrm{mid}}$, the switching sequence is composed of levels 0,..., N − 1 and there are N − 1 switching actions; for $u_{\min}$, the switching sequence is composed of levels 0,..., N − *2* and there are N − 2 switching actions. Since there is no level N − 1 in the switching sequence for $u_{\min}$, $d_{\mathrm{min,N-1}}$ is determined as:

$$d_{\mathrm{min},N-1} = 0. \tag{13}$$

Thus, (7) is rewritten as:

$$i_{\mathrm{mid}}d_{\mathrm{mid,n}} + i_{\min}d_{\mathrm{min,n}} = 0 \quad (\mathrm{n} = 1,2,\cdots,N-2), \tag{14}$$

Letting $d_{\mathrm{mid,n}} = d_{\mathrm{mid},1}$, $d_{\mathrm{min,n}} = d_{\mathrm{min},1}$ $(n = 2,\cdots,N-2)$ and $-i_{\mathrm{mid}}/i_{\min} = K$, so:

$$Kd_{\mathrm{mid},1} = \cdots = Kd_{\mathrm{mid},N-2} = d_{\mathrm{min},1} = \cdots = d_{\mathrm{min},N-2}. \tag{15}$$

Therefore, the calculation model of FRCVBPWM for the DCMLI can be acquired by combining (4), (12)–(15), and the specific solution of all duty ratios is listed in Table 2.

(b). Mode 2: MAX_PB/MIN_N − 1/MID_N − 2

In this mode, the phase corresponding to $u_{\max}$ is clamped to level N − 1 without a switching action. For $u_{\min}$, the switching sequence is composed of levels 0,..., N − 1 and there are N − 1 switching actions. For $u_{\mathrm{mid}}$, there are N − 2 switching actions. There are two cases for the switching sequence of $u_{\mathrm{mid}}$:

Mode 2-1: the switching sequence of $u_{\mathrm{mid}}$ is composed of levels 1..., N − 1.

Mode 2-2: the switching sequence of $u_{\mathrm{mid}}$ is composed of levels 0..., N − 2.

(c). Mode 3: MIN_NB/MAX_N − 1/MID_N − 2

In this mode, the phase corresponding to $u_{\min}$ is clamped to level 0 (i.e., negative bus) without a switching action. For $u_{\max}$, the switching sequence is composed of levels 0,..., N − 1 and there are N − 1 switching actions. For $u_{\mathrm{mid}}$, there are N − 2 switching actions. It also has two cases for the switching sequence of $u_{\mathrm{mid}}$:

Mode 3-1: the switching sequence of $u_{\mathrm{mid}}$ is composed of levels 1..., N − 1.

Mode 3-2: the switching sequence of $u_{\mathrm{mid}}$ is composed of levels 0 ..., N − 2.

(d). Mode 4: MIN_NB/MID_N − 1/MAX_N − 2

In this mode, the phase corresponding to $u_{\min}$ is clamped to level 0 without a switching action. For $u_{\mathrm{mid}}$, the switching sequence is composed of levels 0,..., N − 1 and there are N − 1 switching actions. For $u_{\max}$, the switching sequence is composed of levels 1,..., N − 1 and there are N − 2 switching actions.

**Table 2.** All duty ratios under different modes of FRCVBPWM.

| Mode | Duty Ratio | Mode | Duty Ratio |
|---|---|---|---|
| Mode 1: MAX_PB/MID_N − 1/MIN_N − 2 | $d_{\min,0} = 1-2\frac{(N-1)-u_{L1}}{(N-1)}$<br>$d_{\min,N-2} = \ldots = d_{\min,1} = 2\frac{(N-1)-u_{L1}}{(N-2)(N-1)}$<br>$d_{\min,N-1} = 0$<br>$d_{\mathrm{mid},0} = \frac{u_{L2}}{N-1} + \frac{u_{L1}-(N-1)}{K(N-1)}$<br>$d_{\mathrm{mid},N-2} = \ldots = d_{\mathrm{mid},1} = \frac{2}{K}\frac{(N-1)-u_{L1}}{(N-2)(N-1)}$<br>$d_{\mathrm{mid},N-1} = 1-\frac{u_{L2}}{N-1} - \frac{(N-1)-u_{L1}}{K(N-1)}$<br>$d_{\max,N-1} = 1, d_{\max,N-2} = \ldots = d_{\max,1} = 0, d_{\max,0} = 0$<br>$K = -i_{\mathrm{mid}}/i_{\min}$ | Mode 2-1:<br>MAX_PB/MIN_N − 1/MID_N − 2<br>(The output sequence of the phase corresponding to $u_{\mathrm{mid}}$ is composed of levels 1... , $N-1$) | $d_{\min,0} = \frac{u_{L1}-Ku_{L2}}{(N-1)}$<br>$d_{\min,N-2} = \cdots = d_{\min,1} = \frac{2Ku_{L2}}{(N-1)(N-2)}$<br>$d_{\min,N-1} = 1-\frac{u_{L1}+Ku_{L2}}{(N-1)}$<br>$d_{\mathrm{mid},0} = 0$<br>$d_{\mathrm{mid},N-2} = \cdots = d_{\mathrm{mid},1} = \frac{2u_{L2}}{(N-1)(N-2)}$<br>$d_{\mathrm{mid},N-1} = 1-\frac{2u_{L2}}{(N-1)}$<br>$d_{\max,N-1} = 1, d_{\max,N-2} = \cdots = d_{\max,1} = 0, d_{\max,0} = 0$<br>$K = -i_{\mathrm{mid}}/i_{\min}$ |
| Mode 2-2:<br>MAX_PB/MIN_N − 1/MID_N − 2<br>(The output sequence of the phase corresponding to $u_{\mathrm{mid}}$ is composed of levels 0..., $N-2$) | $d_{\min,0} = \frac{u_{L1}+Ku_{L2}}{N-1} - K$<br>$d_{\min,N-2} = \cdots = d_{\min,1} = \frac{2K[(N-1)-u_{L2}]}{(N-2)(N-1)}$<br>$d_{\min,N-1} = \frac{u_{L1}}{1-N} + \frac{Ku_{L2}}{N-1} + 1 - K$<br>$d_{\mathrm{mid},0} = -1 + 2\frac{u_{L2}}{(N-1)}$<br>$d_{\mathrm{mid},N-2} = \cdots = d_{\mathrm{mid},1} = \frac{2[(N-1)-u_{L2}]}{(N-2)(N-1)}$<br>$d_{\mathrm{mid},N-1} = 0$<br>$d_{\max,N-1} = 1, d_{\max,N-2} = \ldots = d_{\max,1} = 0, d_{\max,0} = 0$<br>$K = -i_{\mathrm{mid}}/i_{\min}$ | Mode 3-1:<br>MIN_NB/MAX_N − 1/MID_N − 2<br>(The output sequence of the phase corresponding to $u_{\mathrm{mid}}$ is composed of levels 1..., $N-1$) | $d_{\min,0} = 1, d_{\min,N-2} = \cdots = d_{\min,1} = 0, d_{\min,N-1} = 0$<br>$d_{\mathrm{mid},0} = 0$<br>$d_{\mathrm{mid},N-2} = \cdots = d_{\mathrm{mid},1} = 2\frac{(N-1)-u_{L3}}{(N-1)(N-2)}$<br>$d_{\mathrm{mid},N-1} = \frac{2u_{L3}}{(N-1)} - 1$<br>$d_{\max,0} = 1-\frac{u_{L1}}{N-1} + \frac{Ku_{L3}}{(N-1)} - K$<br>$d_{\max,N-2} = \cdots = d_{\max,1} = 2K\frac{(N-1)-u_{L3}}{(N-1)(N-2)}$<br>$d_{\max,N-1} = -K\frac{(N-1)-u_{L3}}{(N-1)} + \frac{u_{L1}}{N-1}$<br>$K = -i_{\mathrm{mid}}/i_{\max}$ |
| Mode 3-2:<br>MIN_NB/MAX_N − 1/MID_N − 2<br>(The output sequence of the phase corresponding to $u_{\mathrm{mid}}$ is composed of levels 0..., $N-2$) | $d_{\min,0} = 1, d_{\min,N-2} = \cdots = d_{\min,1} = 0, d_{\min,N-1} = 0$<br>*vspace3pt* $d_{\mathrm{mid},0} = 1-\frac{2u_{L3}}{(N-1)}$<br>$d_{\mathrm{mid},N-2} = \cdots = d_{\mathrm{mid},1} = \frac{2u_{L3}}{(N-1)(N-2)}$<br>$d_{\mathrm{mid},N-1} = 0$<br>$d_{\max,0} = 1-\frac{u_{L1}+Ku_{L3}}{(N-1)}$<br>$d_{\max,N-2} = \cdots = d_{\max,1} = \frac{2Ku_{L3}}{(N-1)(N-2)}$<br>$d_{\max,N-1} = \frac{u_{L1}-Ku_{L3}}{(N-1)}$<br>$K = -i_{\mathrm{mid}}/i_{\max}$ | Mode 4:<br>MIN_NB/MID_N − 1/MAX_N − 2 | $d_{\min,0} = 1, d_{\min,N-2} = \cdots = d_{\min,1} = 0, d_{\min,N-1} = 0$<br>$d_{\mathrm{mid},0} = 1-\frac{1}{K}\left[1-\frac{u_{L1}}{(N-1)}\right] - \frac{u_{L2}}{N-1}$<br>$d_{\mathrm{mid},N-2} = \cdots = d_{\mathrm{mid},1} = \frac{1}{K}\left[\frac{2}{(N-2)} - \frac{2u_{L1}}{(N-1)(N-2)}\right]$<br>$d_{\mathrm{mid},N-1} = \frac{u_{L2}}{N-1} - \frac{1}{K}\left[1-\frac{u_{L1}}{(N-1)}\right]$<br>$d_{\max,0} = 0$<br>$d_{\max,N-2} = \cdots = d_{\max,1} = \frac{2}{(N-2)} - \frac{2u_{L1}}{(N-1)(N-2)}$<br>$d_{\max,N-1} = \frac{2u_{L1}}{(N-1)} - 1$<br>$K = -i_{\mathrm{mid}}/i_{\max}$ |

Remark: $u_{\max} - u_{\min} = u_{L1}, u_{\max} - u_{\mathrm{mid}} = u_{L2}, u_{\mathrm{mid}} - u_{\min} = u_{L3}$.

The switching sequences of the three phases under different modes are presented in Figure 2. The calculation models of all duty ratios for FRCVBPWM under different modes are presented in Table 2. It can be noted that the duty ratios under different modes are determined by the three-phase voltages and currents. The mode is available if the calculated duty ratios under this mode satisfy (6). The application area of one mode means that the mode is available within the area. The application areas under several certain $\varphi$ under different modes are shown in Figures 3–6, where the white areas stand for the application areas.

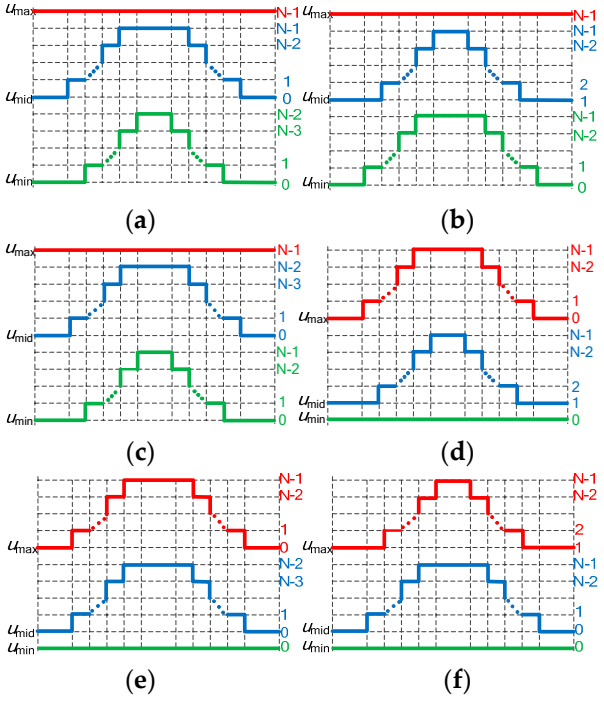



**Figure 2.** The PWM sequences for the FRCVBPWM under different modes: (**a**) Mode 1, (**b**) Mode 2-1, (**c**) Mode 2-2, (**d**) Mode 3-1, (**e**) Mode 3-2, and (**f**) Mode 4.

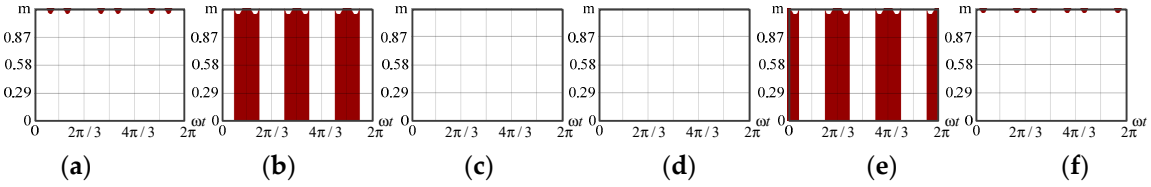



**Figure 3.** The application area for different modes while $\varphi = 0$: (**a**) Mode 1, (**b**) Mode 2-1, (**c**) Mode 2-2, (**d**) Mode 3-1, (**e**) Mode 3-2, and (**f**) Mode 4.

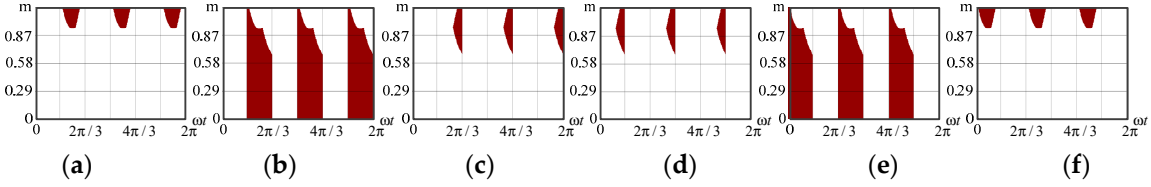



**Figure 4.** The application areas for different modes while $\varphi = \pi/6$: (**a**) Mode 1, (**b**) Mode 2-1, (**c**) Mode 2-2, (**d**) Mode 3-1, (**e**) Mode 3-2, and (**f**) Mode 4.

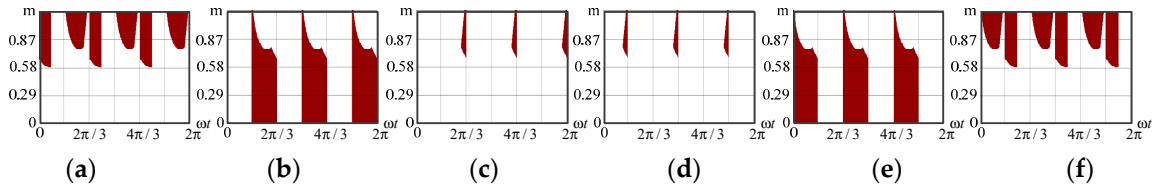



**Figure 5.** The application areas for different modes while $\varphi = \pi/3$: (**a**) Mode 1, (**b**) Mode 2-1, (**c**) Mode 2-2, (**d**) Mode 3-1, (**e**) Mode 3-2, and (**f**) Mode 4.

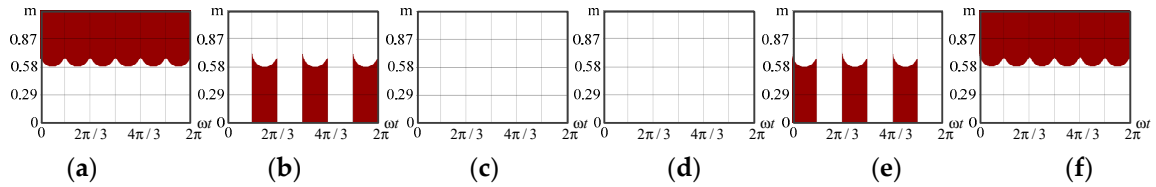



**Figure 6.** The application areas for different modes while $\varphi = \pi/2$: (**a**) Mode 1, (**b**) Mode 2-1, (**c**) Mode 2-2, (**d**) Mode 3-1, (**e**) Mode 3-2, and (**f**) Mode 4.

## 4. Selecting the Mode Based on the Switching Loss

It can be seen from Figures 3–6 that there is at least one available mode in any condition of $m$ and $\omega t$, and there are even three available modes in some conditions of $m$ and $\omega t$, so an optimal available mode can be chosen. In this paper, the minimum switching loss is used as the selection criterion. The switching loss evaluation function for different modes can be expressed as:

$$P_{SL} = \sum_{k = \max,\min,mid} |i_k| \times f_k, \tag{16}$$

where $f_k$ represents the switching action number of phase $k$.

Based on (16), the selected modes with several certain values of $\varphi$ under the whole range of $m$ and $\omega t$ are shown in Figure 7. While $\varphi = 0$, it is necessary to switch between modes 1, 2-2, 3-1 and 4 when $m$ is greater than 1 and it is only necessary to switch between modes 2-2 and 3-1 when $m$ is less than 1. While $\varphi = \pi/2$, it is necessary to switch between modes 2-2 and 3-1 when $m$ is about less than 0.577 and it is necessary to switch between modes 1 and 4 when $m$ is about greater than 0.577.

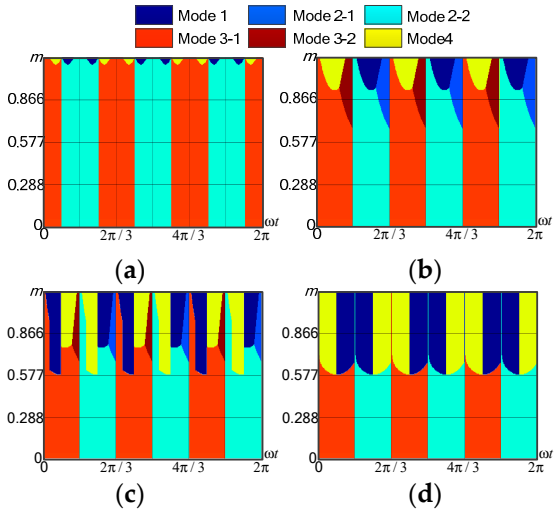



**Figure 7.** The selected modes based on minimum switching loss under several certain values of $\varphi$: (**a**) $\varphi = 0$, (**b**) $\varphi = \pi/6$, (**c**) $\varphi = \pi/3$, and (**d**) $\varphi = \pi/2$.

## 5. The Implementation of FRCVBPWM

A carrier-based PWM method generates the PWM sequences by comparing the carrier with the modulation wave. This method is used for the implementation of FRCVBPWM because it can be easily carried out. For a multilevel inverter, multiple modulation waves are required, which can be obtained based on geometric relationships:

$$\begin{cases} u_{k,N-1} &= d_{k,N-1}u_{dc} \\ u_{k,N-2} &= (d_{k,N-1}+d_{k,N-2})u_{dc} \\ u_{k,N-3} &= (d_{k,N-1}+d_{k,N-2}+d_{k,N-3})u_{dc} \\ \vdots & \\ u_{k,1} &= (d_{k,N-1}+\cdots+d_{k,1})u_{dc} \end{cases}. \tag{17}$$

Multiple PWM sequences can be acquired by comparing a single carrier with multiple modulation waves; then, the final PWM sequence of the FRCVBPWM can be realized by adding the acquired multiple PWM sequences, as shown in Figure 8. The switching action number of FRCVBPWM and VSVPWM under different levels is shown in Table 3.

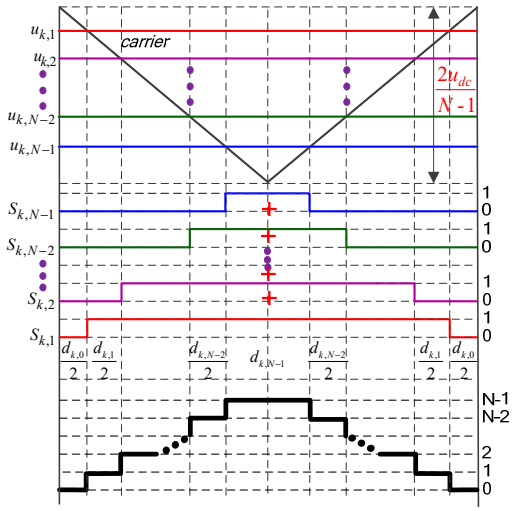



**Figure 8.** Realization of FRCVBPWM based on the carrier-based PWM.

**Table 3.** The switching action number of FRCVBPWM and VSVPWM.

| | Three-Level | Five-Level | ...-Level | *N*-Level |
|---|---|---|---|---|
| FRCVBPWM | 3 | 7 | ... | 2N − 3 |
| VSVPWM | 4 | 10 | ... | 3N − 5 |

## 6. Switching Loss Analysis

For different modulation strategies, the conduction losses are generally considered to be equal and are not taken into account. Therefore, the loss analysis mainly focuses on switching losses. The average switching losses in a fundamental period can be calculated using the method proposed in [24], which is adopted here. When the phase current peaks are the same, the average switching losses of FRCVBPWM and VSVPWM with the variation of $\varphi$ and $m$ can be calculated, which are recorded as $P_{\mathrm{SL\_FCVB}}$ and $P_{\mathrm{SL\_VSV}}$, respectively.

Figure 9 shows the ratios of $P_{\mathrm{SL\_FCVB}}$ to $P_{\mathrm{SL\_VSV}}$ for a DCMLI with different levels. It can be seen that in the operating range of the higher $m$ and lower PF, the switching losses of FRCVBPWM are significantly lower than that of VSVPWM. In addition, the ratios of $P_{\mathrm{SL\_FCVB}}$ to $P_{\mathrm{SL\_VSV}}$ are reduced more obviously with the increase of levels.

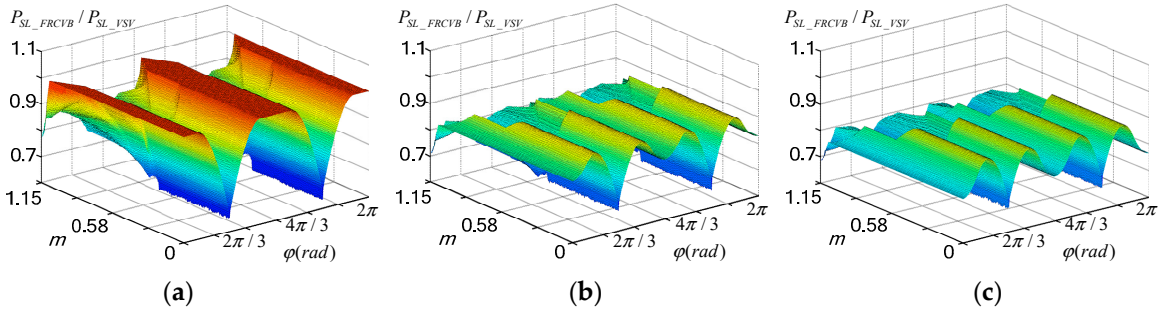



**Figure 9.** The duty ratios of $P_{SL\_FRCVB}$ to $P_{SL\_VSV}$ under different levels: (**a**) three-level, (**b**) four-level, and (**c**) five-level.

## 7. Experimental Verification

A three-level DCMLI is built to verify the proposed FRCVBPWM. The DSP used as the main controller chip is Freescale's MC56F84789, and the IGBT model used as the switching device is F3L300R07PE4. The experimental parameters are listed in Table 4.

**Table 4.** Experimental parameters.

| Parameter | Value |
|---|---|
| DC side voltage | 200 V |
| Upper and lower capacitance values | 1000 μF |
| Load factor with high PF 1 ($Z_{H1}$) | $2e^{j\pi/12}$ Ω |
| Load factor with high PF 2 ($Z_{H2}$) | $6e^{j\pi/12}$ Ω |
| Load factor with low PF 1 ($Z_{L1}$) | $2e^{j5\pi/12}$ Ω |
| Load factor with low PF 2 ($Z_{L2}$) | $6e^{j5\pi/12}$ Ω |
| Fundamental frequency | 50 Hz |

The steady-state experimental results under four conditions with different $m$ and $\varphi$ for FRCVBPWM and VSVPWM are shown in Figures 10 and 11, respectively. The capacitor voltage can be controlled effectively under the two modulation strategies.

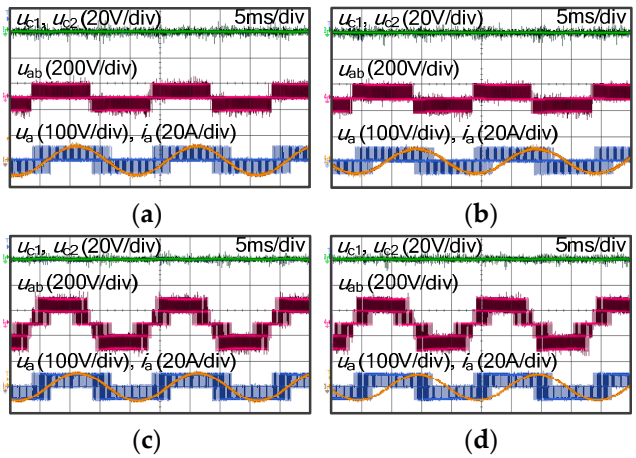



**Figure 10.** Steady state experimental results of virtual space vector pulse width modulation (VSVPWM): (**a**) $m = 0.3$, $\varphi = \pi/12$, (**b**) $m = 0.3$, $\varphi = 5\pi/12$ (**c**) $m = 0.9$, $\varphi = \pi/12$ and (**d**) $m = 0.9$, $\varphi = 5\pi/12$.

From the waveform of phase voltage $u_a$ shown in Figure 10, it can be seen that there is about one-third of an interval of a fundamental cycle in which it outputs levels 0, 1 and 2. It indicates that there are two switching actions during this interval, and there is one switching action during the other

interval. From the waveform of phase voltage $u_a$ shown in Figure 11, it can be noted that there is a clamping interval in which the phase voltage $u_a$ is clamped to the positive or negative bus. Moreover, the interval with two switching actions is roughly equal to the clamping interval. Thus, each phase has one switching action on average, which reduces the switching losses of FRCVBPWM.

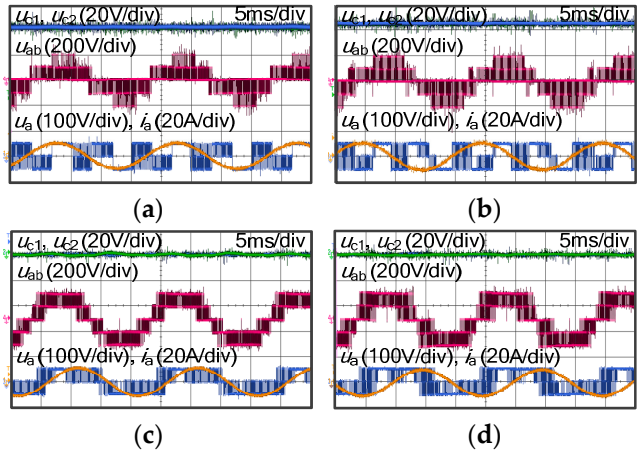



**Figure 11.** Steady state experimental results of FRCVBPWM: (**a**) $m = 0.3$, $\varphi = \pi/12$, (**b**) $m = 0.3$, $\varphi = 5\pi/12$, (**c**) $m = 0.9$, $\varphi = \pi/12$, and (**d**) $m = 0.9$, $\varphi = 5\pi/12$.

For FRCVBPWM and VSVPWM, the switching loss comparisons under four conditions are shown in Figure 12. When PF is higher, the switching loss difference between FRCVBPWM and VSVPWM is very small. When PF is lower, the switching losses of VSVPWM are significantly greater than that of FRCVBPWM.

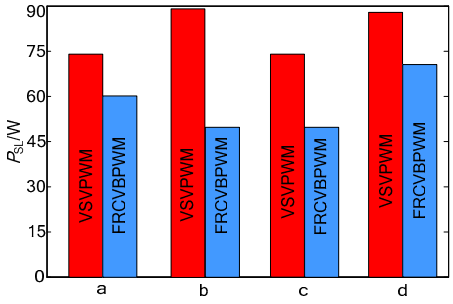
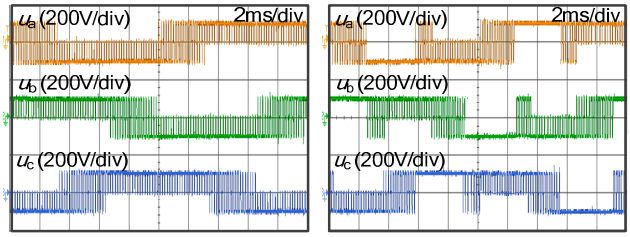



**Figure 12.** The measured switching losses corresponding to Figures 10 and 11.

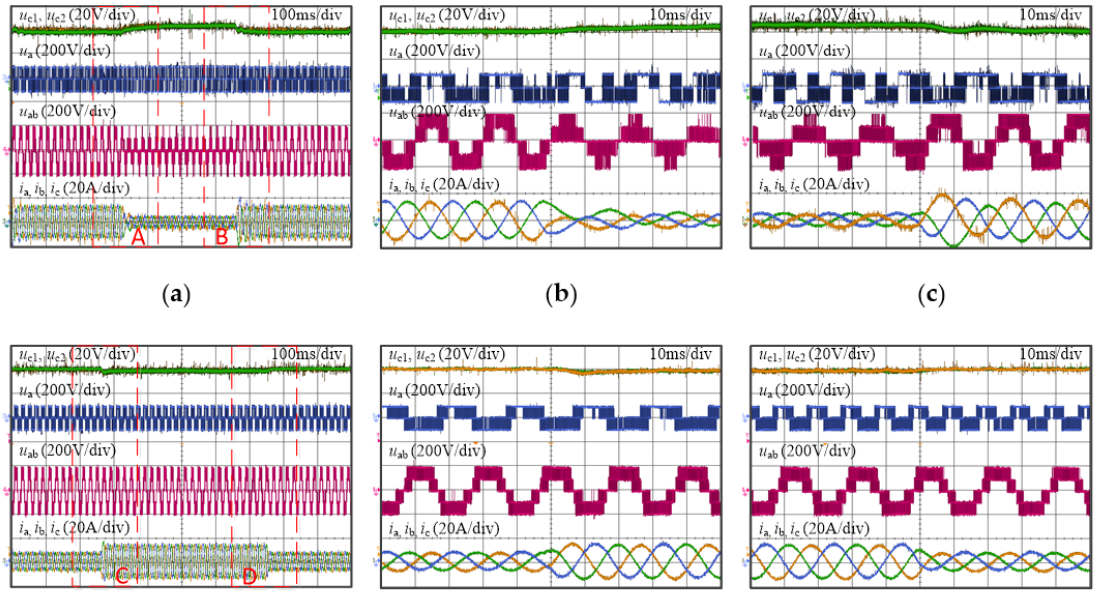
When $m = 0.3$, the three-phase voltage for FRCVBPWM and VSVPWM in one fundamental period are shown in Figure 13. Under VSVPWM, the switching sequence of one phase is composed of levels 0, 1 and 2, and the other two phases are composed of two levels. Thus, there are in total four switching actions for the three phases in one switching cycle. Under FRCVBPWM, the switching sequence of one phase is composed of levels 0, 1 and 2, and one phase is composed of two levels, and one phase is clamped. Thus, there are in total three switching actions for the three phases in one switching cycle.

The dynamic experimental results of the proposed FRCVBPWM are presented in Figure 14, including a sudden change of $m$ and load, respectively. From the dynamic experimental results, it can be seen that not only is DC offset, but also an AC ripple does not appear on the capacitor voltage. Therefore, the proposed FRCVBPWM has excellent capacitor voltage control performance both in steady state and dynamic process.




(**a**) (**b**)

**Figure 13.** The waveforms of three phases voltage for FRCVBPWM and VSVPWM: (**a**) VSVPWM, and (**b**) FRCVBPWM.




(**a**) (**b**) (**c**)

(**d**) (**e**) (**f**)

**Figure 14.** Dynamic experimental results of FRCVBPWM: (**a**) a sudden change of $m$ between 70.3 and 0.9, (**b**) partially enlarged waveforms of region A, (**c**) partially enlarged waveforms of region B, (**d**) a sudden change of load, (**e**) partially enlarged waveforms of region C, and (**f**) partially enlarged waveforms of region D.

## 8. Conclusions

Because one phase is clamped, the switching action number of the proposed FRCVBPWM is reduced from 3N − 5 to 2N − 3 compared to VSVPWM for DCMLI applications, which greatly reduces switching loss. However, the full range capacitor voltage balance can be effectively achieved for FRCVBPWM, just like VSVPWM. Therefore, it can be concluded that the proposed FRCVBPWM has significant advantages in balancing capacitor voltage and reducing switching loss.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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