



Seonghee Kho¹ and Hyunbum Park^{2,*}

- ¹ Department of Defense Science & Technology-Aeronautics, Howon University, 64 Howondae 3gil, Impi, Gunsan 54058, Korea; habari@paran.com
- ² School of Mechanical Convergence System Engineering, Kunsan National University, 558 Daehak-ro, Miryong-dong, Gunsan 54150, Korea
- * Correspondence: swordship@daum.net; Tel.: +82-(0)63-469-4729

Abstract: In this study, a real-time engine model and a test bench were developed to verify the performance of the EECU (electronic engine control unit) of a turbofan engine. The target engine is a DGEN 380 developed by the Price Induction company. The functional verification of the test bench was carried out using the developed test bench. An interface and interworking test between the test bench and the developed EECU was carried out. After establishing the verification test environments, the startup phase control logic of the developed EECU was verified using the real-time engine model which modeled the startup phase test data with SIMULINK. Finally, it was confirmed that the developed EECU can be used as a real-time engine model for the starting section of performance verification.

Keywords: test bench; EECU (electronic engine control unit); turbofan engine



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1. Introduction

The EECU is a very important component in aircraft engines, and the verification test for numerous items should be carried out in its development process. Since it takes a lot of time and cost to carry out such verification test using an actual engine, and an expensive engine may be damaged or a safety hazard may occur, the simulator which virtually generates the same signals with the actual engine is essential [1]. The virtual engine simulator which replaces the actual engine should be able to provide the simulation of engine operation in real time at almost the same level as the actual engine operation. Therefore, the simulation speed should be as fast as the speed of the actual system to carry out input, calculation and output within the time range specified by the user. The development of a real-time engine model which can carry out calculation at almost real time and appropriate hardware is necessary for real-time simulation.

Many studies of electronic engine control systems of gas turbine engines have been conducted. Among the previous studies, W.J. Davies et al. performed F-14 aircraft and propulsion control integration evaluation. Their paper presented the FADEC/F-14 integration evaluation performed by PWA and discussed the benefits of the FADEC/F-14 integrated system [2]. H. Yamane et al. carried out an investigation on aspects of aircraft engine control systems. In their work, various electronic control systems for aircraft engines were proposed [3]. F. Schwamm conducted research on FADEC computer systems for safety-critical applications. In Schwamm's work, the trends in FADEC development were investigated [4]. K. Hjelmgren et al. performed a study on the reliability analysis of single-engine aircraft FADEC. Their paper presented a reliability analysis of two options to fault-tolerant FADEC intended for control of an aircraft gas turbine engine [5]. K. Ito et al. performed a study on the optimal self-diagnosis policy for FADEC of gas turbine engines. In their paper, FADEC is self-diagnosed at the nth control calculations. Numerical examples were finally provided [6]. Ding Shuiting et al. conducted a study on the FHA (functional

hazard assessment) method for the VBV (variable bleed valve) position control function of a FADEC system based on an aero engine dynamic model [7]. G.I. Pogorelov et al. carried out research on application of neural network technology and high-performance computing for identification and real-time hardware-in-the-loop simulation of gas turbine engines [8]. Keeyoung Choi et al. performed a study on the development of an integrated high-fidelity helicopter and engine simulation for control system design [9]. Kang-Yi Lee et al. carried out a study on the certification of electronic engine controls [10]. Joo-Hyun Jung et al. conducted a study on the T-50 engine airstart test. Their paper presented the results of airstart tests performed to verify the T-50 airstart capability for various flight conditions [11]. F. Lu et al. performed research on rotating detonation wave propulsion about experimental challenges, modeling, and engine concepts [12]. S. Jafari et al. conducted a study on meta-heuristic global optimization algorithms for aircraft engine modeling and controller design [13]. S. Jafari et al. conducted a study on modeling and control of the starter motor and startup phase for gas turbines [14]. M. Montazeri-Gh et al. performed research on bond graph modeling of a jet engine with an electric starter [15]. A. Imani et al. studied the research on multi-loop switching controllers for aircraft gas turbine engines with stability proof [16]. Salehi. A. et al. conducted a study on hardware-in-the-loop simulation of a fuel control actuator of a turboshaft gas turbine engine [17]. M. Montazeri-Gh et al. analyzed different numerical linearization methods for the dynamic model of a turbofan engine [18]. M. Song et al. conducted research on optimization for the starting process of a turbofan engine under a high-altitude environment [19]. J. Bai et al. carried out a study on a nonlinear single controller of the DGEN380 aero engine design [20]. Y. Qian et al. conducted a study on LPV/PI control for a nonlinear aero engine system based on guardian maps theory [21]. I. Yazar et al. carried out research on a simulation-based dynamic model and speed controller design of a small-scale turbojet engine [22]. K. Beneda developed modular FADEC for a small-scale turbojet engine [23]. J. Lutambo conducted a study on aircraft turbine engine control system development [24]. Bai Jie carried out research on controller design for a small aero engine [25]. S. Victor et al. performed a study on robust control system design of a turbofan [26]. J. W. Connolly et al. conducted research on propulsion control modeling for a small turbofan engine [27]. Joseph. W. et al. carried out a study on advanced control considerations for turbofan engine design [28]. J. Csank et al. performed a study on a model-based engine control architecture with an extended Kalman filter [29]. R. Andoga conducted a study on intelligent situational control of small turbojet engines [30].

After many years of study, various theories of electronic engine control systems for gas turbine engines have been proposed. Even though various engine control design theories have been proposed, little research work on the development of experimental equipment for electronic engine control systems has been conducted.

In this study, our research group developed a real-time engine model which was essential for the development of the EECU, a core device in the aircraft engine, and the test bench which embedded the real-time engine model on the real-time simulator and generated the same physical signal with the sensor signal from the actual engine. The test bench's function test and the test bench's interface and interworking test were performed. Additionally, then, the real-time startup phase engine model verification test, real-time normal operation phase engine model verification test and target EECU performance verification test were carried out using the developed test bench. Finally, the test results were analyzed.

2. Engine Model

2.1. Target Engine

The target engine for the EECU to be developed is a small turbofan engine which is a two-spool and non-mixing type. The general specifications of the target engine are as shown in Table 1. The target engine is a DGEN 380 turbofan engine. Figure 1 shows the configuration of the target engine. Figure 2 shows the configuration and station numbers employed for a two-spool turbofan engine.

Table 1. Specification of target engine.

Specification	Value
Maximum take-off thrust (TOP, ISA, SL, MN0)	2500 N
Specific fuel consumption (SFC TOP)	0.0438 kg/N/h
Maximum cruise thrust (MCR, ISA, SL, MN0.338)	1170 N
Specific fuel consumption (SFC MCR)	7.58
Weight (without nacelle)	80 kg



Figure 1. DGEN 380 turbofan engine (Price Induction[©], Anglet, France).



Figure 2. Station numbering for the target engine.

2.2. Real-Time Startup Phase Engine Modeling

In this study, a real-time heat flow transient performance model was developed. The heat flow model is the most accurate model of the real-time engine models. This method does not require iteration. Therefore, it is a real-time engine model most commonly used for engine control system hardware development. In this work, a model was developed by applying the following equation [31]:

$$\frac{d\rho_4}{dt} = \frac{(W_3 - W_4 + WF)}{v} \tag{1}$$

where $\frac{d\rho_4}{dt}$ is the change rate of the density at the combustor outlet, and v is volume of the combustor.

$$\frac{dT_4}{dt} = \frac{CP_3 \times T_3 \times W_3 - CP_4 \times T_4 \times W_4 + WF \times LHV)}{CV \times T_4 \times v \times \frac{d\rho}{dt}}$$
(2)

where *LHV* is the fuel calorific value. Equation (2) is the change rate of the temperature at the combustor outlet.

$$P_4 = \left(1 + \frac{\gamma - 1}{2} \times M^2\right)^{\frac{1}{\gamma - 1}} \times R \times T \times \frac{(W_{in} - W_{out})}{v}$$
(3)

$$DP_{cold} = K_{cold} \times P_{31} \times \left(W_{31} \times \frac{\sqrt{T_{31}}}{P_{31}}\right)^2$$
(4)

where DP_{cold} is the cold loss of the combustor, K_{cold} is the cold loss value and M is the Mach number of the turbine inlet.

$$DP_{hot} = K_{hot} \times P_{31} \times \left(\frac{T_4}{T_{31}} - 1\right) \times \left(W_{31} \times \frac{\sqrt{T_{31}}}{P_{31}}\right)^2$$
 (5)

where DP_{hot} is the heat loss of the combustor, and K_{hot} is the heat loss value.

$$W = Q \times \frac{P}{\sqrt{T}} \tag{6}$$

$$T_4 - T_5 = T_4 \times \eta_4 \times (1 - \frac{1}{PR_{4,5}^{\frac{\gamma-1}{\gamma}}})$$
(7)

$$\frac{P_1 - P_0}{P_0} = 100 \times (1 - RRF) \times \frac{P_0 - P_{amb}}{P_0}$$
(8)

where *RRF* is the ram recovery coefficient.

$$T_3 - T_2 = T_2 \times \frac{PR_{2,3}^{\frac{\gamma-1}{\gamma}} - 1}{\eta_2}$$
(9)

$$\frac{dP}{dt} = \left(1 + \frac{\gamma - 1}{2} \times M^2\right)^{\frac{1}{\gamma - 1}} \times R \times T \times \frac{W_{in} - W_{out}}{v}$$
(10)

where $\frac{dP}{dt}$ is the pressure change rate of the volume. A real-time transfer function transient performance model was considered by the following equation:

$$NL(t) = WF(t) \times \left(1 - \frac{TC_{lead}}{TC_{lag}}\right) + \left(1 - \frac{TC_{lead}}{TC_{lag}}\right) \times \left[NL(t-1) + \left(NL(t) - WF(t-1) \times (1 - e^{\frac{dt}{TC_{lag}}}\right)\right]$$
(11)

where NL(t) is the number of revolutions of the low-pressure turbine at time t. A realtime lumped parameter transient performance model was considered by the following equation. The partial derivative of the state variable is obtained from all other parameters.

$$\frac{\partial NL}{\partial t} = \frac{\partial NLdot}{\partial NL} \times (NL - NL_b) + \frac{\partial NLdot}{\partial NH} \times (NH - NH_b) + \frac{\partial NLdot}{\partial WF} \times (WF - WF_b)$$
(12)

where *b* is the operating point.

The modeling of the real-time startup phase engine model in the form of a lookup table based on time was carried out through the reconfiguration of startup phase test data measured from the target engine EECU, as shown in Figure 3. The real-time startup phase engine model was composed of a "Master Switch" module which played the role to start

the engine, a "Startup Real Test" module which provided startup phase data for 0~109 s in the lookup table and an "Engine Simulator" module which generated a physical signal by converting all output signals into analog and discrete signals. Additionally, a "switch model" was added to simulate the short circuit test by assigning a switch to all signals separately and turning on or off a certain signal during the simulation. SIMULINK was used, as shown in Figure 3. In order to load the modeled real-time startup phase engine model on the engine simulator, SIMULINK was used.



Figure 3. Real-time engine model of startup phase.

3. Test Bench Development

In this study, the test bench (TB) was configured for the purpose of verifying the target EECU by loading the real-time engine model. The test bench was configured to satisfy the requirements to enable the integrated performance test of the target EECU. The test bench provided the interface for installing and operating the target EECU as well as the virtual engine which could simulate fault signal input and the same input and output signals as the actual engine through the dual channel.

The test bench consists of a hardware unit (HW) including a real-time engine simulator, a flight vehicle/cockpit simulator, a software simulator, a mapping box, cables and connectors, a power supply unit, a console and desk and a monitor and operating software unit (SW).

The hardware unit in the test bench consists of a "cockpit simulator" which handles the operation and management of the test bench, management of the test database of the test bench and target engine, management of the ARINC429 communication and data and operation and management of the EHD module, a "real-time engine simulator" which is embedded with the real-time engine model simulating the same performance as the actual engine and simulates engine and drive system signals in real time, "engine controls" which play the role of the cockpit where hardwire signals are sent to the EECU directly and various switches are operated to control the EECU through mechanical production of a PLA lever which adjusts the engine thrust and a "software simulator" which carries out the modeling of the real-time engine embedded in the engine simulator or plays the role of the host PC for the engine simulator and uploads software on the target EECU. HW block diagrams of the test bench are shown in Figure 4.





The test bench operation software was programmed using NI LabVIEW, and it consists of a "TB Operation" program of the main GUI which operates and controls the whole test bench, an "EECU Monitoring" program which monitors and uses the target EECU and all input and output signals through the ARINC429 communication, an "EECU Test" program which can monitor and save data in the verification tests such as the target EECU performance test, logic test and startup phase test and an "EHD" program which creates a database of data saved after the target engine test offline and carries out state diagnosis, trend monitoring and maintenance phase management. SW block diagrams of the test bench are shown in Figure 5, and the detailed specifications of the developed TB are shown in Table 2. The conceptual diagram of the developed TB is shown in Figures 6 and 7.



Figure 5. Structure of test bench operational SW.

		Classify	Specification
		Temperature Sensor	RTD (8 Ch), Thermocouple (6 Ch), PTC (2 Ch)
		Pressure Sensor	12 Ch
		Glowplug Current	2 Ch
	Output	RPM Sensor	4 Ch
Engine Simulator	-	PLA Sensor	2 Ch
		Frequency	6 Ch
		Discrete	14 Ch
	Input	Discrete	12 Ch
		PWM	6 Ch
	С	ommunication	ARINC429 (2 Ch), RS232 (2 Ch), Ethernet (2 Ch)
Cockpit Simulator	Output	PLA Sensor	2 Ch
		Discrete	22 Ch
	Input	Discrete	22 Ch

 Table 2. Required specification of test bench.



Figure 6. Conceptual diagram of developed test bench.



Figure 7. Test bench integration.

4. EECU Verification Test

4.1. Functional Test of Test Bench

The manufactured test bench is shown in Figure 7. The state of the test bench was inspected through the functional test after integrating the test bench. For the functional test of the test bench, the inspection cable was connected to each pin at the end of the cable directly connected to the target EECU. The test items, standards and methods for the signals in all items of channels A and B were summarized as shown in Table 3. Three measurements were carried out for each test item, and if all measurement values were within the error range, an "OK" judgment was given.

N	Test Items	Standard Mathod	Asthod Bafaranaa		Measur	ement (C	ase No.)	Desision		
INO.	No. lest items Standard Method Reference		rerence	X1	X2	X3	- Decision			
1		Master (0/5 V,		0 V < X	< 2.6 V (ON)	0.698	0.699	0.698	01/	
1		FS ± 10%)		2.6 V < 2	X < 5 V (OFF)	4.05	4.05	4.05	- OK	
		IGN	-	0V < X	< 2.6 V (ON)	0.702	0.703	0.701		
2		DCRANK	-	0 V < X	< 2.6 V (ON)	0.684	0.684	0.684	OK	
		WCRANK	-	0 V < X	< 2.6 V (ON)	0.696	0.696	0.696	-	
	3 CH. Nor A Discrete Output				IGN	2.6 V < X < 5 V (OFF)	4.8	4.8	4.8	
3		CH. Normal A Discrete	Digital	DCRANK	2.6 V < X < 5 V (OFF)	4.8	4.8	4.8	OK	
			Multimeter	WCRANK	2.6 V < X < 5 V (OFF)	4.8	4.8	4.8	-	
		WOW (0/5 V,	-	0 V < X	< 2.6 V (ON)	0.704	0.704	0.704	OK	
4		FS ± 10%)		2.6 V < X < 5 V (OFF)		4.8	4.8	4.8	- OK	
		CH_A	-	0 V < X	< 2.6 V (ON)	0.7	0.7	0.7		
5	5 CH_AUTO CH_B	-	0 V < X < 2.6 V (ON)		0.692	0.692	0.692	OK		
		CH_B	-	0 V < X	< 2.6 V (ON)	0.690	0.690	0.690	-	
6		OFCsts (0/5 V,	-	0 V < X	< 2.6 V (ON)	0.142	0.141	0.141	OV	
6	$FS \pm 10\%$)		2.6 V < 2	X < 5 V (OFF)	4.21	4.22	4.22	- UK		

Table 3. Result of test bench functional test (discrete output_CH_A).

The result of the functional test is as shown in Table 4, and the measurement values for all test items in channels A and B are within the error range; therefore, it can be regarded that the functional reliability of the test bench for the verification test of the target EECU has been secured.

No	Test Items		Test Result		
INU.	lest	Test items		Ch. B	
1		MASTER	OK	ОК	
2		IGN	OK	OK	
3		DCRANK	OK	OK	
4		WCRANK	OK	OK	
5		NORMAL	OK	OK	
6		WOW	OK	OK	
7		CH_A	OK	OK	
8	Discrete Output	CH_AUTO	OK	OK	

No	Test	Task Ikama		Test Result		
INO.	Test Items		Ch. A	Ch. B		
9		CH_B	OK	OK		
10		OFCsts	OK	OK		
11		FFCsts	OK	OK		
12		OLLsts	OK	OK		
13		FMVsts	OK	OK		
14		FSVsts	OK	OK		
15		OSOVsts	OK	OK		
16		GPcmd	OK	OK		
17		FMVcmd	OK	OK		
18	Discrete Input	FSVcmd	OK	OK		
19	Discrete input	OSOVcmd	OK	OK		
20		SGstart	OK	OK		
21		SGmode	OK	OK		
22		PS3	OK	OK		
23		P0	OK	OK		
24		PFuel	OK	OK		
25		POil	OK	OK		
26		T6	OK	OK		
27		T0	OK	OK		
28		TFuel	OK	OK		
29	Applog Output	TOil	OK	OK		
30	Analog Output	TSG	OK	OK		
31		GPcur	OK	OK		
32		PLA	OK	OK		
33		NH	OK	OK		
34		NL	OK	OK		
35		FPMspd	OK	OK		
36		OPMspd	OK	OK		
37		SGspd	OK	ОК		
38		FPMcmd	OK	OK		
39	Analog Input	OPMcmd	OK	OK		
40		SGcmd	OK	OK		

4.2. EECU Interface and Interworking Test

The interface and interworking test between the test bench and target EECU is the test to check if the data transmission and reception between the test bench and target EECU through the ARINC429 communication are carried out smoothly after connecting the test bench and EECU with a cable and operating the test bench operating program. The interface and interworking test was carried out in the process as shown in Figure 8.

At this time, a separate interface test engine model was embedded in the engine simulator, and the test items, standards and methods for the signals in all items of channels A and B were summarized as shown in Table 5 in a similar way to the functional test. Three measurements were carried out for each test item, and if all measurement values were within the error range, an "OK" judgment was given.

The result of the interface and interworking test between the test bench and target EECU is as shown in Table 6, where it is confirmed that all test items in channels A and B were within the error range. Therefore, it can be regarded that the functional reliability for data signals through the communication between the test bench and target EECU has been secured for the following verification test of the target EECU.



Figure 8. Process of interface test.

Table 5. Result of interface	and interworking test	(discrete output CH	A).
indic 5. Result of interface	and miter working test	(uberete output_err_	<u>, , , , , , , , , , , , , , , , , , , </u>

No.	Test Items	Standard	Method	Reference	Me	asurement (Case N	No.)	Decision	
1	1		Master	MASTER	ON	ON	ON	ON	OV
1		(ON/OFF)	Switch	OFF	OFF	OFF	OFF	- OK	
		IGN (ON)		IGN	IGN	IGN	IGN		
2		DCRANK (ON)	MODE Switch	DCRANK	DCRANK	DCRANK	DCRANK	ОК	
		WCRANK (ON)	ownen	WCRANK	WCRANK	WCRANK	WCRANK		
3		NOMAL (ON)		NOMAL	NOMAL	NOMAL	NOMAL	OK	
4		WOW	WOW	Ground	Ground	Ground	Ground	OK	
4		(ON/OFF)	Switch	Flight	Flight	Flight	Flight	- OK	
	-	CH_A		CH_A	CH_A	CH_A	CH_A		
5	CH.	CH_AUTO	Channel Switch	CH_AUTO	CH_AUTO	CH_AUTO	CH_AUTO	OK	
	A Discrete	CH_B		CH_B	CH_B	CH_B	CH_B		
	Output	OFCsts (0/5 V)	Engine	Discrete, 0	Clogged	Clogged	Clogged	OK	
6			Simulator	Discrete, 1	Not Clogged	Not Clogged	Not Clogged	- UK	
		EECata (0/E V)	Engine	Discrete, 0	Clogged	Clogged	Clogged	OK	
7		$\operatorname{PPCSIS}\left(0/5V\right)$	Simulator	Discrete, 1	Not Clogged	Not Clogged	Not Clogged	· UK	
		OLLata (0/5 M)	Engine	Discrete, 0	Low Oil	Low Oil	Low Oil	OK	
0		OLLSIS $(0/5 V)$	Simulator	Discrete, 1	Enough Oil	Enough Oil	Enough Oil	UK	
		FMVsts	Engine	Discrete, 0	Open	Open	Open	OV	
9	9	(0/5 V) Simulator	Simulator	Discrete, 1	Closed	Closed	Closed	UK	
10		ESVata (0 / 5 V)	Engine	Discrete, 0	Open	Open	Open	OV	
10		137515(0/37)	Simulator	Discrete, 1	Closed	Closed	Closed	UK	
	-	OSOVsts	Engine	Discrete, 0	Open	Open	Open	OV	
11		(0/5 V)	Simulator	Discrete, 1	Closed	Closed	Closed	UK	

NT	Track Hearing		Test R	Test Result		
N0.	lest	ltems	Ch. A	Ch. B		
1		MASTER	OK	OK		
2		IGN	OK	OK		
3		DCRANK	OK	OK		
4		WCRANK	OK	OK		
5		NORMAL	OK	OK		
6		WOW	OK	OK		
7		CH_A	OK	OK		
8	Discrete Output	CH_AUTO	OK	OK		
9	-	CH_B	OK	OK		
10		OFCsts	OK	OK		
11		FFCsts	OK	OK		
12		OLLsts	OK	OK		
13		FMVsts	OK	OK		
14		FSVsts	OK	OK		
15		OSOVsts	OK	OK		
16		GPcmd	OK	OK		
17		FMVcmd	OK	OK		
18	Discrete Input	FSVcmd	OK	OK		
19	Disciele input	OSOVcmd	OK	OK		
20		SGstart	OK	OK		
21		SGmode	OK	OK		
22		PS3	OK	OK		
23		P0	OK	OK		
24		PFuel	OK	OK		
25		POil	OK	OK		
26		T6	OK	OK		
27		Т0	OK	OK		
28		TFuel	OK	OK		
29	Analog Output	TOil	OK	OK		
30	Thinking Output	TSG	OK	OK		
31		GPcur	OK	OK		
32		PLA	OK	OK		
33		NH	OK	OK		
34		NL	OK	OK		
35		FPMspd	OK	OK		
36		OPMspd	OK	OK		
37		SGspd	OK	OK		
38		FPMcmd	OK	OK		
39	Analog Input	OPMcmd	OK	OK		
40		SGcmd	OK	OK		

 Table 6. Result of EECU test bench interface test.

4.3. Real-Time Engine Model Verification Test

The interworking test with the target EECU was carried out by loading the startup phase real-time engine model established from data obtained through trial operation of the target engine on the engine simulator.

It was confirmed from the NH, NL, T6 and FMVsts result on the startup phase that the test data matched well within 1% in the whole startup phase, as shown in Figures 9–11, and data were saved in a fixed time interval (0.02 s). Therefore, it was confirmed that analog sensor output signals and discrete output signals of the actual engine were monitored in the engine simulator embedded in the real-time engine model through the ARINC429 communication, and the signals were within the permissible error range of the target EECU. It was verified that this model could be used as the startup phase real-time engine model for the startup phase performance verification of the target EECU.



Figure 9. Result of startup phase performance test (NH).



Figure 10. Result of startup phase performance test (NL).



Figure 11. Result of startup phase performance test (T6).

4.4. Startup Phase Control Logic Verification Test

EECU software consists of a control logic, application software and a real-time operating system. Here, the control logic handles the engine speed control, sequence control, engine state monitoring and engine protection functions. It is the most important part in the development of EECU software. The application software handles the system communication interface and dual channel management, and the real-time operating system manages the tasks of the application program to be carried out in a consistent and appointed time.

The verification test of the control logic which performed the most important role in the EECU software was carried out using the test bench developed through this study. Currently, the target EECU is being developed in the country. Therefore, the test was carried out for the control logic of the startup phase which was developed up to date. When the target EECU is developed completely in the future, the control logic test will be carried out for the whole operation phase of the target engine. The startup phase control logic test was carried out in the process as shown in Figure 12.

The EECU delivers FPMcmd, FMVcmd and FSVcmd output values according to the control logic calculation result to the engine in the startup phase, as shown in Figures 13–15, and the engine receives the input of this command. The result shows that the control logic in the early stage of development shows a significant difference from the reference data. Therefore, the reasons for the error occurrence from the control log were analyzed, and the control logic was modified accordingly. The test was carried out again until the final control logic test result almost matched with the target data.



Figure 12. Process of control logic performance test.



Figure 13. Result of EECU control logic verification test (FPMcmd).



Figure 14. Result of EECU control logic verification test (FMVcmd).



Figure 15. Result of EECU control logic verification test (FSVcmd).

5. Conclusions

A test bench for the performance test of an EECU was developed, and the test was carried out. The test bench's functional test, test bench's interface and interworking test, real-time startup phase engine model verification test and target EECU performance verification test were carried out using the configured test bench, and the test results were analyzed.

As the result of the TB functional test, the measurement values for all test items in channels A and B were within the error range; therefore, the functional reliability of the test bench for the verification test of the target EECU was secured. As a result of the interface and interworking test between the test bench and target EECU, it was confirmed that all test items in channels A and B were within the error range. Therefore, the functional

reliability for data signals through the communication between the test bench and target EECU was secured for the verification test of the target EECU.

As a result of the startup phase verification test after the verification of the test bench, it was confirmed that analog sensor output signals and discrete output signals of the actual engine were monitored and saved accurately in a 0.02 s interval in the engine simulator embedded in the real-time engine model through the ARINC communication, and the signals were within the permissible error range of the target EECU. Therefore, it was confirmed that this model could be used as the startup phase real-time engine model for the startup phase performance verification of the target EECU. Additionally, as a result of the control logic test, the control logic in the early stage of development showed a significant difference from the reference data. Therefore, the reasons for the error occurrence from the control log were analyzed, and the control logic was modified accordingly. The test was carried out again until the final control logic test result almost matched with the target data. Currently, the target EECU is being developed in the country. Therefore, the test was carried out for the control logic of the startup phase which was developed up to date. When the target EECU is developed completely in the future, the control logic test will be carried out for the whole operation phase of the target engine.

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Abbreviations

EECU	electronic engine control unit
ρ	density
t	time
ν	volume
LHV	fuel calorific value
DP _{cold}	cold loss of combustor
DP _{hot}	heat loss of combustor
K _{cold}	cold loss value
<i>K</i> _{hot}	heat loss value
RRF	ram recovery coefficient
RTD	resistance temperature diode
PTC	positive temperature coefficient thermistor
EHD	engine health diagnostic
GUI	graphical user interface
EECU	electronic engine control units
Р	pressure
NL(t)	the number of revolutions of low pressure at time t
В	operating point

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