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# Advanced Modulation Scheme of a Dual-Active-Bridge Series Resonant Converter (DABSRC) for Enhanced Performance

Asad Hameed <sup>1,†</sup> , Ali Nauman <sup>2,†</sup> , Munleef Quadir <sup>3,\*</sup>, Irfan Latif Khan <sup>1</sup> , Adeel Iqbal <sup>1</sup> , Riaz Hussain <sup>1</sup>   
and Tahir Khurshaid <sup>4,\*</sup> 

<sup>1</sup> Department of Electrical and Computer Engineering, COMSATS University, Islamabad 45550, Pakistan  
<sup>2</sup> Department of Information and Communication Engineering, Yeungnam University, Gyeongsan 38541, Republic of Korea  
<sup>3</sup> Department of Computer Science and Information Technology, Jazan University, Jazan 45142, Saudi Arabia  
<sup>4</sup> Department of Electrical Engineering, Yeungnam University, Gyeongsan 38541, Republic of Korea  
\* Correspondence: mquadir@jazanu.edu.sa (M.Q.); tahir@ynu.ac.kr (T.K.)  
† These authors contributed equally to this work.

**Abstract:** This paper proposes a two-degree-of-freedom (2-DoF) modulation technique for the efficient optimization of an open-loop three-phase dual-active-bridge series resonant converter (3P-DABSRC). The efficiency and performance of a conventional dual-active-bridge (DAB) converter decrease when it is operated over a wide range of voltage gain. The efficiency and performance of a DAB converter depend upon the switching and conduction losses. Circulating current is the main cause of conduction loss, and hard switching of active switches adds a switching loss. To increase the performance of DAB converters, the first objective is to minimize the conduction loss, and the second objective is to reduce the switching loss. Still, unfortunately, it is not easy to achieve these two objectives simultaneously. Circulating current helps us to reduce the switching loss, but the unbridled amount of circulating current will increase the root-mean-square inductor tank current, and as a result, the conduction loss will be increased. This paper presents an advanced modulation scheme for a 3P-DABSRC that can be used not only in low-power applications, but also in high-power applications. The DABSRC consists of a series LC resonant tank, isolated high-frequency transformer, and dual active bridge connected with the primary and secondary sides of the transformer. The proposed 2-DoF modulation technique not only minimizes the circulating current, but also eliminates the switching loss. Keeping the minimum phase shift between the primary and secondary bridges reduces the circulating current, and thus, all switches can be operated with zero-voltage switching (ZVS) for the entire power range. The power is controlled by changing the switching frequency from 45 to 63 kHz. To confirm the proposed topology and modulation scheme, a 1500 W DABSRC, which interfaces a 300 V DC bus with a 75 V DC bus, is simulated. A loss model of the proposed topology is also made to verify the results. The simulation results are used to confirm the proper operation of the 3P-DABSRC.

**Keywords:** dual-active-bridge series resonant converter; open loop; dual active bridge; switching loss; conduction loss; hard switching; circulating current; LC resonant tank; phase shift; switching frequency

MSC: 94C11



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## 1. Introduction

In recent years, bidirectional power flow has become an important feature in much electronic equipment. Bidirectional DC-to-DC converters (BDCs) play an important role in bidirectional power flow, such as in electric vehicles [1], dual-active-bridge battery chargers used in plug-in hybrid electric vehicles [2], HVDC grid integration [3], dual active bridges (DABs) with solid-state transformers [4], energy storage systems [5], DC microgrid energy

storage systems [6], fuel-cell vehicles and hybrid electric vehicles [7], plug-in chargers for electric vehicles (PEVs) [8], high-power battery-charging systems for PEVs and vehicle-to-grid (V2G) systems [9], and uninterruptible power supplies (UPSs) [10], as shown in Figure 1.

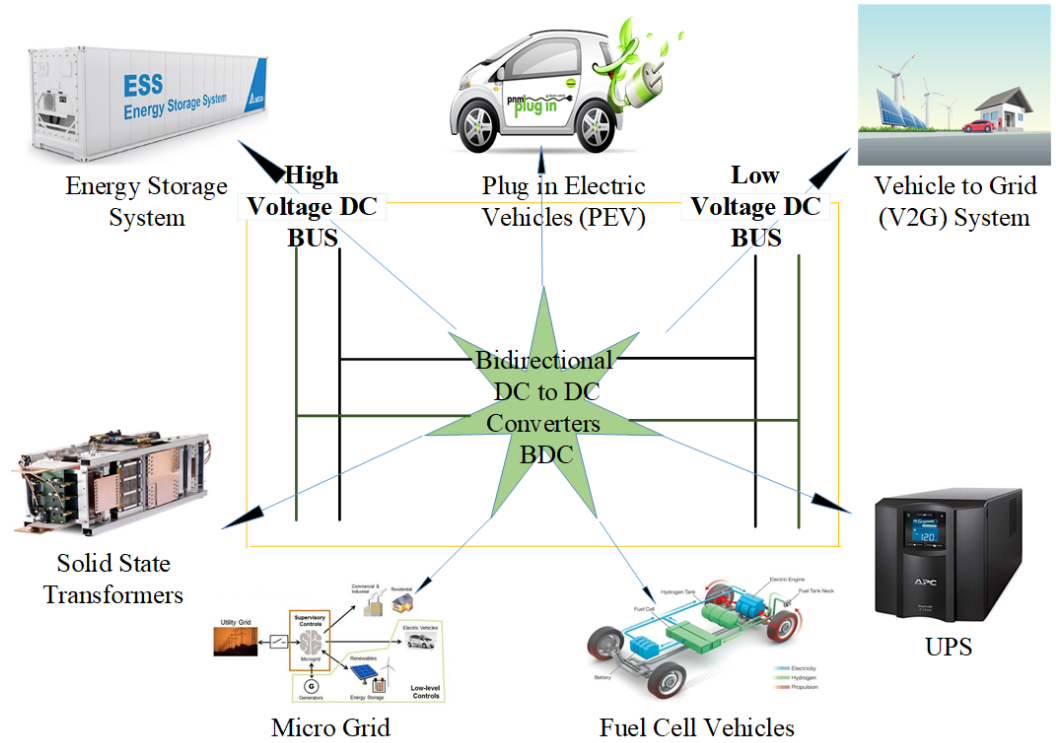
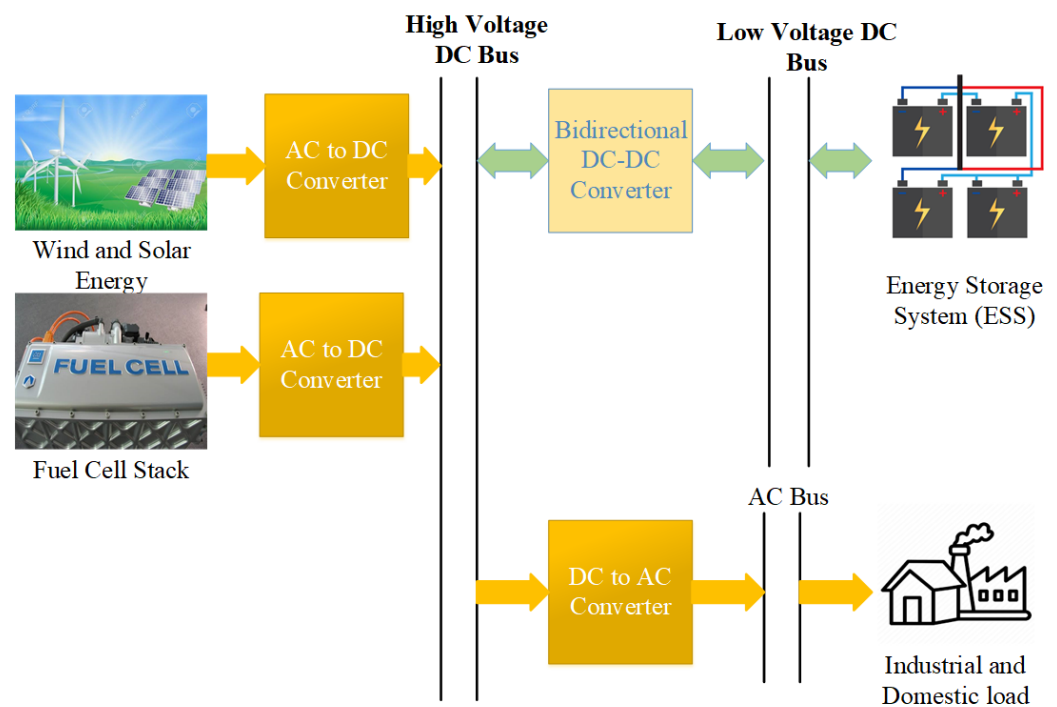


Figure 1. Applications of BDCs in various sectors.

Today, energy demand is constantly increasing around the globe. Unfortunately, the depletion of fossil fuels, such as natural gas and coal, is becoming a major concern for sustainable energy. Globally, the utilization of fossil fuel causes an increase in carbon emissions, which is harmful for the environment and results in climate change [11]. Due to the challenge of global warming, many transportation sectors are moving towards hybrid electric vehicles (HEVs) [12]. Hence, conventional power plants that use fossil fuel for the generation of electricity are shifting towards renewable smart power grids. Due to the increase in the harvesting of renewable energy in the power system, power generation units have been upgraded with intelligent controls [13,14]. The main drawback of renewable energy is that it is highly intermittent in nature. To cope with this problem, smart power grids must be equipped with an energy storage system to ensure an uninterrupted power supply, as shown in Figure 2. BDCs are the main part of a smart grid because they are used to integrate the DC bus with the energy storage system. This is the main reason for why BDCs play an important role in power systems. The reason that was elaborated above has led researchers to concentrate and focus their attention on BDCs. As a result, many researchers have proposed BDCs. BDC models are classified according to the number of switches, e.g., there are dual-switch (dual-flyback), three-switch (forward-flyback), four-switch (dual-half-bridge), five-switch (full-bridge-forward), six-switch (half-full-bridge), and eight-switch (dual-active bridge) models. Dual-active-bridge (DAB) DC–DC converters have many prominent features, including a high power density, low device stress, galvanic isolation, and easy control [15].



**Figure 2.** Smart grid.

The first BDCs were introduced in [16]. Since then, different types of BDC models have been explored. Among them, the three-phase with dual-active-bridge (3P-DAB) converter has become the best choice because of its high power density, high power transfer capability with a minimum root-mean-square (RMS) three-phase transformer current, low voltage stress on components, requirement of a low-rating filter capacitor, small ripple current, and ability to be operated in buck–boost mode. The above-mentioned advantages of 3P-DAB converters are the main reason for why such converters have become the foremost choice in high-power applications [17]. The conventional 3P-DAB shown in Figure 3 uses a low-voltage (LV) connector as a primary bridge and a high-voltage (HV) connector as a secondary bridge. These primary and secondary bridges are connected and coupled with a three-phase transformer by using a Y-Y connection. A 3P-DAB makes use of the transformer leakage inductance as a current and power-transfer element [18]. Research was conducted [19,20] on the different types of connections in a 3P-DAB, which included Y-Y, Y- $\Delta$ ,  $\Delta$ -Y, and  $\Delta$ - $\Delta$  connections. It turned out that Y-Y-connected transformers were verified to have far better current-sharing abilities than those of other three-phase topologies with various transformer connections [21,22]. From the point of view of control, the most popular and widespread modulation scheme for 3P-DAB is single-phase shift (SPS) because of its simplicity [23]. In SPS modulation, two square waves are applied across the power-transfer element. By varying the magnitude of the phase shift, the output power can be regulated, and by changing the sign of the phase shift, the direction of the power flow can be reversed. Although SPS modulation is very simple, unfortunately, it also suffers from a major drawback. This modulation scheme induces a circulating current that increases when the voltage gain ( $M = \frac{n \cdot V_0}{V_{in}}$ ) deviates from unity. Furthermore, zero-voltage switching (ZVS) drastically decreases under partial load conditions. As a result, the efficiency of 3P-DAB decreases, which makes it unfit in applications with vast voltage ranges. So, increasing the ZVS range and reducing the circulating current become the main objective. This has turned the focus of the researchers toward achieving these possibilities. To increase the efficiency of 3P-DAB converters under partial load conditions, many advanced modulation schemes have been introduced.

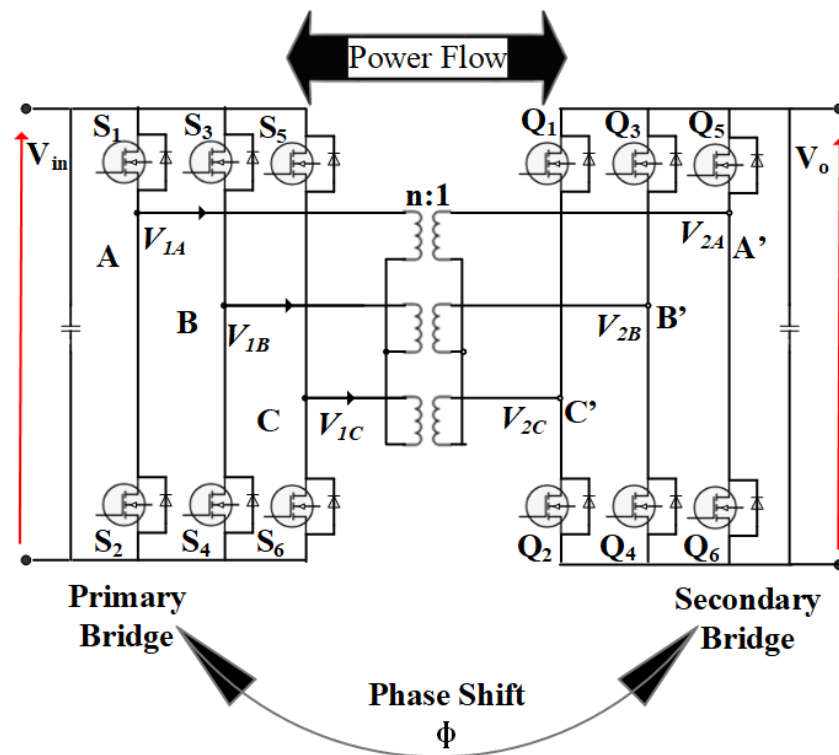


Figure 3. Conventional 3P-DAB converter.

The asymmetrical duty-cycle control (ADCC) modulation scheme and variable duty-cycle control with a dual-phase-shift (DPS) and extended-phase-shift (EPS) control were introduced in [24–26]. None of them were able to reduce the circulating current, achieve a full range of ZVS, or increase the partial load efficiency during operation in a vast voltage range. A DAB converter integrated with a dual transformer and dual tank is discussed in [27,28], but unfortunately, the dual transformer technique induced hard switching during the reversal of power, and the dual-tank technique decreased the ZVS range when the voltage gain was varied from unity. To achieve the full range of ZVS, a resonant converter integrated with a tuned CLLC tank was proposed in [29], but unfortunately, the circulating current in the proposed manuscript was increased. To increase the soft-switching range, an LLL-tank-based topology was also introduced in [30–32], but unfortunately, these modulation schemes caused an increase in the circulating current in wide-voltage-range applications. In addition, the frequency-based modulation scheme proposed in [33–37] had the drawback of having too much frequency variation. Another hybrid frequency- and phase-shift modulation scheme with a reconfigurable and tunable resonant network was introduced in [38], but it had a few drawbacks, such as complex control, a higher component count, and a bigger footprint. Similarly, the closed-loop SPS modulation scheme reported in [33] had the drawback of a vast frequency range, and it failed to reduce the circulating current.

To increase the efficiency of DAB converters by increasing the ZVS and reducing the circulating current, many modulation schemes were introduced, and they are discussed in this section. However, it is important to realize that the above-mentioned modulation schemes failed to attain the full range of soft switching, which increased the switching loss during conversion when operated in a wide voltage range. Moreover, it is not easy to achieve these two objectives at the same time due to their contrasting nature, i.e., circulating current is required to achieve zero-voltage switching (ZVS), but the presence of an excessive amount of circulating current is the main cause of conduction loss and low efficiency.

This paper proposes an open-loop three phase dual-active-bridge series resonant converter (3P-DABSRC) that is incorporated into a series LC resonant structure with a

frequency-based control modulation scheme. To reduce the voltage stress of the transformer, the HV and LV sides of the dual bridge are connected with the transformer by using a Y-Y connection, which has become the best candidate for high-voltage applications. This advanced topology can overcome the drawbacks of 3P-DAB converters. It was designed in such a way that through the frequency control modulation scheme, a full ZVS range is achieved with minimal reactive power, circulating current, backflow power, and reductions in conduction loss, as well as a complete elimination of hard switching. The comparison between the frequency modulation and SPS modulation techniques is shown in Figure 4, while Figure 5 gives ample reasons for the preference of the frequency modulation technique over the SPS modulation technique.

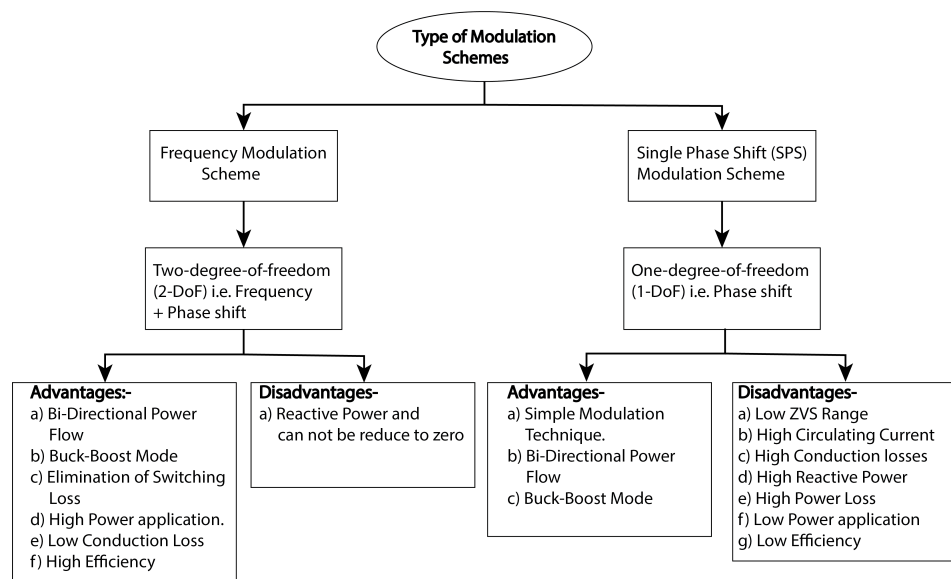


Figure 4. Comparison between the frequency modulation and single-phase shift (SPS) modulation techniques.

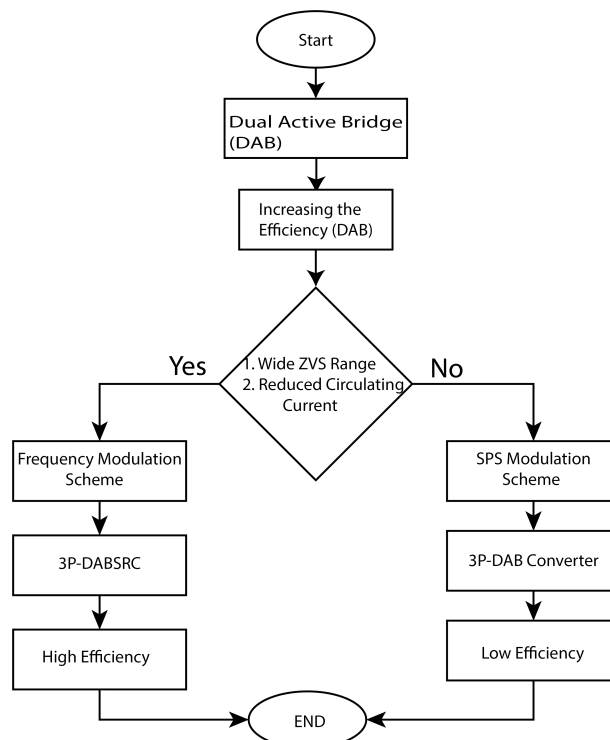


Figure 5. Preference for the frequency modulation technique over the SPS modulation technique.

### 2. Design and Analysis of the 3P-DABSRC

Figure 6 shows the proposed topology of the 3P-DABSRC. It consists of a high-frequency three-phase (Phase A, Phase B, and Phase C) dual active bridge. The two bridges are coupled to three single-phase transformers  $T_1, T_2, T_3$  with Y-Y connections and three series resonant tanks.  $n$  is defined as a turn ratio between the primary and secondary sides of the transformer. Each phase consists of a resonant tank that acts as a power-transfer element, and it consists of capacitors ( $C_A, C_B, C_C$ ) and inductors ( $L_A, L_B, L_C$ ) that are connected in series.

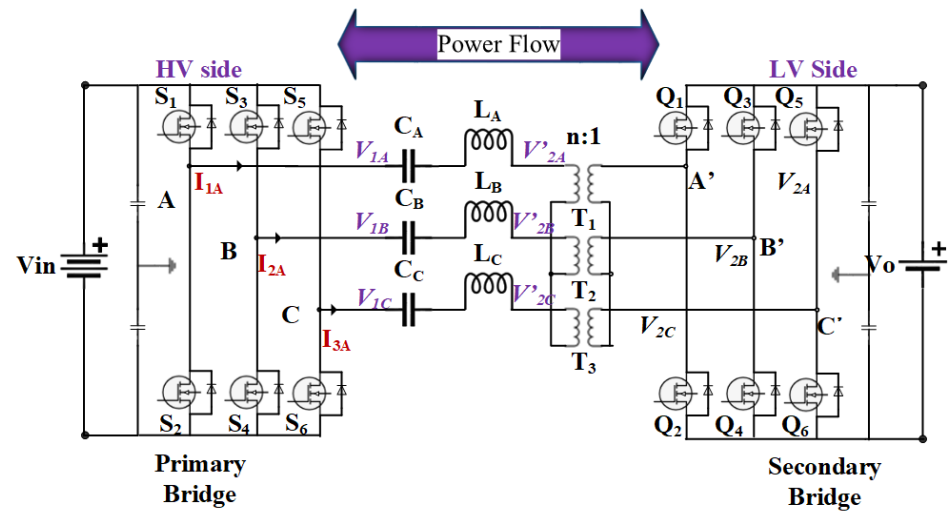


Figure 6. The 3P-DABSRC.

A duty cycle of 50% was selected for both bridges of the 3P-DABSRC. The proposed topology consisted of 12 MOSFET switches. Six MOSFETs ( $S_1$  to  $S_6$ ) were connected in the primary bridge, which was the HV side, and the rest of the MOSFETs ( $Q_1$  to  $Q_6$ ) were connected in the secondary bridge, which was the LV side. A subscript of 1 represents the input parameter and a subscript of 2 represents the output parameter. Two energy storage systems, i.e., a higher-voltage battery ( $V_{in}$ ) and lower-voltage battery ( $V_o$ ), were connected at the primary bridge (HV side) and secondary bridge (LV side), respectively. Two capacitors were connected in parallel across the input voltage ( $V_{in}$ ) and output voltage ( $V_o$ ); therefore, a two-step voltage was generated across the primary winding. The phase difference between phases A and B was  $120^\circ$ , and it was  $240^\circ$  between phases A and C, as shown in Figure 7. In the buck mode, the system transferred power from the HV side  $V_{in}$  to the LV side  $V_o$ , and in the boost mode, the system transferred power from the LV side  $V_o$  to the HV side  $V_{in}$ .

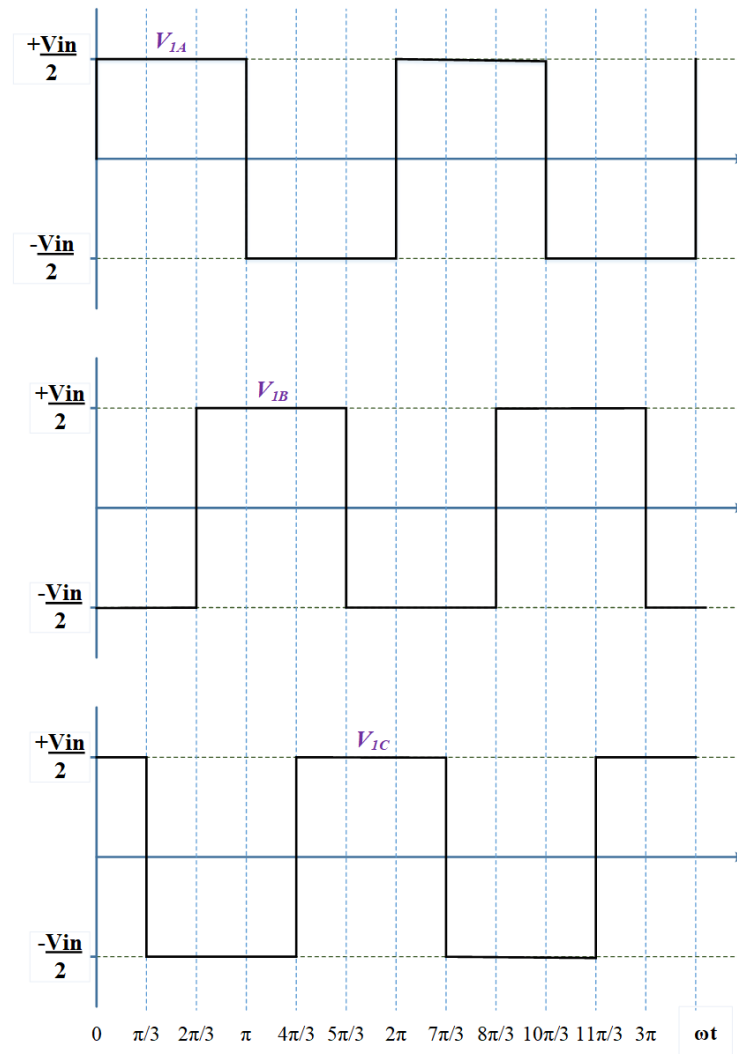


Figure 7. The primary-phase voltage waveform.

2.1. Mathematical Analysis of the 3P-DABSRC Converter

Figure 8 shows the per-phase equivalent circuit of the 3P-DABSRC converter.

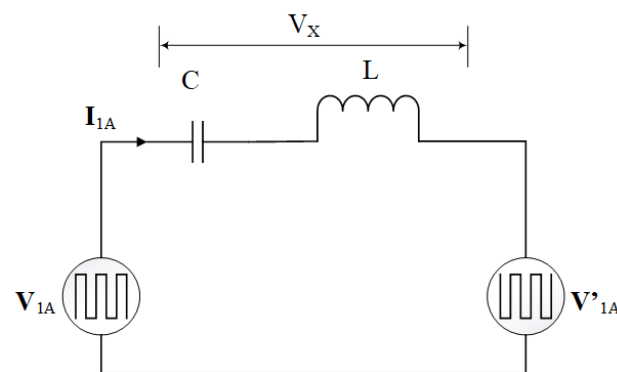


Figure 8. Equivalent circuit of the 3P-DABSRC converter.

The resonant tank behaves as a high-pass filter. This tank only facilitates the first or fundamental harmonic frequency of the input square wave and ignores the higher harmonic frequencies.  $V_x$  is the voltage across the resonant LC tank. To achieve ZVS for all

switches, it is necessary for the inductive impedance to dominate in the LC network. This can be done by keeping the resonant frequency ( $f_r$ ) lower than the switching frequency ( $f_s$ ):

$$\omega_r < \omega_s$$

$$\omega_r = \frac{1}{\sqrt{LC}} \quad \omega_s = 2\pi f_s \tag{1}$$

Since the waveform of the input voltage  $V_{1A}$  is square, as shown in Figure 8, by using the fundamental component analysis (FCA) explained in [39], the converter’s behavior can be determined. The Fourier representation of a square wave is given by (2):

$$V_{1A} = a_0 + \sum_{n=1}^{n=\infty} [a_n \cos n\omega_0 t + b_n \sin n\omega_0 t] \tag{2}$$

So, the Fourier expansion of a square wave (2) is given in (3):

$$V_{1A} = \frac{4A}{\pi} \sin \omega_0 t + \frac{4A}{3\pi} \sin 3\omega_0 t + \frac{4A}{5\pi} \sin 5\omega_0 t + \dots \tag{3}$$

where,  $A$  is the amplitude of a square wave. The first term in the Fourier expansion becomes significant, while higher terms are filtered by the resonant tank. In this topology, due to the two capacitors (Figure 6) across the input voltage, the amplitude of the square wave becomes  $A = \frac{V_{in}}{2}$ . Therefore, the per-phase primary voltage is given by (4):

$$V_{1A} = 2 \frac{V_{in}}{\pi} \cdot \sin(\omega t)$$

$$V_{1B} = 2 \frac{V_{in}}{\pi} \cdot \sin\left(\omega t + 2\frac{\pi}{3}\right) \tag{4}$$

$$V_{1C} = 2 \frac{V_{in}}{\pi} \cdot \sin\left(\omega t - 2\frac{\pi}{3}\right)$$

The phase voltages  $V_{1A}$ ,  $V_{1B}$ , and  $V_{1C}$  are phase-shifted by  $120^\circ$ . Since we are interested in the voltage across the resonant tank, the secondary per-phase voltage referred to the primary side is given by (5):

$$V'_{2A} = \frac{2n \cdot V_o}{\pi} \sin(\omega t + \phi)$$

$$V'_{2B} = \frac{2n \cdot V_o}{\pi} \sin\left(\omega t + 2\frac{\pi}{3} + \phi\right) \tag{5}$$

$$V'_{2C} = \frac{2n \cdot V_o}{\pi} \sin\left(\omega t - 2\frac{\pi}{3} + \phi\right)$$

where  $\phi$  is a phase shift between the primary and secondary bridges and is used to regulate and control the power. This means that the phase shift between MOSFET  $S_1$  and  $Q_1$  is  $\phi$ , that between MOSFET  $S_3$  and  $Q_3$  is  $120^\circ + \phi$ , and that between MOSFET  $S_5$  and  $Q_5$  is  $240^\circ + \phi$ . In our topology, the power is controlled by varying the switching frequency ( $f_s$ ). A waveform and phasor diagram between the voltage and current is shown in Figure 9. As already mentioned,  $f_s$  is kept higher than  $f_r$ , so the LC tank current  $I_{1A}$  causes the primary bridge voltage to lag and leads to the secondary bridge, which is referred to as the primary side voltage. The LC tank’s current is given by (6).

$$I_{1A} = \frac{V_{1A} - V'_{2A}}{Z}$$

$$I_{1B} = \frac{V_{1B} - V'_{2B}}{Z} \tag{6}$$

$$I_{1C} = \frac{V_{1C} - V'_{2C}}{Z}$$



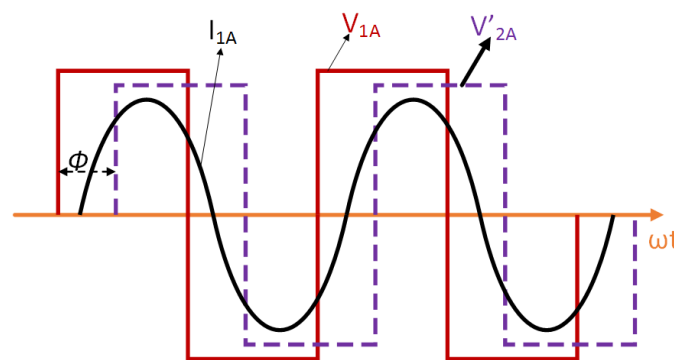
where  $Z$  is the impedance of the LC tank at  $f_s$  given by (7).

$$Z := j\left(\omega_s L - \frac{1}{\omega_s C}\right) \tag{7}$$

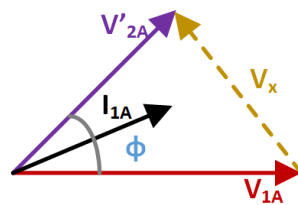
Considering that our network is a lossless phase, the voltage is balanced, and the single-phase power can be obtained from (4), (6), and (7), then by multiplying the expression by three, the average output power  $P_0$  can be obtained.

$$P_o = \frac{3}{2\pi} \left( \int_0^{2\pi} V_{1A} \cdot I_{1A} \cdot d\omega t \right) \tag{8}$$

$$P_0 = \frac{12 \cdot M \cdot V_{in}^2 \cdot C \cdot f_s - \sin(\phi)}{\pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)}$$



(a)



(b)

**Figure 9.** (a) Voltage and current waveform. (b) Voltage and current phasor.

2.2. ZVS Condition

Depending upon the frequency and voltage ratings of the 3P-DABSRC, MOSFETs were preferred over IGBTs [40]. In the proposed modulation scheme, ZVS can be achieved for all MOSFET switches. The phase A leg of the primary and secondary bridges is shown in Figure 10. The switches of primary bridge legs  $S_1, S_2$  and secondary legs  $Q_1, Q_2$  turn ON in a complementary manner. So, when  $S_1$  is going to switch ON, the phase A current  $I_{1A}$  is negative, and its direction is similar to that of  $I_{ZVS1}$ ; then, the body diode of  $S_1$  will conduct, and as a result, switch  $S_1$  will be switched ON at zero voltage. When the switch  $Q_1$  of the same leg is turned ON, at that instant, the phase current  $I_{2A}$  is positive in the direction of  $I_{ZVS1}$  and will activate the ZVS for switch  $Q_1$ . Because of the direction of the current into the secondary bridge, the ZVS conduction for the switches of the secondary bridge depends upon the current  $I_{2A}$  in a reverse manner. Soft switching depends upon the phase shift  $\phi$  and voltage gain ( $M$ ). The complete soft-switching region, hard-switching region, and boundary of the ZVS of the DAB converter using the SPS modulation scheme are plotted in Figure 11.

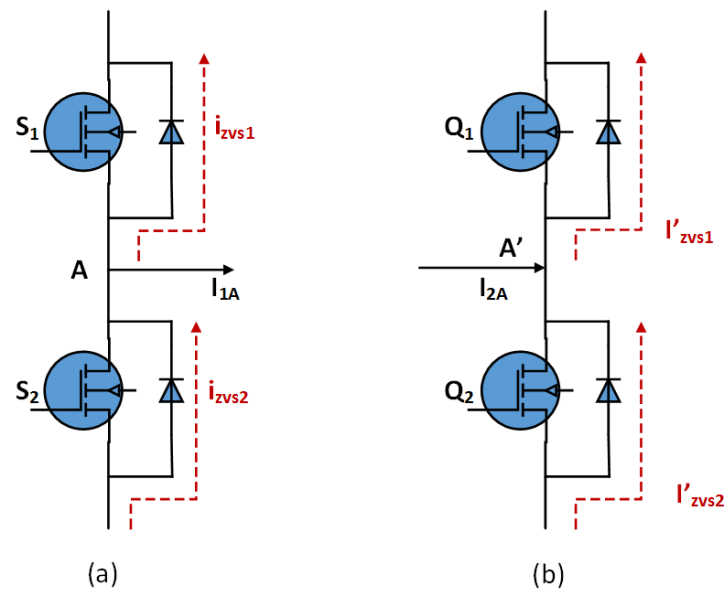


Figure 10. (a) Phase A leg of the primary bridge. (b) Phase A leg of the secondary bridge.

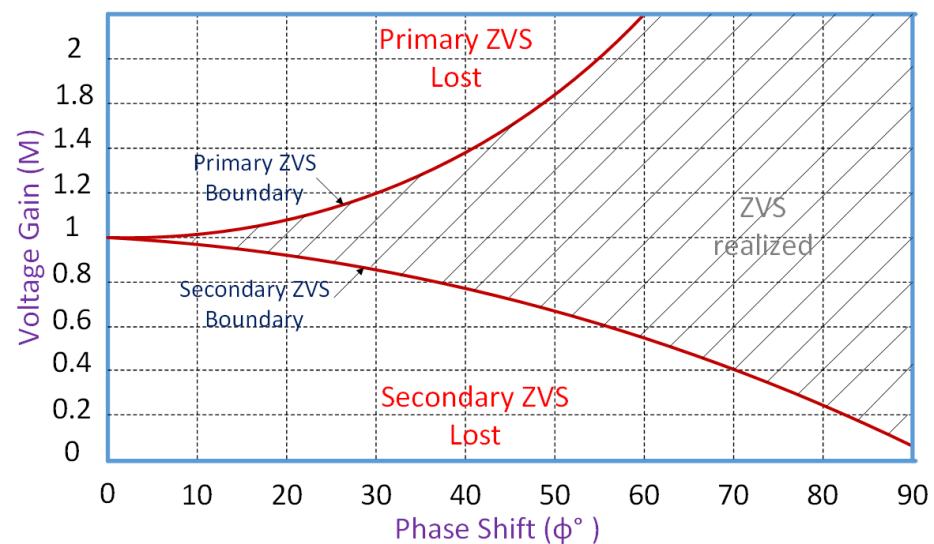
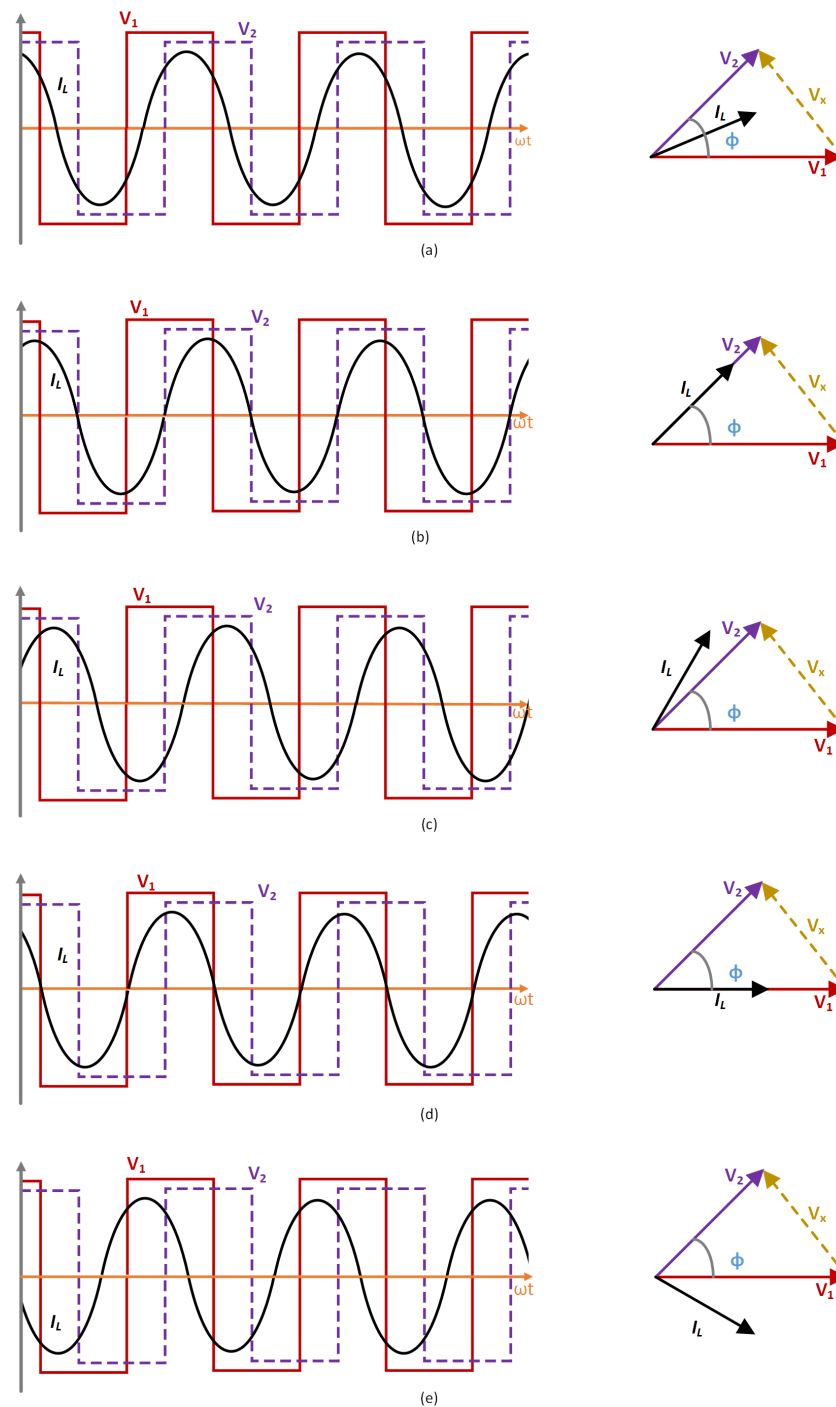


Figure 11. Soft-switching region of a DAB converter using SPS modulation.

Generally, the following are the conditions for the switches in order to obtain soft switching or hard switching, as shown in Figure 12.

- If  $\cos(\phi) < M < \frac{1}{\cos(\phi)}$ , then the inductor current ( $I_L$ ) lags behind the primary voltage ( $V_1$ ) and leads the secondary voltage ( $V_2$ ). As a result, the primary and secondary bridge switches will achieve ZVS, as shown in Figure 12a.
- If  $M = \cos(\phi)$ , then  $i_L$  lags behind  $V_1$  and becomes in phase with  $V_2$ ; the primary bridge switches achieve ZVS and the secondary bridge switches achieve ZVS under the boundary conditions, as shown in Figure 12b.
- If  $M < \cos(\phi)$ , then  $i_L$  lags behind both  $V_1$  and  $V_2$ . As a result, the primary bridge switches achieve ZVS and hard switching occurs for the secondary bridge switches, as shown in Figure 12c.
- If  $M = \frac{1}{\cos(\phi)}$ , then  $i_L$  leads  $V_2$  and becomes in phase with  $V_1$ . As a result, ZVS is achieved under boundary conditions for the switches of the primary bridge and ZVS is achieved for the switches of the secondary bridge, as shown in Figure 12d.

- If  $M > \frac{1}{\cos(\phi)}$ , then  $i_L$  leads both  $V_1$  and  $V_2$ . As a result, hard switching occurs for the primary bridge and ZVS is achieved for the secondary bridge, as shown in Figure 12e.



**Figure 12.** (a) For  $\cos(\phi) < M < \frac{1}{\cos(\phi)}$ , ZVS was achieved for the primary and secondary side switches. (b) For  $M = \cos(\phi)$ , the primary and secondary side switches achieved ZVS and ZVS under the boundary conditions, respectively. (c) For  $M < \cos(\phi)$ , the primary side switches achieved ZVS and the secondary side switches lost ZVS. (d) For  $M = \frac{1}{\cos(\phi)}$ , the primary and secondary side switches achieved ZVS under the boundary conditions and achieved ZVS, respectively. (e) For  $M > \frac{1}{\cos(\phi)}$ , the primary side switches lost ZVS and the secondary side switches achieved ZVS.

In the proposed topology, to achieve full-range soft switching, the frequency modulation technique is used. With the help of this technique, the proposed topology works

within the boundaries of ZVS over a wide range of  $M$ . The phasor and waveform diagrams of 3P-DABSRC, which show  $M < 1$ ,  $M = 1$ , and  $M > 1$ , are given in Figure 12b, Figure 12a, and Figure 12d, respectively. The optimal value of the phase shift  $\phi$  is given as follows:

$$\begin{aligned} \phi &= \cos^{-1}(M) && \text{When } M < 1 \\ \phi &= \cos^{-1}\left(\frac{1}{M}\right) && \text{When } M > 1. \end{aligned} \tag{9}$$

To keep the 3P-DABSRC converter within the boundaries of ZVS (Figure 11), the optimal value of the phase shift  $\phi$  between the primary and secondary bridges, which was selected from (9), is kept fixed and put into Equation (8). The power is then regulated by varying  $f_s$ .

The range of the switching frequency ( $f_s$ ) plays an important role in achieving ZVS in a wide operational range. The wide switching frequency range in conventional DAB converters not only increases the hard switching, but also decreases the efficiency of such converters [41]. So, it is very important to keep the frequency range at the minimum in the frequency modulation scheme. In the proposed topology, with the help of a frequency modulation scheme, ZVS is achieved in a wide operational range. From (8), the equation for  $f_s$  in the 3P-DABSRC is given in (10). The frequency range for different voltage gains in the proposed topology is shown in Figure 13.

$$f_s := \frac{\sqrt{2} \cdot \sqrt{\frac{2 \cdot \pi^4 \cdot L \cdot P_o^2 + 9 \cdot C \cdot M^2 \cdot v_{in}^4 - 9 \cdot C \cdot M^2 \cdot v_{in}^4 \cdot \cos(2 \cdot \phi)}{C} + 6 \cdot M \cdot v_{in}^2 \cdot \sin(\phi)}}{4 \cdot \pi^3 \cdot L \cdot P_o} \tag{10}$$

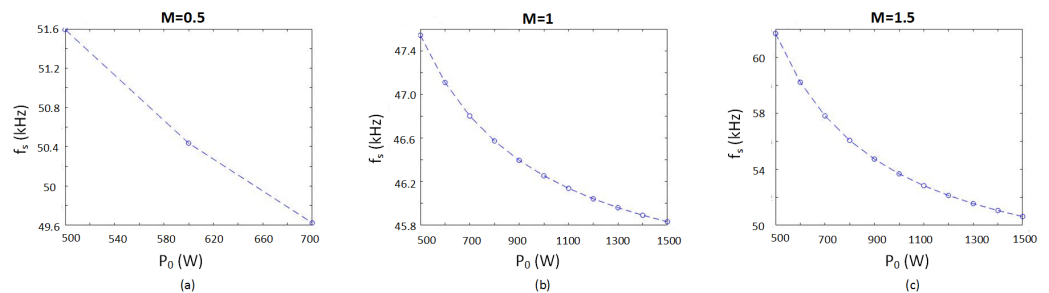


Figure 13. Frequency ranges for (a)  $M = 0.5$ , (b)  $M = 1$ , and (c)  $M = 1.5$ .

### 2.3. Minimum Tank Current Requirement

Reactive power and conduction loss play a significant role in the performance of the 3P-DABSRC converter. Figure 14 shows the reactive power and circulating current. When the converter is operated with the SPS modulation scheme, the inductor current  $I_L$  contains some fraction of the reverse current (gold-shaded area), which is known as the circulating current. It transmits power backward; as a result, reactive power (the green-shaded area) is induced. This circulating current increases the root-mean-square inductor tank current, due to which switching losses and conduction losses are increased. This circulating current and reactive power drastically increase under light load conditions or when the voltage gain deviates from unity [42].

The output current is given in (11), which is obtained from (8).

$$I_0 = \frac{12 \cdot n \cdot C \cdot M \cdot V_{in}^2 \cdot f_s \cdot \sin(\phi)}{M \cdot V_{in} \cdot \pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)} \tag{11}$$

The root-mean-square inductor tank current can be obtained with (6), which is given in (12).

$$\begin{aligned}
 I_{rms} &= \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} (I_{1A})^2 d\omega t} \\
 &= 2 \cdot \sqrt{\frac{2 \cdot c^2 \cdot v_{in}^2 \cdot f_s^2 \cdot (M^2 - 2 \cdot \cos(\phi) \cdot M + 1)}{(4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)^2}}
 \end{aligned}
 \tag{12}$$

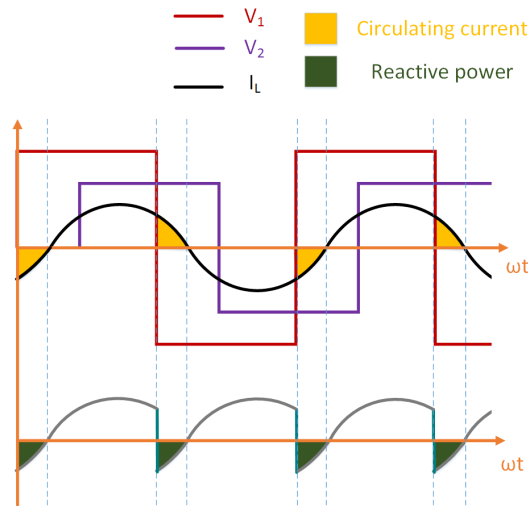


Figure 14. Reactive power and circulating current with SPS modulation.

The RMS inductor tank current is further normalized by dividing (12) by (11), as shown in (13).

$$\frac{I_{rms}}{I_o} = \frac{\pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1) \cdot \sqrt{\frac{2 \cdot C^2 \cdot V_{in}^2 \cdot f_s^2 \cdot (M^2 - 2 \cdot \cos(\phi) \cdot M + 1)}{(4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)^2}}}{6 \cdot C \cdot V_{in} \cdot f_s \cdot n \cdot \sin(\phi)}
 \tag{13}$$

In order to find the condition for the minimum tank current, the minimum value of  $\frac{I_{rms}}{I_o}$  can be obtained by taking the first derivative as equal to zero. Equation (14) gives the condition for the minimum tank current for  $M \leq 1$  and  $M > 1$ . Substituting (14) into (12) and (8) for  $M \leq 1$  and  $M > 1$ ,

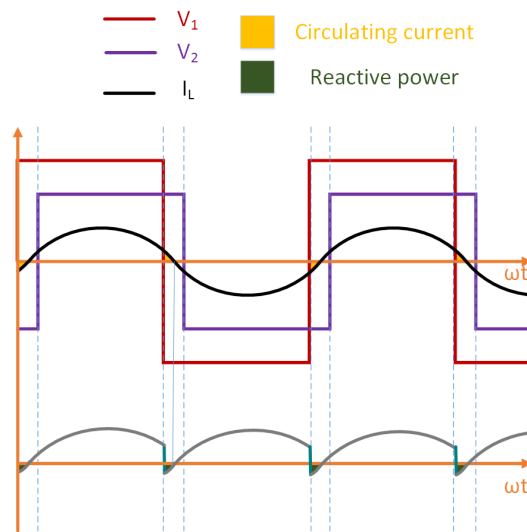
$$\frac{d}{d\phi} \left( \frac{I_{rms}}{I_o} \right) = 0 \Rightarrow \phi = \begin{cases} \cos^{-1}(M) & M \leq 1 \\ \cos^{-1}\left(\frac{1}{M}\right) & M > 1 \end{cases}
 \tag{14}$$

Hence, Equations (12) and (8) can be rewritten as (15) and (16).

$$I_o = \begin{cases} \frac{12 \cdot n \cdot C \cdot M \cdot V_{in}^2 \cdot f_s \cdot \sin[\cos^{-1}(M)]}{M \cdot V_{in} \cdot \pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)} & M \leq 1 \\ \frac{12 \cdot n \cdot C \cdot M \cdot V_{in}^2 \cdot f_s \cdot \sin[\cos^{-1}\left(\frac{1}{M}\right)]}{M \cdot V_{in} \cdot \pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)} & M > 1 \end{cases}
 \tag{15}$$

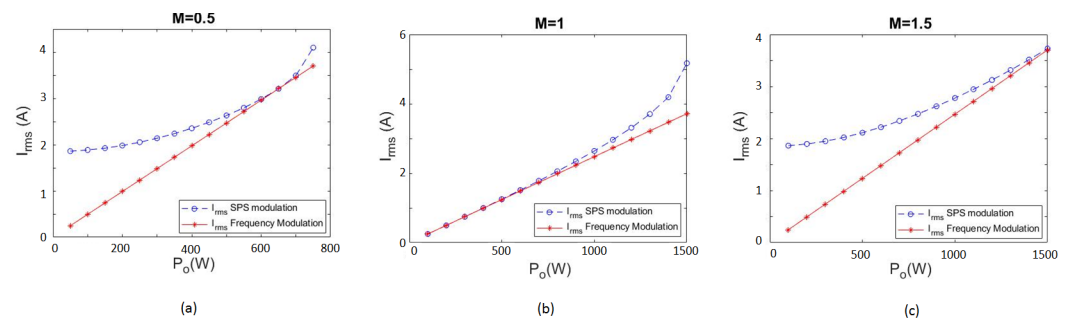
$$P_o = \begin{cases} \frac{12 \cdot M \cdot V_{in}^2 \cdot C \cdot f \cdot \sin[\cos^{-1}(M)]}{\pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)} & M \leq 1 \\ \frac{12 \cdot M \cdot V_{in}^2 \cdot C \cdot f_s \cdot \sin[\cos^{-1}\left(\frac{1}{M}\right)]}{\pi \cdot (4 \cdot \pi^2 \cdot C \cdot L \cdot f_s^2 - 1)} & M > 1 \end{cases}
 \tag{16}$$

By selecting the condition of (14), the optimal values of the output current (15) and output power (16) can be obtained. This means that the phase shift in the primary bridge will be locked, and the power will only be regulated by varying  $f_s$ . At this optimal point, the circulating current is decreased, and this reduces both the RMS current and reactive power. As a result, not only is the conduction loss decreased, but all of the switches of the 3P-DABSRC are also allowed to realize ZVS, as shown in Figure 15.



**Figure 15.** Operation waveform of the 3P-DASRC with the minimum tank current and low reactive power.

With the help of (12), for a comparison of the RMS tank currents at different voltages, the gain is plotted in Figure 16 when considering the use of the SPS modulation scheme and proposed frequency modulation scheme. It is clear from Figure 16 that the minimum tank current can be achieved by using the frequency modulation scheme. Moreover,  $I_{rms}(frequency\ modulation)$  is lower than  $I_{rms}(SPS\ modulation)$  at different voltage gains for most of the time, except at some particular loads, where they become equal. Therefore, the 3P-DABSRC with the proposed frequency modulation scheme can be used for high-power applications.



**Figure 16.** Comparison of the RMS tank currents between the SPS modulation and frequency modulation schemes for (a)  $M = 0.5$ , (b)  $M = 1$ , and (c)  $M = 1.5$ .

2.4. Power Loss Model

The power losses that are responsible for reductions in efficiency are classified as conduction loss, switching loss, and transformer core loss [43]. Switching loss occurs when MOSFETs are exposed to high voltages and currents while they are in the transition (ON–OFF) phase. Conduction loss includes the conduction losses of MOSFETS, transformers, and inductors. In this section, the losses of the 3P-DABSRC are calculated for the use of SPS modulation and the proposed frequency modulation. The efficiency of the 3P-DABSRC increases when the frequency modulation scheme is used. To understand the performance and power loss of a converter over a wide range of voltage gains, the power loss models developed in [44] are used to find the performance of the 3P-DABSRC. In this model, the conduction losses of the switches, inductor, and transformer are calculated by using

$P_{S,cond} = I_{rms}^2 R_S$ ,  $P_{L,cond} = I_{rms}^2 R_L$ , and  $P_{Tr,cond} = I_{rms}^2 R_{Tr}$ , respectively. The switching losses  $P_{MOSFET}$  are also calculated [44]. The equation for the switching loss is given in (17).

$$P_{(MOSFET)} = \frac{1}{2} \cdot 2(L_D + L_S) \cdot [n \cdot i_{inst}(t_{sw})]^2 \cdot \frac{V_{pk}}{V_{pk} - V_{in}} \tag{17}$$

where  $L_D$ ,  $L_S$ , and  $V_{pk}$  are the parasitic drain inductance, parasitic source inductance, and peak voltage, respectively.  $(n \cdot i_{inst}(t_{sw}))$  is the instantaneous MOSFET current at the switching time  $t_{sw}$ . The core loss  $P_{Core}$  is estimated by using Steinmetz’s equation [45]. The equation of the core loss is given in (18):

$$P_{core} = K_{core} \cdot (\Delta B)^\beta \cdot A_c \cdot l_m \tag{18}$$

where  $K_{core}$ ,  $\Delta B$ ,  $\beta$ , and  $A_c \cdot l_m$  are the core loss coefficient, peak AC flux density, core loss exponent, and volume of the core. The total power loss and efficiency ( $\eta$ ) of the 3P-DABSRC illustrated by (19) and (20), respectively.

$$P_{Loss} = P_{S,cond} + P_{L,cond} + P_{Tr,cond} + P_{MOSFET} + P_{Core} \tag{19}$$

$$\eta = \frac{P_0}{P_0 + P_{Loss}} \times 100\% \tag{20}$$

$P_{Loss}$  (from (19)) and  $\eta$  (from (20)) are calculated by using the SPS modulation and proposed frequency modulation schemes at different voltage gains and are plotted in Figures 17 and 18, respectively. Figure 17a–c plot  $P_{Loss}$  versus the output power for  $M = 0.5, 1, \text{ and } 1.5$ , respectively. Figure 18a–c plot  $\eta$  versus the output power for  $M = 0.5, 1, \text{ and } 1.5$ , respectively.

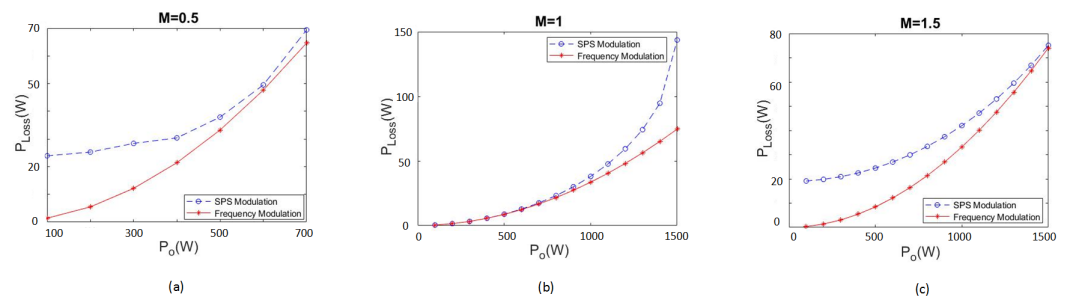


Figure 17. Comparison of the power losses between the SPS modulation and frequency modulation schemes for (a)  $M = 0.5$ , (b)  $M = 1$ , and (c)  $M = 1.5$ .

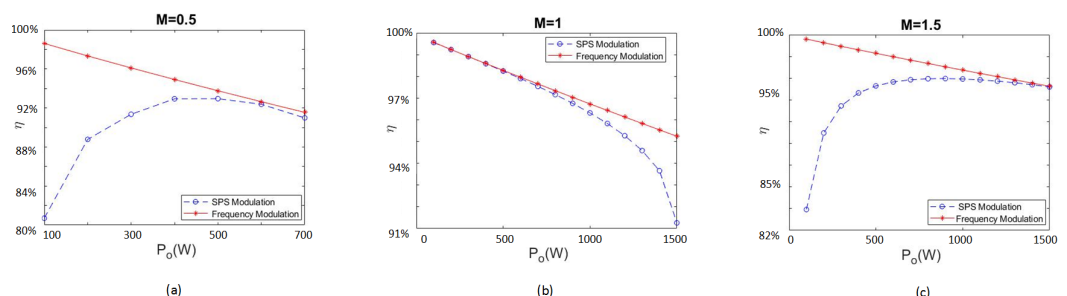


Figure 18. Comparison of the efficiencies between the SPS modulation and frequency modulation schemes for (a)  $M = 0.5$ , (b)  $M = 1$ , and (c)  $M = 1.5$ .

It is clear from Figure 17a,b that  $P_{Loss}(SPSmodulation)$  is always greater than  $P_{Loss}(frequencymodulation)$ , except at a particular load, where these losses become equal. Furthermore, if we analyze Figure 18a,b, the efficiency  $\eta$  of frequency modulation always dominates that of the SPS modulation scheme. It is noted that by using the frequency modulation scheme in the 3P-DABSRC, at a low output power  $P_o$ , the efficiency  $\eta$  becomes

close to 100% due to the low tank current  $I_{rms}(frequency\ modulation)$  and the low power loss  $P_{Loss}(frequency\ modulation)$ , as shown in Figures 16 and 17, respectively. The ranges in which the frequency modulation technique is more efficient are from 50 to 51 kHz for  $M = 0.5$ , 45 to 47 kHz for  $M = 1$ , and 45 to 50 kHz for  $M = 1.5$ .

2.5. Simulation Results and Discussion

The proposed 3P-DABSRC topology was simulated in PSIM. The specifications of the 3P-DABSRC are given in Table 1. The simulation results for different output powers (i.e., 25%, 50%, and 100% rated power) at different voltage gains (i.e.,  $M = 0.5, 1$ , and 1.5) while using conventional SPS modulation and the proposed frequency modulation scheme are shown in Figures 19–21. In Figure 19, the SPS modulation scheme is used. The primary bridge switches achieved soft switching, while the secondary bridge switches operated in the hard-switching mode. In Figure 19c, the SPS modulation scheme was used. The primary and secondary bridge switches achieved soft switching. In Figure 19b,d, the frequency modulation scheme was used. The primary and secondary bridge switches achieved soft switching. In Figure 20a–f, the primary and secondary bridge switches achieved soft switching while using the SPS and frequency modulation schemes. In Figure 21a,c, the SPS modulation scheme was used. The secondary bridge switches achieved soft switching and the primary bridge switches operated in the hard-switching mode. In Figure 21e, the SPS modulation scheme was used. The primary and secondary bridge switches achieved soft switching. In Figure 21b,d,f, the frequency modulation scheme was used. The primary and secondary bridge switches achieved soft switching. As mentioned earlier, the proposed frequency modulation scheme not only helps us to achieve the full ZVS range, but also reduces the tank current due to the decreased conduction loss.

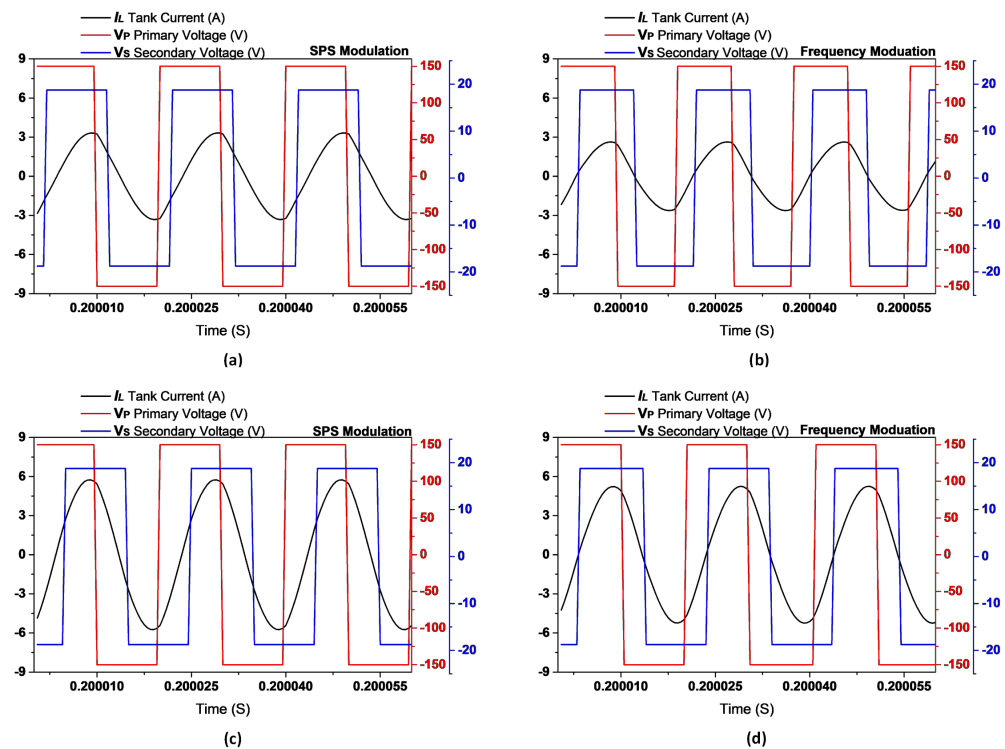
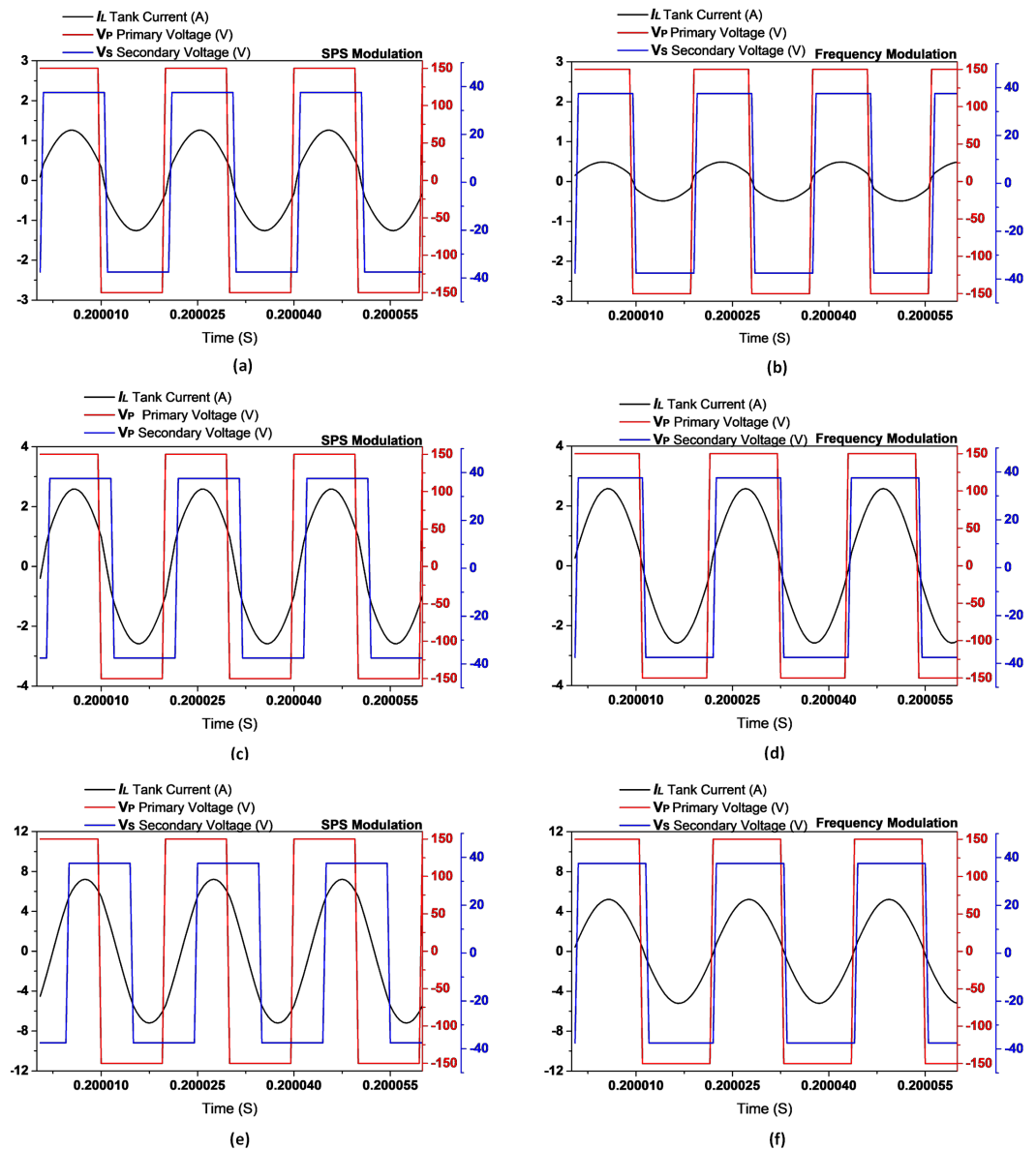


Figure 19. Simulated waveform at a voltage gain of  $M = 0.5$ : (a) 25% rated power using SPS modulation; (b) 25% rated power using frequency modulation; (c) 50% rated power using SPS modulation; (d) 50% rated power using frequency modulation.

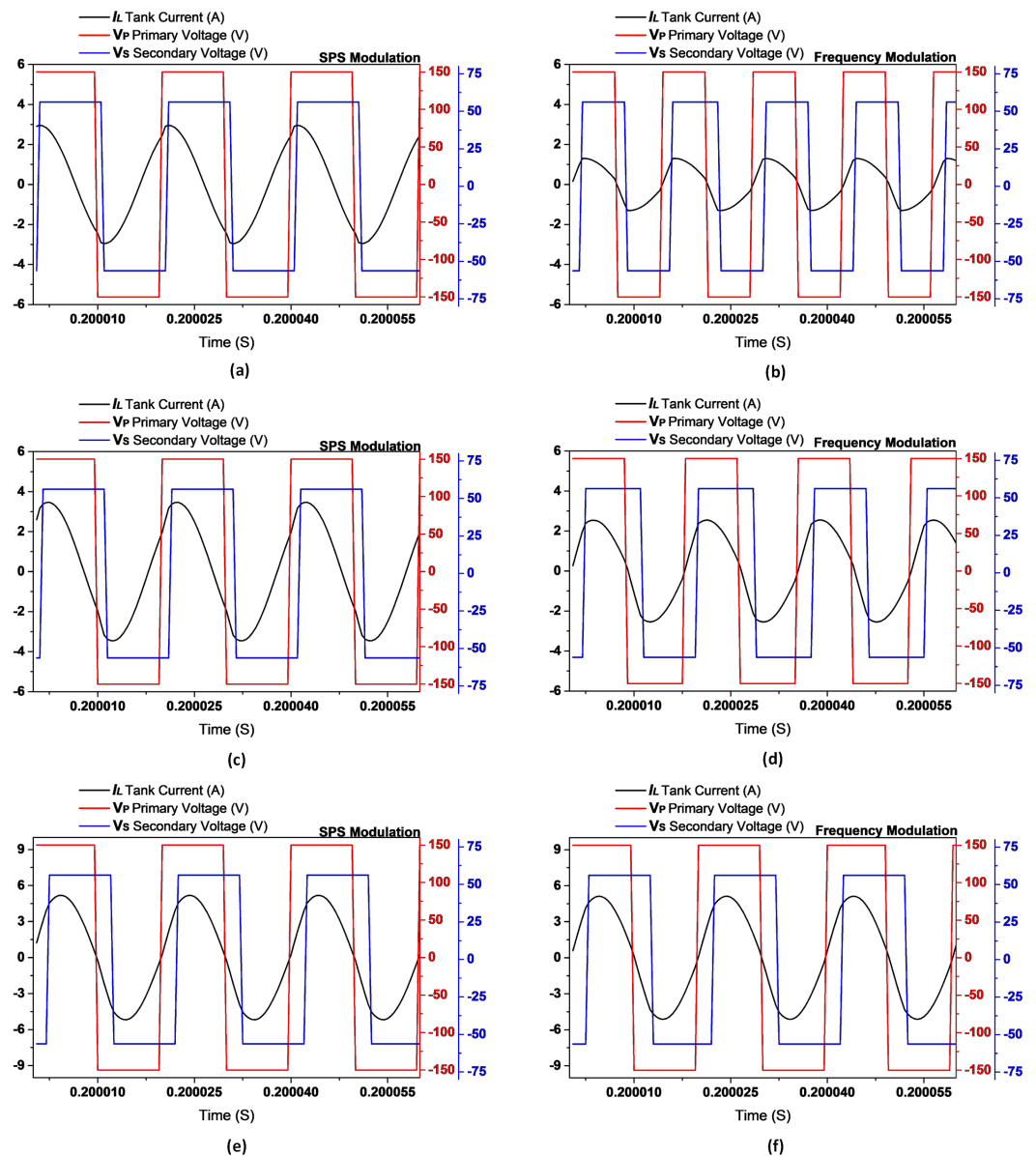




**Figure 20.** Simulated waveform at a voltage gain of  $M = 1$ : (a) 25% rated power using SPS modulation; (b) 25% rated power using frequency modulation; (c) 50% rated power using SPS modulation; (d) 50% rated power using frequency modulation; (e) 100% rated power using SPS modulation; (f) 100% rated power using frequency modulation.

**Table 1.** Specifications of the 3P-DABSRC.

Parameter	Symbol	Value
Input voltage	V1	300 Vdc
Output voltage	V2	37.5–112.5 Vdc
Maximum power	Pmax	1500 W
Switching frequency	$f_s$	45–63 kHz
Resonant frequency	$f_r$	45 kHz
Phase-shift range	$\phi$	0–90 degree
Inductor	L	610.8 $\mu$ H
Capacitor	C	20.48 nF
Transformer (Core ETD 49)	Turns ratio n	4
MOSFET	SPW47N60CFD	600 V, 46 A



**Figure 21.** Simulated waveform at a voltage gain of  $M = 1.5$ : (a) 25% rated power using SPS modulation; (b) 25% rated power using frequency modulation; (c) 50% rated power using SPS modulation; (d) 50% rated power using frequency modulation; (e) 100% rated power using SPS modulation; (f) 100% rated power using frequency modulation.

2.6. Conclusions

Due to hard switching and a high circulating current, when operated with SPS modulation at high frequencies, DAB converters endure significant switching and conduction losses. This paper presented a modified 3P-DABSRC. Due to its three-phase current-sharing capabilities, this converter can be used in high-power applications with very little ripple at the DC output port. The proposed converter is operated with SPS and frequency modulation schemes. It is clear from the simulation results that when the SPS modulation scheme is used, the 3P-DABSRC converter experiences hard switching and a high circulating current, but when this converter is operated with a high-frequency modulation scheme, all switches achieve soft switching over a wide range of voltage gains. Furthermore, with the frequency control modulation scheme, the converter works with minimal tank current, which, in turn, reduces the conduction losses.

The advantages and utility of the proposed model were demonstrated through mathematical modeling and simulation. We will extend this work with experimentation.

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