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Review

Active Power-Decoupling Methods for Photovoltaic-Connected Applications: An Overview

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Abstract: This study compares ripple port, stacked switched capacitor, and capacitive energy storage architectures for active power decoupling, comparing the number of components, performance, energy density, DC-link capacitor reduction, efficiency, and frequency operation to highlight their main benefits and drawbacks for single-phase grid-connected applications. The overview reveals equivalent effective energy density without electrolytic capacitors, as well as enhanced simplicity, performance, and durability, thereby providing stacked switched capacitors as an attractive power-decoupling alternative for multi-stage connected applications, based on the principle that its individual buffer capacitors absorb and deliver energy without tightly constraining their individual terminal voltages, while maintaining a narrow range voltage at the buffer DC port.

Keywords: power decoupling; stacked switched capacitor; voltage capacitor active power decoupling; ripple-port

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1. Introduction

Single-phase inverters must balance AC and DC power for buffering (P_{Buffer}) [1]. Based on the application [2–5], the input power (P_{DC}) must comply with a small and constant ripple, while the output power ($P_{AC}(t)$) varies sinusoidally at a twice-line frequency between zero and twice its average value ($P_{Avg}(t)$) [6]. As Equation (1) shows, a robust element(s) is needed to process the excess energy and optimize energy use.

$$P_{Buffer}(t) = P_{DC} - P_{AC}(t) = P_{DC}\cos(2\omega_{grid}t) \quad (1)$$

where ω_{grid} denotes the angular frequency of the line and t the time.

The power pulsation in Equation (1) affects the lifetime of the system, produces large passive components, degrades waveform qualities, reduces the performance, and can deteriorate the maximum power point tracking (MPPT) [7,8]. Consequently, electrolytic capacitors are typically used to store excess energy owing to their high energy density and low cost [9]. However, the use of electrolytic capacitors results in poor energy utilization, short lifetimes, temperature constraints, and an increase in volume [10]. Hence, the development of new decoupling arrangements is important for future grid-connected systems, whose principal characteristics are small size, high energy density, and high reliability [11].

To clarify the earlier physics phenomenon, a conventional grid-connected scheme is shown in Figure 1, where a multi-stage photovoltaic (PV)-connected application is represented [12]. This PV-connected application generally comprises five power stages, in which the use of an electrolytic capacitor (C_c) to decouple the DC and AC sides is expected, but produces high power loss, low reliability, and short lifetime.

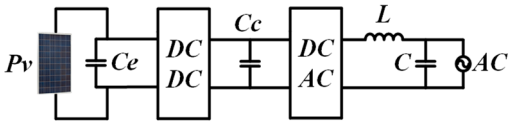

Figure 1. Conventional scheme used for multi-stage PV-connected applications [12].

In Figure 1, the first stage (C_e) allows low-frequency ripples. In the second stage, according to the inverter specification, the voltage level from the PV is increased (DC-DC). The third and fourth stages represent the inverter (DC-AC) and LC filter, respectively, which must shape the current into a sinusoidal waveform; if the PV array voltage is lower than the grid network voltage, the PV array voltage must be boosted with an additional element. Finally, the fifth stage filtered the sinusoidal signal using a second-order *LC* filter.

According to the component characteristics in the third stage, many alternative solutions have been proposed to avoid the use of a bulky and low-reliability device [13–17]. Some of these solutions have been classified into two principal groups [18–26]: passive and active power-decoupling methods (PPD and APD, respectively). The former methods commonly apply an *LC* filter or bulky passive components (inductor or capacitor), while the latter provides many attractive features, such as a relatively small size and high reliability, because it stores the ripple power in another component by adding an extra switching circuit.

From this classification, one interesting PPD method for eliminating the use of electrolytic capacitors is the current source converter (CSC) [27,28]. The CSC has as principal advantages a continuous input current and high voltage gain, making it an interesting option for a single-phase connected application. However, CSCs present some drawbacks, such as the need for a large and bulky inductor, low efficiency, complex control, and poor power density.

Similar to the CSC, the passive *LC* branch for bypassing the power decoupling [29] represents another PPD method, which generates an AC current that compensates for the twice-line frequency ripple. However, the resonant circuit is sensitive to voltage distortion in the grid network, and the voltage across the capacitor of the *LC* circuit can be significantly higher than the maximum DC-link voltage. It also presents high oscillations, adds more weight and size to the system, and is still not cost-effective owing to the low-frequency *LC* circuit.

Different to the PPD method, the APD applies an extra switching circuit to store the energy [30,31]. One alternative to this method is the use of bidirectional DC-DC converters to effectively utilize film capacitors while maintaining the desired narrow-range bus voltage [32]. However, owing to the power losses in the DC-DC converter, these solutions present low buffering efficiency if high power density needs to be maintained.

Another APD method involves injecting a second or fourth harmonic into the circulating current to balance the grid power at higher frequencies [33], aiming to apply small capacitors because a large voltage ripple across the decoupling component can be applied. However, these methods are not entirely convenient for grid-network-connected PV applications because they are preferable for motor drives, wind turbines, and LED applications at low frequencies and modulation indices [34,35]. In addition, these techniques are generally used by adding an extra DC-DC bidirectional converter; the smaller the capacitor, the greater the stress on power semiconductor devices, which results in increased losses when a high power density is to be maintained, and consequently, lower efficiency is achieved.

Other APD solutions have been proposed based on boost-buck and buck-boost inverters [36,37]. These works are generally aimed at achieving low AC distortion, small volume, and high efficiency. However, they do not entirely represent the stability of current injection into the utility grid network.

The use of current control in parallel with a decoupling capacitor is another APD solution [38]. This active technique controls and reduces the amount of current drawn from the capacitor, thereby effectively reducing the need for energy damping [39–43]. However,

the voltage across the switches is very high because the switches can be exposed to voltages as high as the DC link, increasing the switching losses of power semiconductor devices.

Similar to the previously mentioned topologies, the flyback-type inverter is another topology to permit small-volume, lightweight, and stable AC current injection into the utility grid network [44,45]. This type of solution almost removes low-frequency power pulsation, with the aim of using small capacitors. However, their efficiency is significantly affected by high power losses in power semiconductor devices. In addition, its use is suggested in low-power applications.

In contrast to earlier methods, alternative active filter configurations were introduced in the form of stacked switched capacitors (SSCs) [46,47], voltage capacitor active power decoupling (VCAPD) [48], and ripple-port module-integrated inverters (RP-MIIs) [49]. The first presents a bipolar or unipolar architecture to replace the electrolytic capacitor, the second one stores the power ripple on the capacitor, while the last applies a third port on the DC link for ripple cancellation purposes, which is added to the converter, and handles approximately one-third of the total energy in the system. These techniques maintain comparable effective energy densities, require a very small DC-link capacitance, and can be applied in any isolated boosting DC-DC converter.

In a brief review, one of the principal drawbacks of the PPD method is the need to apply almost infinite values of passive components to become approximately constant voltage and current at the DC-link, causing a large volume and weight in the entire system. In contrast, the APD solution permits an increase of approximately 50% in the power density, thereby providing these methods as attractive solutions to decouple the twice-line frequency ripple.

In this regard, the main contribution of this study is to provide a comprehensive review of APD methods, mainly referring to the solutions presented for SSC, RP-MII, and VCAPD in single-phase, multi-stage, isolated PV-connected applications, by comparing the number of components, performance, energy density, reduction of decoupling components, efficiency, and frequency operation. The present study differs from different works introduced earlier, such as the one presented in [50], where its main contribution is focused on control strategies in APD, or [51], where it focuses on the evolution of control algorithms in power system support functions, such as voltage and frequency regulation, while also offering an overview of power system support functions derived from renewable distributed energy resources (DERs). In addition, this study differs from some reported techniques focused on the AC side, such as parallel power factor corrections (PFCs), DC-bus conditioners, AC-side active filters, and two-stage cascaded PFC, because all these methods are applied to solve the second-order harmonic current issue presented in single-phase pulse-width modulation rectifiers [52].

The remainder of this paper is organized as follows. Section 2 describes the operational principles of SSC, RP-MII, and VCAPD methods. Section 3 presents a general overview of the selected APD methods by comparing the number of components, performance, energy density, reduction of the decoupling element, efficiency, and frequency of operation. Section 4 provides a discussion and comparison. Finally, Section 5 concludes the paper.

2. The Principal Operation of the SSC, RP-MII, and VCAPD Methods

2.1. SSC Architectures

The use of SSC architectures, which reconfigure capacitors between parallel and series combinations to decouple power energy, results in an interesting alternative for improving energy utilization [53]. This method adds a switching circuit that includes a block of capacitors and switches to eliminate the use of electrolytic capacitors.

In this regard, the energy buffer, by applying SSC configurations, works on the principle that each capacitor absorbs and delivers energy, maintaining a narrow range of voltage at the buffer port, allowing maximum utilization of the energy storage capability [54]. Another approach to increasing the energy density is to optimize the capacitance ratio of the capacitors used in the energy buffer [55,56].

There are two blocks within these architectures: the backbone and supporting capacitors. The first buffers most of the total energy utilized, and the second provides voltage support, maintaining the total bus voltage in the desired range (Figure 2). In addition, the backbone capacitors have components that reflect the performance of the DC-link capacitor as if it was just one component, while the supporting capacitors included components that helped to maintain the voltage level in the principal block, allowing the preservation of the necessary energy to the load.

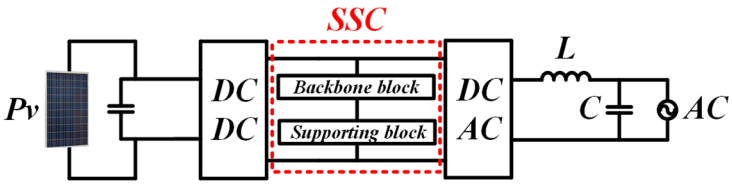

Figure 2. Basic scheme by applying an SSC architecture.

In Figure 2, the decoupling circuit is presented with two systems of general architecture: unipolar (Figure 3a) and bipolar (Figure 3b) [57,58]. The former is suggested in low-power applications and is composed of series-connected support, backbone blocks of switches (S_1, S_2, and S_m), and capacitors (C_1, C_2, and C_m). The latter provides a support block comprising an H-bridge (S_{H1}, S_{H2}, and S_{H3}, S_{H4}), switches (S_2, S_{2m}), and capacitors (C_{2b}, C_{2mb}) in combination with backbone capacitors (C_{1b}, C_{mb}) and switches (S_1, S_m). This architecture is suggested for high-power applications and has a principal characteristic that it can be applied to as many capacitors and switches as required.

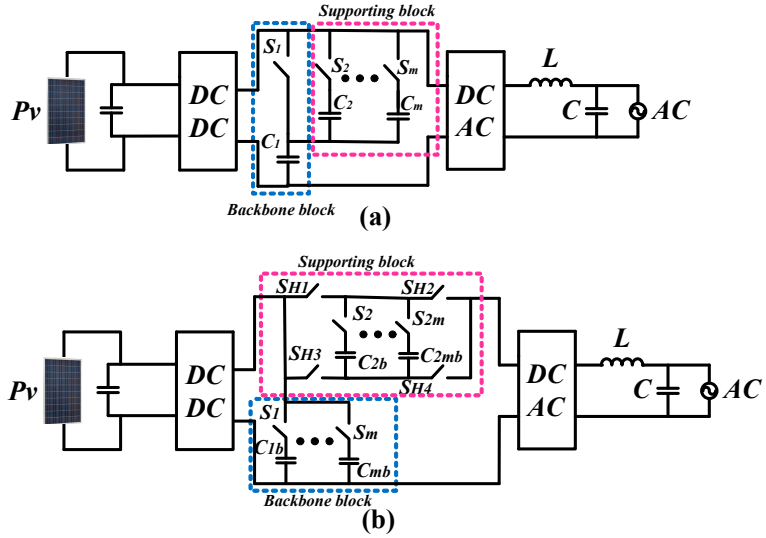

Figure 3. SSC architectures: (**a**) unipolar; (**b**) bipolar [57,58].

The unipolar scheme shown in Figure 3a, consists of one backbone capacitor (C_1), m supporting capacitors (C_2, and C_m), and $m + 1$ supporting switches (S_1, S_2, and S_m). This architecture is called the 1-m enhanced unipolar design, in which conventionally all capacitors present the same value of capacitance, but different voltage ratings. For this architecture, once the buffer starts, S_1 is turned on, while the rest of the switches are turned off, charging the backbone capacitor C_1 until a specific bus voltage. When this voltage is reached, S_1 is turned-off and S_2 turned on, allowing the charge of the supporting capacitor C_2; this process continues until the rest of the supporting capacitors are charged and discharged during a complete period (the switches are turned on and off in reverse order during the discharging cycle).

According to the literature, for a *1-m* unipolar architecture, the energy buffering ratio (Γ_b) can be defined as

$$\Gamma_b = \frac{C_1((1+{R_v}^2)-(1-m{R_v}^2))+(mR_v)^2}{C_1(1+R_v)^2+C_2(1+2^2+3^2+\ldots+m^2){R_v}^2} \quad (2)$$

where R_v is the bus voltage ripple ratio, defined as

$$R_v = \frac{V_{\max}-V_{\min}}{2\cdot V_{nom}} \quad (3)$$

In Equation (3), the maximum, minimum, and nominal voltage values are represented by V_{max}, V_{min}, and V_{nom}.

The architecture in Figure 3b, presents a scheme comprising n backbone capacitors (C_{1b}, C_{mb}), m supporting capacitors (C_{2b}, C_{2mb}), and switches ($n + m + 4$ switches). This architecture is called an *n-m* enhanced bipolar design, in which all capacitors have equal capacitance, but different voltage ratings. This architecture permits an increase in the energy buffering ratio because it provides an energy buffering capability of 71.1% of the total peak energy storage [59]. For this architecture, C_{1b} can be increased to C_{mb} backbone capacitors as needed, as well as the supporting capacitors from C_{2b} to C_{2mb}.

An interesting point to note is the fact that for the bipolar architecture, the values of the backbone and supporting capacitors are the same, but with different voltage ratings; however, the supporting capacitors are put into an h-bridge to enable bi-directional charging.

According to the efficient charging and discharging process of the capacitors shown in Figure 3, the energy density can be increased. Further, the voltage ratings in all capacitors can be optimized. This point is critical because the voltage rating depends exclusively on the V_{nom} of the bus voltage (V_{bus}).

On the other hand, the capacitors for both versions of architecture must be pre-charged through a specific sequence, so that at the beginning of the discharge cycle, all the capacitors are charged to their maximum level, the first to discharge being the backbone capacitor. Once the voltage on the DC-link ($V_{DC\text{-}link}$) reaches its minimum allowed value, the supporting capacitors are charged/discharged one by one in each transition, so that the capacitors that were used in the previous cycle can be loaded independently. Figure 4 shows an example of unipolar architecture according to a charged and discharged cycle, where the supporting capacitors (C_2, C_3, and C_4) are added one by one to the backbone capacitor (C_1) to obtain the desired behavior for energy damping.

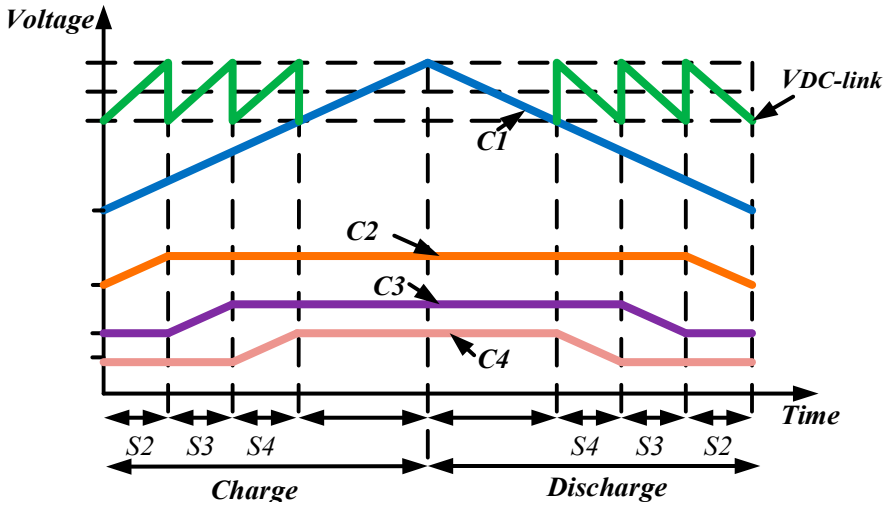

Figure 4. States of commutation of unipolar SSC [60].

A key point to achieve high efficiency in SSC architecture is to define correctly the commutations shown in Figure 4 (for S_2, S_3, and S_4). The efficiency of the SSC system across a full operating range can be especially high because the grid network only operates at very low switching frequencies, reducing losses.

2.2. Capacitive Energy Storage for Ripple Power Compensation

As an alternative to SSC architecture, power decoupling based on capacitive energy storage consists of a storage capacitor (*Cdc*), a full H-bridge (*T1*, *T2*, *T3*, and *T4*), and an additional third leg (*T5*, and *T6*), which is composed of an energy storage variable capacitor (*Ccx*) and a smoothing inductor (*Lc*), as shown in Figure 3a of the study published in [61], where the inductor L_c is used to absorb the high switching frequency ripple, and L_a, L_b, which are utilized to filter the input signal.

The reference voltage for the capacitor C_{cx} is a sinusoidal waveform operating at a similar frequency to the AC source (V_s). As the operating frequency is low, this method can achieve a good power decoupling performance at low switching frequencies. The processed energy C_{cx} is controlled by the additional phase leg to absorb the 2ω ripple. Thus, C_{cx} can be fully charged to V_s and discharged to its voltage $-V_s$; as a result, this approach only requires a minimum DC capacitor and a minimum AC capacitor to implement its function.

The VCAPD control system consists of an inner loop control and an outer loop proportional resonant control.

The control system first suppresses the high resonance peak, and then it uses a proportional resonant controller on the outer layer to achieve steady-state precision. The capacitor voltage reference is modified through the closed-loop control. The main idea is to compensate the ripple power based on the control of the capacitor voltage or capacitor current.

From Figure 3a in [61], the reference voltage for the capacitor (V_{cx}) is a sinusoidal wave with the same frequency as the V_s. On the other hand, due to the use of a capacitor as an energy storage component, the electrical efficiency is higher than using inductors. Moreover, the current stresses of the rectifier legs (i_a, i_b, and i_c) do not increase.

The first step of parameter design for the VCAPD method is to choose an appropriate *LC* resonant frequency. Apart from setting the upper limit of the system bandwidth and directly determining the cancelation of two coefficients, it has an impact on many other variables. It is important to note that the total capacitance can be reduced by almost five times.

To verify the performance of the VCAPD method, there are some reported works. For example, Figure 9 of the study published in [62] shows the simulation results of the PWM rectifier, where v_a, v_b, and v_c are the phase voltages; v_{cac} is the voltage in the storage capacitor (c_{ac}); V_s is the input voltage; i_s is the input current; i_{cac} is the current in c_{ac}; and v_{dc} is the voltage in the output capacitor.

On the other hand, the literature also shows that some of the principal advantages of applying the VCAPD method are high efficiency compared to inductance energy storage, a low requirement for switching frequency/control bandwidth, full utilization of the energy storage capability, and no excessive current stresses for the power devices [63]. Therefore, this method can increase the life expectancy of a power supply.

Compared with the *LC* resonance filters tuned at twice the grid frequency, the passive components in the VCAPD circuit are also greatly reduced. Furthermore, the voltage rating of the capacitor is lower than in passive *LC* filters. To enhance the power decoupling performance, a closed-loop modification of the capacitor voltage reference based on the residual ripple voltage is carried out.

2.3. RP-MII

To demonstrate the analysis of the RP-MII, a conventional single-phase grid-connected structure is shown in Figure 5 [64].

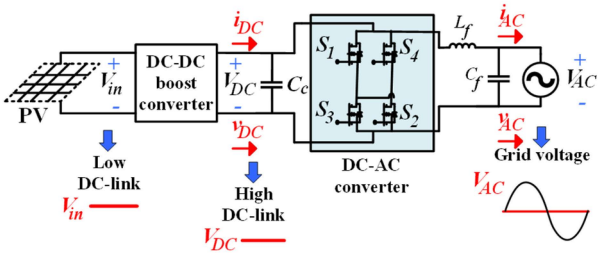

Figure 5. Single-phase grid-connected scheme [64].

In Figure 5, V_{in} is the input voltage; C_c is the decoupling capacitor; i_{DC} and v_{DC} are the current and voltage, respectively, across C_c, and L_f, C_f, which are utilized as filter steps.

From Figure 5, the current (i_{AC}) and voltage (V_{AC}) that fluctuate in the grid network can be determined as

$$V_{AC}(t) = V_{DC}cos(\omega t) \tag{4}$$

$$i_{AC}(t) = I_{DC}cos(\omega t - \alpha) \tag{5}$$

where V_{DC} and I_{DC} are the DC-link voltage and current, respectively; ω is the angular frequency ($2\pi f_{grid}$); f_{grid} is the grid frequency (60 Hz); and α is the angle between the AC voltage and the current.

Since the AC-side power fluctuation is the product of V_{AC} and i_{AC}, the AC power (P_{AC}) can be calculated as

$$P_{AC} = V_{AC}i_{AC} \tag{6}$$

From the previous equation, by applying the trigonometric identity in Equation (7), P_{AC} is defined as shown in Equation (8).

$$\cos^2(\omega t) = \frac{1 + \cos(2\omega t)}{2} \tag{7}$$

$$P_{AC} = \frac{1}{2}\left[\underbrace{V_{DC} \cdot I_{DC} \cdot \cos(2\omega t + \alpha)}_{(1)} + \underbrace{V_{DC} \cdot I_{DC} \cdot \cos(\alpha)}_{(2)}\right] \tag{8}$$

From Equation (8), term 1 represents the power ripple (P_{rip}), which causes a voltage variation in the DC-link that is reflected at the PV terminals (in this example), causing an efficiency reduction. When P_{AC} is greater than the power in the DC-link (P_{DC}), the difference in P_{rip} is absorbed by the power decoupling component. Alternatively, when P_{AC} is less than P_{DC}, the decoupling component must deliver the stored power to compensate P_{AC} and ensure energy conservation.

Term 1 from Equation (6) is crucial to demonstrate the power decoupling strategy by applying an RP-MII scheme. This configuration is shown in Figure 6 [64].

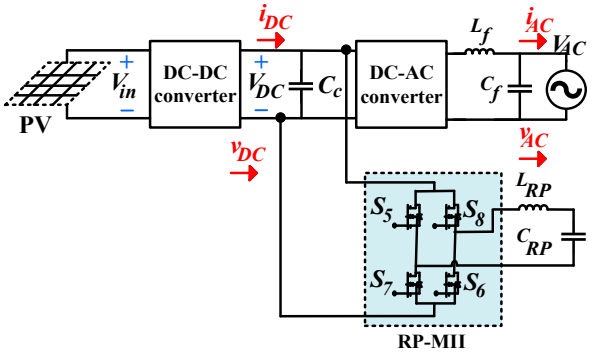

Figure 6. Single-phase grid-connected structure by applying an RP-MII [64].

The scheme in Figure 6 presents a single-phase connected system that applies a RP-MII as a power decoupling method. This system is made up of a magnetically isolated DC–DC converter (to adjust the voltage level provided by the PV), an inverter, and a ripple port that is responsible for mitigating power fluctuation.

Power decoupling through an RP-MII consists of adding a circuit comprising a full H-bridge inverter (S_5, S_6, and S_7, S_8) and a second-order arrangement made up of L_{RP} and C_{RP}. From this arrangement, L_{RP} is used to prevent any sudden voltage changes, while C_{RP} is used to serve as a support component for C_c, avoiding a high-voltage ripple on the DC-link.

Similar to the scheme shown above, it is expected that the DC port provides a nominal power value that, for practical purposes, is as close as possible to the average value of the power demanded by the load. However, as this condition never occurs, the power managed by the ripple port is essential for energy conservation.

Therefore, the main function of the RP-MII is to process the P_{DC}, which means that the total power in the RP-MII (P_{RP}) can be approximated as the sum of the average power in L_{RP} (P_{LRP}) and C_{RP} (P_{CRP}), as follows.

$$P_{RP} = P_{LRP}(t) + P_{CRP}(t) \tag{9}$$

From Equation (9), since the current through L_{RP} and C_{RP} is the same, P_{RP} can be expressed as

$$P_{RP}(t) = -C_{RP} \cdot V_{CRP} \cdot \omega \cdot \sin(\omega t + \alpha) \cdot (V_{CRP}(t)) - C_{RP} \cdot V_{CRP} \cdot \omega \cdot \sin(\omega t + \alpha) \cdot (V_{CRP}(t)) \tag{10}$$

where V_{CRP} is the voltage across C_{RP}, and by applying the trigonometric identity in Equation (11), it is possible to reduce Equation (10), as shown in Equation (12).

$$(\sin(2\alpha) = 2 \cdot \sin(\alpha) \cdot \cos(\alpha)) \tag{11}$$

$$P_{RP}(t) = \frac{-{V_{CRP}}^2 \cdot C_{RP} \cdot \omega(1 - \omega^2 \cdot L_{RP} \cdot C_{RP})}{2 \cdot \sin(2(\omega t + \alpha))} \tag{12}$$

From Equation (12), it is possible to determine C_{RP}. This value is shown in Equation (13).

$$C_{CRP}(t) = -\sqrt{\frac{{V_{CRP}}^2 - 8P_{DC}\omega \cdot L_{RP}}{4 \cdot \omega^4 \cdot {L_{RP}}^2 \cdot {V_{CRP}}^2}} + \frac{1}{2\omega^2 \cdot L_{Rp}} \tag{13}$$

The scheme shown in Figure 6, is based on adding a port that processes only the minimum value of energy required. Therefore, due to the benefits offered by this topology, it is necessary to carry out an analysis that obtains the performance values that define its operation, advantages, and drawbacks. Therefore, Section 3 presents a comprehensive review focused on SSC architecture, the VCAPD method, and RP-MII as power decoupling strategies.

3. Overview

3.1. SSC as an APD Method

SSC architecture can achieve greater energy efficiency and a substantial reduction in the decoupling capacitor thanks to the effective use of stored energy. In this meaning, the energy buffering ratio (EBR) represents the total energy extracted from the buffer, while a higher EBR lowers the energy storage requirement, allowing a considerable reduction in passive volume. This means that the EBR is a key parameter for the verification of the optimal performance of the energy buffer.

A bipolar SSC architecture that analyzes part of these characteristics is [65], and it is essentially introduced to solve low efficiency in high power (2 kW) as a result of the control strategy applied. Its principal contribution is a variable-frequency, constant, peak current

control strategy, which permits a performance of 90% of efficiency by applying power semiconductor devices based on silicon carbide (SiC). This scheme is shown in Figure 3 of the study published in [65].

The scheme in Figure 3 from [65] presents a bipolar energy buffer architecture comprising a supporting block (C_{21}, C_{22}, C_{23}, C_{2m} with S_{21}, S_{22}, S_{23}, S_{2m} as switches, respectively, and a full bridge S_{H1}, S_{H2}, S_{H3}, and S_{H4}), a backbone block (C_{11}, C_{12}, C_{1n} with S_{11}, S_{12}, S_{1n} as switches, respectively) that pre-charges all the capacitors at the beginning of the switching period, a DC–AC inverter, and a filter stage.

This topology performs the SSC arrangement across the DC input bus, and one of the principal characteristics is the performance provided by its control strategy. This control permits the commute of part of the DC–AC converter at a high frequency to shape an output current, while the rest of the converter commutes at line frequency. This characteristic allows an optimal choice of inductor peak current (at the filter stage), improving the efficiency over varying average power levels, simplifying the EMI filter design, and reducing the switching losses.

Alternatively, according to the results provided by the authors, addressing the energy density, based on the nominal voltage under the ceramic capacitors implemented, permits the observation of the real minimization of the total volume under the selected scheme.

Similar to the previous architecture, work [66] presents a topology where a large portion of the energy used is extracted by the arrangement in the backbone capacitors. The high energy density reduces the passive volume requirement according to the ripple voltage, so the capacitors used in the energy buffer have a similar capacitance with a different voltage rating. A pre-charge circuit ensures that the initial voltage is applied to the buffer capacitors. The SSC architecture is presented in Figure 7.

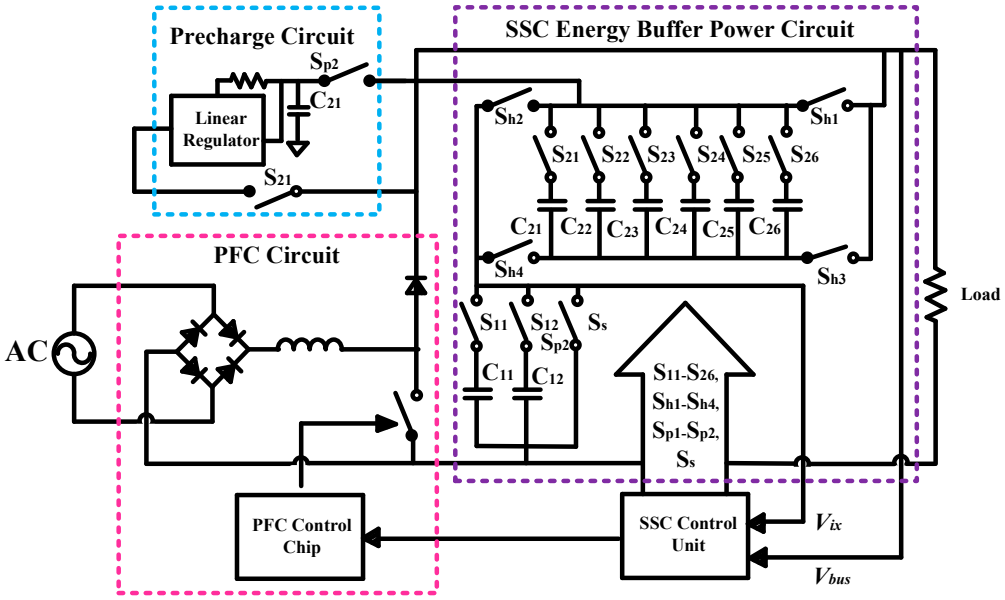

Figure 7. SSC energy buffer system: pre-charge circuit, SSC energy buffer, SSC control unit, and PFC circuit [66].

In contrast to the earlier works that utilized backbone and supporting capacitors with equal capacitance values, work [67] is a SSC architecture whose principal contribution is an optimization methodology that achieves a substantial increase in the effective energy density of the SSC energy buffer. This methodology optimizes the capacitance ratio of the capacitors used, in which the ripple ratio and the number of capacitors affect directly the increment of the energy density. With this capacitance, it is possible for the optimization to increase the effective energy density by 100% in a 1–10 enhanced unipolar architecture (with a 10% DC-bus voltage ripple) in comparison to when the energy buffer is designed

with equal capacitance values. This optimization permits a higher effective energy density and lower passive volume. The architecture based on SSC is an interesting APD method to implement for a twice-line power variation.

Another important point mentioned in the literature is that the bipolar scheme offers higher energy buffering at lower voltage ripple ratios than the unipolar scheme. This is not completely true, because according to [67], a higher ripple ratio allows a superior energy buffer performance; this means that the energy stored is a larger fraction of the energy buffer.

The optimal capacitance ratios in an SSC scheme permit a substantial improvement in the energy buffering ratio. This, in combination with the optimal choice of the capacitor, helps to enhance the energy buffering ratio. For example, from [67], for a 1–2 unipolar scheme designed for a 5% voltage ripple ratio, it is possible to have a reduction in the passive volume of 17%. Moreover, for a 1–10 unipolar architecture, it is possible to achieve a 100% increase in the energy buffering ratio. This increment presents a significant opportunity to increase the energy density of similar schemes, as shown in Figure 1.

Similar structures using the SSC method have been presented in the literature. Table 1 lists some principal reported works, where the electrical efficiency, power rating, and reduction of capacitance were considered as key comparison parameters. The maximum reduction and maximum efficiency were obtained with a 7.5 times reduction and 98.5% efficiency.

Table 1. Principal SSC methods reported in the literature: (η) efficiency, (V_{pp}) output ripple voltage, (R_c) required capacitance, (R_{ec}) resulting capacitance, (R_{edc}) reduction of capacitance.

Ref.	P (kW)	η (%)	(V_{pp})	(R_c) (μF)	(R_{ec}) (μF)	(R_{edc})	Comments
[46]	0.135	95.2	32	34.97	17.6	1.98	The objective is to restrict the apparent voltage ripple while utilizing a large fraction of the energy in the capacitors.
[47]	92	-	10	1248	624	2	Fewer power losses and a reduction of 60% in passive volume.
[53]	2	90	1.5	7200	960	7.5	The physical volume of the system decreased from 40 to 17 in^3.
[57]	0.008	98	21	720	560	1.2	Presents a methodology optimization for increasing the energy density.
[68]	0.06	93	5	141	47.2	3	Wide dimming range with combined frequency and selective phase shift tuning.
[69]	0.135	97.2	32	40	17.6	2.2	Achieves higher effective energy density and round-trip efficiency by modifying the control and switching patterns, maintaining the bus voltage ripple ratio, and applying fewer capacitors and switches than similar architectures.
[70]	0.3	98.5	20	980	280	3.5	Presents an improved closed-loop capacitance ratio optimization methodology.

Finally, as a summary, the principal characteristics of the SSC method are listed in Table 2.

As described above, unipolar and bipolar SSC energy buffer architectures have advantages that present them as an interesting APD alternative. Furthermore, both architectures present enhanced variants that permit them to increase the energy density and reduce volume. This improved performance is realized in the unipolar case by adding an extra switch, in the bipolar case by modifying its control stage, or in both cases by optimizing the capacitance ratio of the capacitors used.

Table 2. Characteristics of SSC as an APD method.

Advantages	Disadvantages
Can significantly reduce the capacitor size in a single-phase system.	Needs many switches and capacitors to maintain a narrow-range bus voltage while achieving high energy utilization.
Is effective in low-voltage, low-power DC–AC and AC-DC applications.	Presents more complexity.
The overall volume is much smaller.	It is crucial to identify the capacitance ratio that results in the highest effective energy density for a given SSC energy buffer topology.
Maintains a small DC-link voltage.	Commonly, the number of capacitors used has a stronger effect on the failure rate than the value of the capacitance itself.
Energy density can be almost doubled.	
Enables better capacitor reduction performance.	
Achieves higher energy efficiency conversion than magnetic passive solutions.	
Eliminates the need for inductors (eliminating magnetic losses).	
Utilizes relatively low blocking voltage switches (reducing conduction losses).	
Commutes at low multiples of the line frequency (minimizing switching losses).	
Presents a high-energy buffering capability.	
The energy buffer achieves a smaller bus voltage or a higher energy buffering ratio.	

3.2. VCAPD as an APD Method

Similar to the SSC architectures, the VCAPD method focuses on reducing the DC-link capacitor. This means that some topologies store energy in one inductor or capacitor. A focused work on a VCAPD method is [71]. The scheme is shown in Figure 8 and comprises a full-bridge inverter (S_1, S_2, S_3, and S_4) and a half-bridge inverter (S_5, and S_6), which are considered as the load arrangement made by C_d and L_{cx}. In this scheme, the 2ω power ripple is transferred to C_d, and the voltage on the C_d capacitor is controlled as a DC component superimposed with a second-order harmonic. However, rich harmonic content in the reference signal poses a challenge for controller design, and the problem gets worse for high-power applications, where the switching frequency is limited. So, the energy storage is greater than the energy used, ideally.

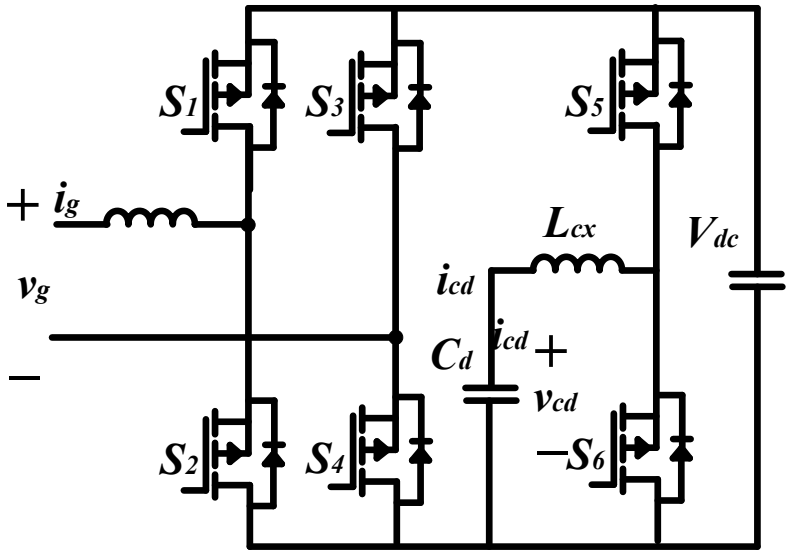

Figure 8. Capacitor energy storage in bipolar mode [71].

The PWM rectifier system with two capacitors (C_1 and C_2) as energy storage elements is shown in Figure 9. The power on C_1 and C_2 is equal to the 2ω ripple power; by controlling this power, the total capacitance required is less by using a single capacitor. Moreover, the capacitors C_1 and C_2 are used as DC filter capacitors. One disadvantage is the required DC voltage, because it is the sum of the voltage in C_1 and C_2. Therefore, the energy of C_1 and C_2 are not completely used for the compensation of the ripple power.

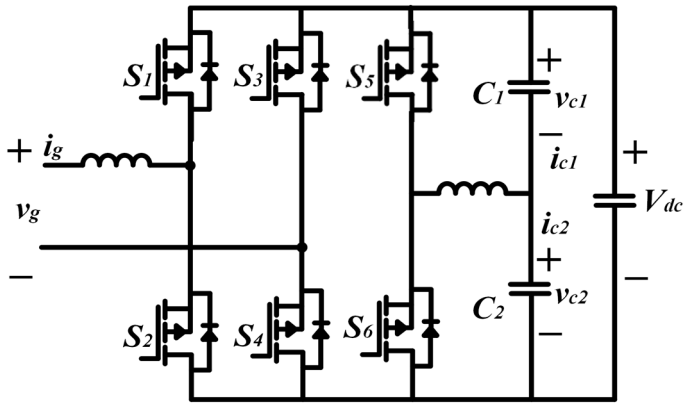

Figure 9. PWM rectifier system with two capacitors as energy storage elements.

Another alternative to this idea is to replace the *LC* circuit by applying a full-bridge inverter in parallel to the DC-link capacitor (Figure 10). The L_{ac}-C_{ac} circuit is used as a load in the inverter, so sinusoidal waveforms are obtained in C_{ac}. Based on the processed energy in C_{ac}, the DC capacitance is reduced. One drawback is the use of two extra switches to the half-bridge proposal.

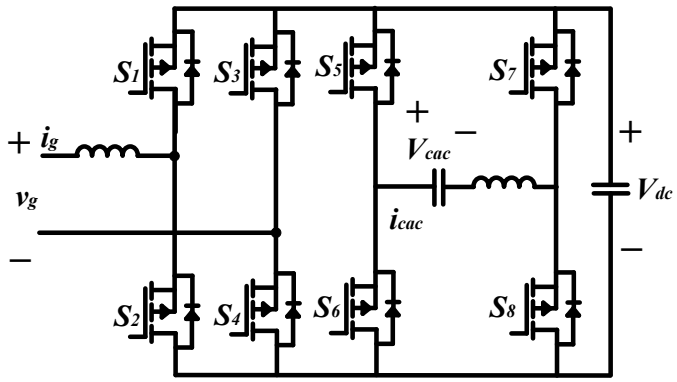

Figure 10. Capacitive energy storage with a full-bridge inverter.

Another approach based on VCAPD with minimum DC capacitance was introduced in [72]. Adding a phase leg in parallel to the full-bridge inverter and considering the L_c series circuit, the 2ω component can be absorbed, and the DC capacitance is reduced.

The method presented is shown in Figure 3 of the study published in [72]. Basically, by controlling the angle between the input voltage vs. and the input current i_s (which has the same value as i_a), the inverter acts as a pure capacitor. Meanwhile, by controlling the amplitude of i_s, the inverter can achieve continuous variable capacitance. Therefore, the inverter can be considered a variable capacitor.

A constant voltage across the DC capacitor C_{dc} is needed to operate the H-bridge inverter as a variable capacitor. The reference voltage for C_{ac} is a sinusoidal wave in the same frequency as the AC input voltage. Since the capacitor is always totally charged and discharged, full utilization of its energy storage capability is also attained. Furthermore, it was shown by the analysis that the current stresses of the two rectifier legs were not increased.

The three-phase legs can be modeled as a controlled voltage source, as shown in Figure 4 of the study published in [72]. To compensate for the grid side ripple power, the power reference of C_{ac} (P_{Cac}) should be controlled to be equal to the ripple power (P_{ripple}); so, the energy of C_{ac} (E_{cac}) should be

$$E_{cac} = \frac{1}{2} C_{ac} v_{Cac}{}^2 = \int P_{Cac} = \int P_{ripple} = \int v_s i_s \tag{14}$$

As shown in Equation (14), the ripple power is equal to P_s and can be calculated based on vs. and i_s. The capacitor voltage and current reference are accurate and simple to calculate directly, based on the power reference. The grid power reference has two parts: the DC component and the 2ω ripple AC component. Thus, by using a high-pass filter, the 2ω ripple power is obtained.

Figure 11 shows the overall control diagram of the active power decoupling. It consists of three controllers: the DC voltage controller, which maintains the DC-link voltage V_{dc}; the grid current controller, which takes charge of reactive power control; and the power decoupling controller, which controls the AC capacitor voltage V_{cs} and current I_c.

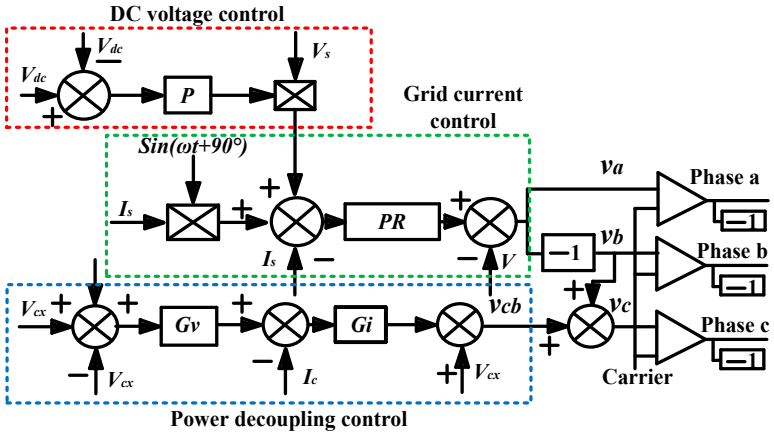

Figure 11. Control to proposed active power decoupling.

Experimental results show the capacitance reduction is nearly 13 times that of the conventional H-bridge inverter. This clearly shows that the advantages of this proposal are promising; however, the power density is not mentioned, and the control strategy is complicated. Furthermore, there are some problems related to the PR controller: its gain is much reduced at other frequencies, it is not adequate to eliminate harmonic influence caused by grid voltage, and the tuning process is difficult to achieve.

Another proposal is presented in [73], where a new current source converter topology for PV applications is detailed. The main advantages of this proposal are that the low ripple power was eliminated, the power density was increased because of the non-use of electrolytic capacitors, and the maximum power point tracking was improved.

The circuit proposed is shown in Figure 2 of the study published in [73]. The bidirectional switches are implemented by a series of an arrangement made by a diode and an IGBT. An inductor L_{dc} is placed in series with the PV. In a typical single-phase inverter, L_{dc} has to be a significantly large size to maintain the double-frequency ripple current, which results from the pulsating instantaneous power flow, at a sufficiently low level for proper operation of the converter. However, the DC link inductor in this topology is sized according to the switching frequency ripple components. Therefore, the size of L_{dc} is smaller than a conventional single-phase inverter.

In the case of the AC side of the converter, phase-legs a and c of the bridge are connected to the grid voltage v_g through an L_f-C_f filter. The phase-leg b of the converter is connected to the grid through C_b. The voltage across the C_b depends only on the current flowing through phase-leg b. With proper control of the current i_b, it is possible to

achieve a constant instantaneous power flow across the bridge. Thus, the low-power ripple is reduced.

Similar structures under the VCAPD method have been presented in the literature. Table 3 lists some of these principal reported works, where the electrical efficiency, power rating, and reduction of capacitance were considered as key comparison parameters. The maximum reduction and maximum efficiency were obtained in [74], with a 12.6 times reduction and 93.7% efficiency.

Table 3. Principal VCAPD methods reported in the literature: (η) efficiency, (V_{pp}) output ripple voltage, (R_c) required capacitance, (R_{ec}) resulting capacitance, (R_{edc}) reduction of capacitance.

Ref.	P (kW)	η (%)	(V_{pp})	(R_c) (μF)	(R_{ec}) (μF)	(R_{edc})	Comments
[61]	4	--	14.2	2025	440	4.6	Complex control, full utilization of capacitor energy.
[74]	1	93.7	10	757	180	4.2	Big inductance is used as filter, power density is reduced.
[75]	15	93.2	28	1600	300	5.33	DC capacitor reduction is not remarkable.
[72]	1.5	92	5	4600	385	11.94	Complex control, operation is limited to the resonant controller.
[76]	--	--	10	--	310	--	Half-bridge plus two capacitors and one inductor are used. Power density is reduced.
[77]	1	--	8	1658	132	12.5	Capacitance reduction is considerably reduced.

Finally, as a summary, some of the principal characteristics of the VCAPD method are listed in Table 4.

Table 4. Characteristics of VCAPD as APD method.

Advantages	Disadvantages
Capacitance is reduced by approximately 13 times as compared to using an electrolytic capacitor.	Control complex.
Current and voltage stress in switches can be reduced.	A dual loop with an outer voltage loop and an inner current loop is necessary for the control.
Stable DC voltage and fast dynamic response.	To minimize the voltage and current stress is necessary to adopt SPWM.
The proposed control can be extended to other single-phase power applications.	
The minimum energy storage in the capacitor is minimum E_{cmin}.	

As described above, the VCAPD method focuses attention on the reduction of the DC-link capacitor by varying the voltage across a passive component. In the case of the inductor, its low power density and high-power losses result in a poor strategy. However, as the literature shows, energy optimization by applying a capacitor is more efficient, and with this strategy, it is possible to reduce the DC-link capacitor up to ≈13 times from its nominal value.

3.3. RP-MII as an APD Method

Similar to the SSC and VCAPD methods, RP-MII as a power decoupling structure focuses attention on the reduction of the decoupling DC-link capacitor. According to the RP-MII definition, there are two operation approaches. One is connected through a transformer, and the other is through the connection in parallel to the rail voltage. These are shown in Figure 12a,b, respectively [78].

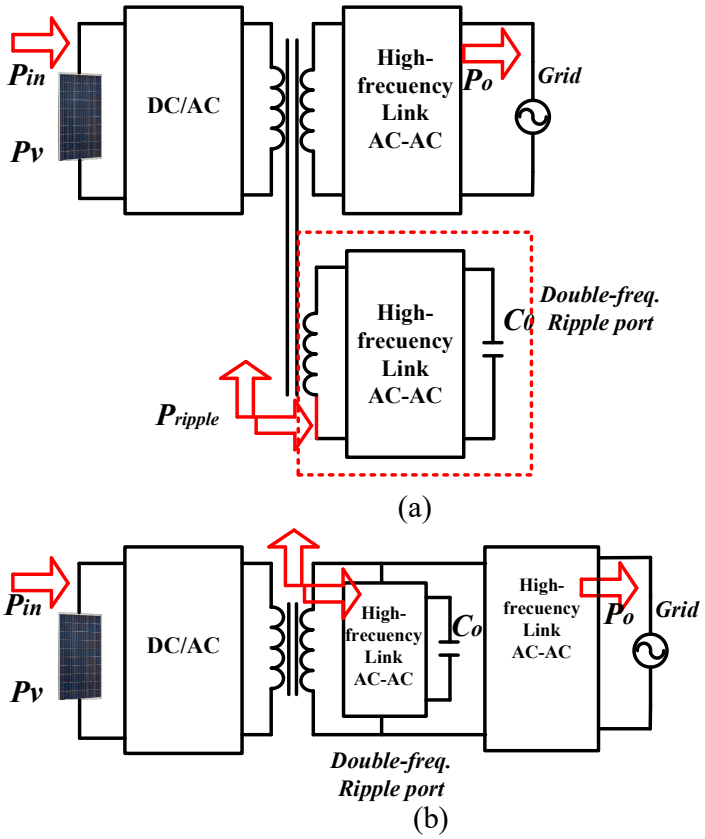

Figure 12. Approaches to the ripple port connections: (**a**) ripple port by using the rail voltage indirectly; (**b**) ripple port by using the rail voltage directly [78].

According to these configurations, in [79], a new PV-module integrated inverter is presented, where the ripple power consists of an inverter full bridge, an energy storage decoupling capacitor C_0, and an inductor to limit the instantaneous switching currents L_o. The proposed approach is presented in Figure 4 of the study published in [79], where the full-bridge inverter, plus the *LC* series circuit, is connected in parallel to the secondary side of the transformer.

As shown in [79], because the input voltage to the inverters is variable (AC), the inverter must provide a bidirectional current flow; so, MOSFETs connected in series are used as bidirectional switches.

Another focused work that integrates this strategy, but on the secondary winding side in a flyback DC–DC converter, and is a solid, reliable study is [80]. This work presents that one of the principal advantages is that the decoupling capacitor peak voltage (V_{dc}) can be reduced by applying a higher voltage because V_{dc} is not limited by the DC-link. It aims to use film capacitors instead of electrolytic ones. This work is shown in Figure 2 of the study published in [80].

In [80], the RP-MII consists of a full H-bridge inverter comprising four switches (Q_1, Q_2 *and* Q_3, Q_4), and an *LC* filter (L_D, C_D). Basically, the role of the ripple port consists of power processing on the DC-link, and its principal purpose is to be able to process the power difference between the input and output (P_{pv} and P_o). Furthermore, the capacitor C_{dc} determines the required decoupling component for a specific power rating. The topology also contains a voltage source inverter (VSI) comprising S_1, S_2, S_3, and S_4 and a second-order low-pass filter comprising L_f and C_f.

An important point regarding the ripple cancelation process, from the work presented in [80], is the simplicity in the control stage, because to control the voltage across C_{dc} (which stores the excess power and feeds the output when necessary), it only has to apply the sinusoidal pulse width modulation (SPWM) technique and aims for the topology to

be simpler than others. Another advantage is that the ripple port can be used with any isolated DC–DC converter capable of boosting the input voltage with galvanic isolation for grid-connected applications.

Another alternative is to place the power ripple port in parallel to the PWM rectifier, similar to the other options. This topology is presented in Figure 1 of the study published in [81], where the RP-MII comprises an energy storage decoupling capacitor (C_{dc}), an inductor (L_D) to limit and filter instantaneous switching currents, and an H-bridge (S_1, S_2, S_3, and S_4) to control the bidirectional current flowing in the decoupling capacitor (C_{dc}).

Another alternative is [82], where the proposed converter is based on the traditional flyback converter, adds a circuit as the third port to eliminate the low-frequency current ripple. This topology is shown in Figure 2 of the study published in [82].

From Figure 2 in [82], the excess energy of the ripple port is processed by auxiliary winding, switches (S_{x1} and S_{x2}), diodes (D_{x1} and D_{x2}), and a capacitor (C_x), where, by charging and discharging the auxiliary capacitor, the switches and diodes are used. The transformer stores the same energy during each commutation, so the input power is constant, and the output power is given by the energy processing from the ripple port.

In [83], a novel active filter technique using a RP-MII with multiport structure is presented (the scheme is shown in Figure 2 of the study published in [83]). To suppress the power pulsating at the DC link, the inverter proposed has two identical circuit structures, circuit A and circuit B. Moreover, the ripple port is composed of one capacitor and one inductor. The circuits A and B consist of a boosting switching cell and a half-bridge inverter. The A and B circuit work in different fundamental cycles. For example, when the reference voltage is in the positive half cycle ($v_{in}(t) > 0$), the A circuit will be active, and the B circuit will be in an off state; in the complementary half cycle, the B circuit will be active, and the A circuit will be in an off state.

Each circuit has one energy storage element, C_1 or C_2. Compared to alternatives to the ripple port, the proposed inverter adopts the concept of a switched-capacitor circuit and uses the semiconductor power devices and capacitors to build a circuit without large magnetic components.

The advantage of the ripple port is the direct control over the decoupling capacitor voltage and current. Therefore, the AC capacitor C_d is totally employed to store low ripple energy.

Additional to the advantages, the presented topology includes the following: (1) ability to boost the output voltage with a multilevel operation, (2) utilization of GaN devices to increase the power density, and (3) the ripple power is processed with no additional component cost or external circuit.

The approach presented in [84] consists of a flyback converter using an active power decoupling circuit with auxiliary winding, and a novel switching sequence is proposed. The proposed topology is shown in Figure 1 of the study. This proposal consists of a three-port flyback converter configured by DC port, AC port, and ripple port. The AC port is connected to the flyback by the inverter switch S_D. The ripple port considers a small value of the inductor to attenuate switching frequency and prevent drastic current flow to the capacitor, auxiliary switch, and decoupling capacitor. As can be seen, the ripple port has two switches; both are used for charging and discharging the decoupling capacitor in the ripple port. In the mode of charging and discharging, the DC input power is compared with the instantaneous output power. If the output power is higher than the input power, excess energy will be demanded, so the decoupling capacitor will process it. In contrast, when the input power is smaller than the output power, the shortage of power is supplied by the charged energy in the decoupling capacitor. An equivalent diagram of the charging and discharging mode is shown in Figure 3 of the study published in [84].

Another option to RP-MII is presented in [49]; the main advantage of this proposal is the alternative to choose the capacitor voltage to optimize its voltage stress.

The paper considers an alternative active filter configuration, as shown in Figure 5 of the study published in [49], in which a third energy management port is added to the

converter. The voltage variation on the capacitor is large by design, and the power ripple is controlled directly to achieve the desired double-frequency value. Given a target capacitor voltage, this configuration can be used to achieve the minimum possible capacitance value for the system, since energy storage is addressed directly. When the capacitor voltage is controlled, the power flow in the ripple port cancels the power flow in the AC port, so the combined effect yields the desired smooth, constant power at the DC port. It was concluded that for voltage ranges up to 400 V, the active filter capacitance of 33 nF per watt was sufficient for the power ripple cancellation in a single-phase 60 Hz application.

Similar structures under the RP-MII method have been presented in the literature. Table 5 lists some of these principal reported works, where the electrical efficiency, power rating, and reduction of capacitance were considered as key comparison parameters.

Table 5. Principal RP-MII methods reported in the literature: (η) efficiency, (V_{pp}) output ripple voltage, (R_c) required capacitance, (R_{ec}) resulting capacitance, (R_{edc}) reduction of capacitance.

Ref.	*P* (kW)	η (%)	(V_{pp})	(R_c) (μF)	(R_{ec}) (μF)	(R_{edc})	Comments
[79]	0.2	95.6	1.25	1700	150	11.33	This proposal can increase the power density; however, additional component cost is added.
[80]	0.23	-	12	200	100	2	Easy control stage by applying the SPWM modulation.
[81]	0.1	-	8	1330	220	6	The design and control are easy.
[85]	0.5	-	20	156	14	11.1	Controlled using a modulator-based regulator, requires multiple control loops and tuning numerous gains.
[86]	0.16	90	5.5	200	150	1.3	Closed-loop strategy implemented, which guarantees the ripple cancellation even under time-varied conditions.

From the above characteristics, Table 6 lists some important advantages and disadvantages of the RP-MII.

Table 6. Characteristics of RP-MII as APD method.

Advantages	Disadvantages
The interface of the grid network can be performed by thyristors.	Introduces substantial implementation complexity.
The control stage at a closed loop is simpler than other APD techniques.	Potential added cost.
Reduces the size of the overall system by eliminating a rectifier stage.	
Can support inverter and rectifier applications.	
Increases the MPPT performance in the PV-connected system.	
Achieves the minimum possible capacitance value in a determined application since energy storage is addressed directly.	
Is controlled directly to achieve the desired double-frequency value.	
The decoupling capacitor voltage is independent of other system voltages.	
Permits direct control of the ripple power, allowing direct control over the coupling capacitor voltage and current.	
Avoids voltage limitations of the DC–DC topology.	

4. Comparison of SSC, RP-MII, and VCAPD

The decoupling methods previously described are classified and compared according to the electrical efficiency, quantity of components, resulting decoupling capacitance, reduction of initial decoupling capacitance, processed energy, power, and technical features, which are shown in Table 7.

Table 7. Comparison of decoupling strategies: (*Dca*) decoupling capacitance, (*P*) power rating, (f_{sw}) switching frequency, (*E*) energy, (η) efficiency, and (V_{dc}) DC-link voltage.

Ref.	Type of Method	Topology	*Dca* (μF)	*P* (W)	f_{sw} (kHz)	*E* (J)	η (%)	V_{dc} (V)	Additional Elements	Features
[80]	RP-MII	Flyback	36	235	100	0.72	--	200	4 MOSFETs, 1 inductor, and 1 capacitor.	Simple control; ripple current suppression to less than 10% peak-to-peak.
[81]		Full-bridge inverter	220	100	100	0.352	--	200	4 MOSFETs, 1 inductor, and 1 capacitor.	The design and control are easy and affordable.
[85]		Flyback	14	500	40	0.077	--	250	4 MOSFETs, 1 inductor, and 1 capacitor.	The control requires multiple control loops and tuning numerous gains.
[53]	SSC	Single-phase inverter	80	2000	--	0.048	90	400	16 switches and 11 capacitor.	DC–AC conversion, high-frequency operation, and SiC-MOSFET solution by applying variable-frequency constant peak current control.
[65]		Single-phase inverter	--	2000	--	--	90	--	--	Advanced implementation of the SSC architecture, soft-switching SiC-FET DC–AC conversion, and digitally implemented variable-frequency constant peak current control.
[87]		Flyback	46	110	50	0.29	90.6	150	5 MOSFETs and 2 capacitors.	The transformer leakage energy is stored in the decoupling capacitor with minimal added components.
[74]	VCAPD	Single-phase inverter	180	1000	19.2	0.63	93.7	350	1 capacitor and 1 inductor.	The capacitance is considerably reduced.
[72]		Single-phase inverter	385	1500	10.8	1.33	92	200	2 MOSFETs, 1 inductor, and 1 capacitor.	The control is complex, and the operation is limited to the resonant controller.

5. Concluding Remarks

Some main features offered for the APD studied methods are listed below.

For SSC.

The SSC energy buffer has a higher effective energy density than most of the APD methods reviewed. Moreover, optimizing the capacitance ratio of the complete architecture permits a reduction in the total passive volume, allowing it to have efficiency that is similar to the electrolytic capacitors that it replaces, but with half the passive volume that they generate. In some works, such as [43,73], it is possible to achieve high efficiency (98%) and an important capacitance reduction (up to 7.8 times) above the original decoupling component. Other important features are listed below:

- Greater energy efficiency is achieved and a substantial reduction of the decoupling capacitor due to the effective use of stored energy;
- Higher effective energy density (an increment of 100%) and lower passive volume are achieved by energy buffer optimization;
- Small DC-link voltage is maintained;
- Need for inductors is eliminated (eliminating magnetic losses).

For VCAPD.

The VCAPD method reduces the decoupling capacitance, and the electrical efficiency is improved compared to the use of an inductor as an energy storage element. The literature shows that the maximum reduction and efficiency by applying this method were obtained in [19], with a 12.6 times reduction and 93.7% efficiency. However, the power density was not mentioned, and the control strategy is complicated. For example, the PR controller gain is limited to a range of frequencies, the harmonics generated by the grid voltage are not eliminated, and the PR controller tuning is complex.

For RP-MII.

The RP-MII permits a considerable reduction in the decoupling capacitor by applying it to a higher voltage because it is not limited by the DC-link. With this characteristic, it is possible to reduce up to 11.33 times the decoupling capacitor, and it has high efficiency (95.6%), enabling the use of a very small and highly reliable film capacitor. This improves the power density of the entire system. Other important features are listed below:

- Overall size of the system is reduced by eliminating a rectifier stage;
- Inverter and rectifier applications are supported;
- Most simple control stage (SPWM) is performed;
- Reduced decoupling capacitor peak voltage (Vdc) by applying a higher voltage, because Vdc is not limited by the DC-link;
- Any isolated DC–DC converter can be implemented;
- Direct control over the decoupling capacitor voltage and current can be performed;
- Better MPPT performance in the PV-connected system;
- Minimum possible capacitance value for the system with a nominal load (the active filter capacitance of 33nF per watt is sufficient for power ripple cancellation in a single-phase 60 Hz application) can be achieved;
- Voltage limitations of the DC–DC topology are avoided.

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