

Review

Hybrid System of Polystyrene and Semiconductor for Organic Electronic Applications

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Abstract: While organic semiconductors hold significant promise for the development of flexible, lightweight electronic devices such as organic thin-film transistors (OTFTs), photodetectors, and gas sensors, their widespread application is often limited by intrinsic challenges. In this article, we first review these challenges in organic electronics, including low charge carrier mobility, susceptibility to environmental degradation, difficulties in achieving uniform film morphology and crystallinity, as well as issues related to poor interface quality, scalability, and reproducibility that further hinder their commercial viability. Next, we focus on reviewing the hybrid system comprising an organic semiconductor and polystyrene (PS) to address these challenges. By examining the interactions of PS as a polymer additive with several benchmark semiconductors such as pentacene, rubrene, 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene), 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT), and 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C₈-BTBT), we showcase the versatility of PS in enhancing the crystallization, thin film morphology, phase segregation, and electrical performance of organic semiconductor devices. This review aims to highlight the potential of an organic semiconductor/PS hybrid system to overcome key challenges in organic electronics, thereby paving the way for the broader adoption of organic semiconductors in next-generation electronic devices.

Keywords: hybrid system; polystyrene; organic semiconductor; organic thin film transistors; organic electronics



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1. Introduction

The field of organic semiconductors has witnessed remarkable advancements in recent years, particularly in enhancing charge carrier mobility, which is a factor that critically governs the performance of a wide array of electronic devices [1–12]. This progress has been driven by innovations in material design, molecular engineering, and processing techniques, each contributing to the development of organic semiconductors with increasingly competitive performance characteristics [13–17]. The ability to fine-tune molecular structures to promote efficient charge transport, coupled with precise control over the crystallization and morphology of thin films, has brought organic semiconductors closer to their inorganic counterparts in terms of mobility and device efficiency [18–20]. These advancements have not only broadened the application potential of organic semiconductors in devices such as organic thin-film transistors (OTFTs) [21–23], but also elucidated the underlying mechanisms and the innovative techniques that have made these achievements possible, paving the way for their integration into commercial technologies that would require both scalability and high performance [24–32]. In this section, we will focus on reviewing the research advances made in enhancing the charge carrier mobility, developing controlled crystallization techniques, and exploring the applications in organic electronic devices.

1.1. Advances in Charge Carrier Mobility

The research efforts in recent years have switched to enhancing the charge carrier mobility of organic semiconductors, focusing on innovations in material design, molecular engineering, and processing techniques. Material design has focused on developing new organic semiconductors with optimized molecular structures that promote efficient charge transport [33–41]. This includes designing molecules with extended conjugation, which facilitates better π - π stacking interactions between adjacent molecules, leading to improved charge carrier mobility [42–46]. Additionally, the incorporation of side chains that enhance solubility and self-assembly has been reported as crucial in achieving uniform thin-film morphologies [47–56]. Material design also involves the strategic selection of functional groups that can enhance intermolecular interactions, thereby improving the overall electronic properties of the semiconductors [57–63].

Molecular engineering further refines these designs by tailoring the electronic properties of the organic semiconductors at the molecular level. This approach often involves modifying the molecular backbone [64–66] or side chains [52,67–75] to control the energy levels, molecular packing, and crystallinity of the semiconductors. For example, introducing electron-donating or electron-withdrawing groups can tune the energy levels of the semiconductor, optimizing it for specific applications such as *p*-type or *n*-type conduction in OTFTs [76–88]. Molecular engineering also enables the design of semiconductors with improved environmental stability by incorporating elements that protect against oxidation or photodegradation, thereby extending the operational lifespan of the organic electronic devices [89–91].

Processing techniques play a critical role in transforming these molecular designs into high-performance devices. Advances in solution-based processing methods, such as spin coating [92,93], inkjet printing [94–99], and spray coating [100–102], have enabled the production of thin films with precise control over thickness, crystallinity, and morphology. These techniques allow for the deposition of organic semiconductors in a manner that promotes optimal molecular alignment and crystallization, which are key to achieving both optimized thin film morphology and high charge carrier mobility. Additionally, post-deposition treatments, such as thermal annealing [103–107] or solvent vapor annealing [108,109], are employed to further enhance the crystallinity and reduce defects within the films, leading to more consistent and higher-performing organic semiconductor devices. These processing innovations are essential for scaling up the production of organic electronics while maintaining the high performance required for commercial applications.

1.2. Advances in Controlled Crystallization Techniques

The performance of organic semiconductors is critically dependent on the crystallinity, molecular alignment, and morphology of the thin films formed during device fabrication [110–115]. Controlled crystallization techniques by virtue of external forces have therefore become a focal point in advancing organic semiconductor technology, as they enable the precise manipulation of these parameters to optimize charge transport and device efficiency. Many external force-based methods have been developed to achieve controlled crystallization, each offering unique advantages in directing crystal growth, improving thin-film morphology, and enhancing charge transport properties. These methods can be mainly categorized into capillary force alignment-based techniques, solution shearing-based techniques, temperature gradient-based techniques, zone casting-based techniques, surface energy patterning-based techniques, and so on.

Capillary force alignment is a technique that utilizes the capillary forces generated by a meniscus of liquid to align organic semiconductor molecules during the drying process [116–119]. As the solvent evaporates, capillary forces guide the molecules into an ordered arrangement, promoting uniform crystallization. This method is particularly effective in creating highly aligned thin films with long-range order, which is essential for reducing crystal anisotropy and nonuniformity. The capillary forces help to minimize defects and grain boundaries, leading to smoother films with enhanced charge

transport properties. For example, Bi et al. apply the capillary force-based controlled evaporative self-assembly (CESA) technique alongside a binary solvent system to direct crystal growth of 2,5-di-(2-ethylhexyl)-3,6-bis(500-n-hexyl-2,20,50,200)terthiophen-5-yl-pyrrolo[3,4-c]pyrrole-1,4-dione (SMDPPEH) [120]. As shown in the polarized optical image of Figure 1a, implementation of this highly effective CESA method and optimization of the solvent ratios produced well-aligned SMDPPEH crystals with greatly enhanced area coverage.

Solution shearing involves dragging a meniscus of organic semiconductor solution across a substrate using a blade or other shearing tool [121–124]. This technique applies a directional shear force that aligns the molecules in the direction of the shearing motion, encouraging the formation of large, well-ordered crystals. Solution shearing is advantageous for producing uniform thin films over large areas, with controlled crystallization leading to high-performance devices. The alignment of the crystals in the shearing direction results in more uniform charge transport, which can be beneficial for specific devices that require high consistency of electrical performance. Kim et al. utilized the shearing method to align the misoriented of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene), which induced a uniform alignment of the organic semiconductor [125]. As shown in the device optical image of Figure 1b, well-aligned TIPS pentacene were formed using an inorganic polymer allylhybridpolycarbosilane (AHPCS) as the shearing blade, showcasing the applicability of solution shearing to printed flexible electronics.

Temperature gradient methods involve the application of a controlled temperature gradient across the substrate during the crystallization process [126–128]. This gradient induces directional crystal growth, with the organic semiconductor molecules aligning along the temperature gradient. Temperature gradient techniques allow for precise control over crystal size and morphology, leading to films with high crystallinity and uniform orientations. These methods are particularly effective in producing large, single-crystal domains, which are ideal for maximizing charge carrier mobility. For instance, Asaree Yeboah et al. reported an effort to reduce the crystal misorientation of TIPS pentacene/poly(α -methyl styrene) (P α MS) blends by applying the temperature gradient [129]. As displayed in the optical image of Figure 1c, the crystal alignment appears to be relatively uniform, with the crystalline structures extending in parallel lines across the image. The more even spacing and consistent directionality of the crystals imply a high degree of crystallinity and structural integrity in this region of the material.

Zone casting is a technique where a solution of organic semiconductor is cast onto a moving substrate, and a heating element selectively melts and recrystallizes the material in a controlled manner [130–133]. The movement of the substrate and the controlled heating zone promote the growth of well-aligned crystals along the casting direction. Zone casting is highly effective for producing continuous, large-area films with controlled crystallization and minimal grain boundaries. This method is particularly useful for applications requiring high charge transport efficiency. Mas-Torrent et al. reported the creation of extensive, well-aligned films of dithiophene-tetrathiafulvalene (DT-TTF) using the zone casting method [134]. As shown in the optical image of Figure 1d, the black arrow shows the direction of casting, while the white arrows highlight certain areas on the substrate that remain uncovered by the organic layer. It can be inferred that the DT-TTF films were highly aligned through zone casting on a Si/SiO₂ substrate.

Surface energy patterning involves the modification of the substrate surface to create regions with different surface energies, which guide the crystallization of the organic semiconductor [135–138]. By patterning the surface energy, the nucleation and growth of crystals can be controlled, leading to films with desired crystal orientations and morphologies. Surface energy patterning is a powerful tool for directing the self-assembly of organic molecules, enabling the fabrication of highly ordered thin films with tailored electronic properties. This method is particularly advantageous for creating complex device architectures with precise control over the active layer's morphology and alignment. Harper et al. introduced a surface energy patterning-based technique for contact deposition and pattern-

ing and created fully printed OTFTs on paper [139]. Their approach involves depositing contacts via aerosol spray and patterning them using a digitally printed mask produced by a standard office laser printer, all conducted at room temperature and pressure.

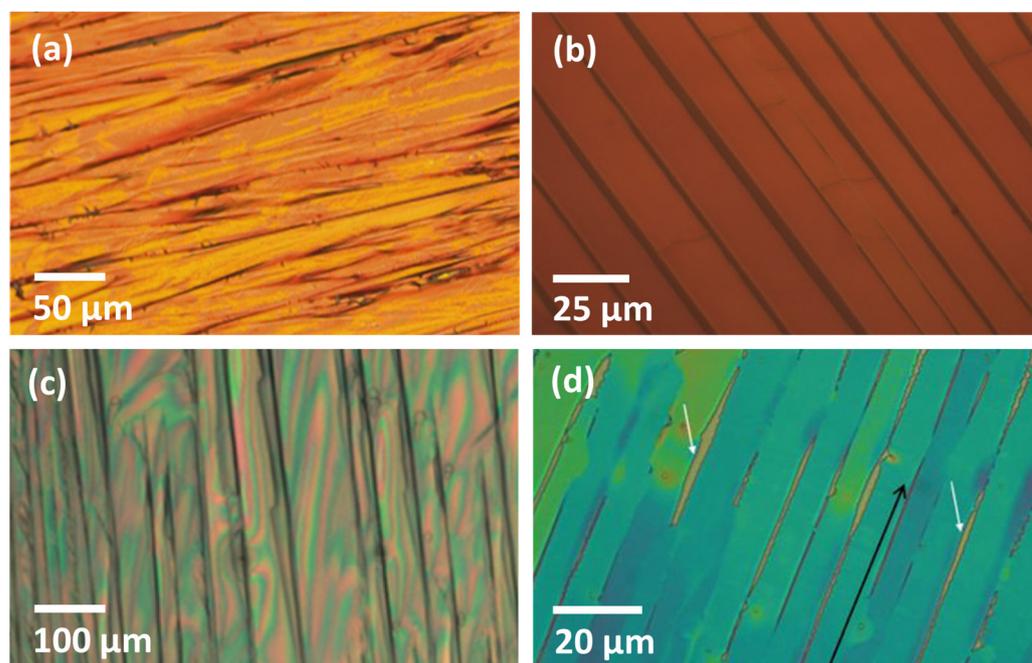


Figure 1. Optical images showing: (a) SMDPPEH crystals aligned by using the capillary force-based CESA method; (b) TIPS pentacene crystals aligned by using the solution-shearing method based on an inorganic polymer blade; (c) TIPS pentacene crystals aligned by using the temperature gradient method; (d) DT-TTF films well-aligned by using the zone-casting method. Reproduced from reference [120,125,129,134], with permission from Elsevier, American Institute of Physics, and Wiley.

Each of these controlled crystallization techniques, as mentioned above, plays a crucial role in advancing the performance of organic semiconductor devices. By enabling the precise manipulation of crystal growth, thin-film morphology, and molecular alignment, these methods contribute to the development of organic electronics with enhanced charge transport properties, improved device stability, and greater scalability. As the field continues to evolve, the refinement and combination of these techniques will be essential for pushing the boundaries of what organic semiconductors can achieve in commercial applications.

1.3. Advances in Organic Electronic Applications

These advancements in charge-carrier mobilities and controlled crystallization techniques have brought organic semiconductors closer to their inorganic counterparts, making them more competitive for a wider range of applications, including OTFTs, photodetectors, gas sensors, and inverters, each of which leverages the unique properties of these materials for specific functionalities. In OTFTs, organic semiconductors function as the active channel material, where they modulate the flow of charge carriers (electrons or holes) between the source and drain electrodes under the influence of a gate voltage [140–142]. The performance of OTFTs is highly dependent on the mobility of these charge carriers, which is influenced by the molecular packing and crystallinity of the organic semiconductor. In photodetectors, organic semiconductors act as the light-absorbing material that converts incoming photons into electrical signals [143–151]. When light is absorbed, excitons are generated and separated into free carriers, creating a photocurrent that is proportional to the intensity of the incident light. The sensitivity and speed of photodetectors are influenced by the absorption spectrum and charge mobility of the organic semiconductor, which further highlights the research efforts to enhance the charge carrier mobilities. Gas

sensors utilize organic semiconductors for their sensitivity to chemical interactions with gas molecules [152–158]. When exposed to specific gases, the organic semiconductor's electrical properties, such as conductivity or mobility, can change due to interactions between the gas molecules and the semiconductor's surface or bulk. These changes can be detected and correlated with gas concentration, making organic semiconductors ideal for detecting trace amounts of gases. In inverters, organic semiconductors are employed in complementary circuits where *p*-type and *n*-type materials are used to switch between different states (i.e., on/off) based on the input voltage [159–164]. The operation of inverters relies on the effective charge transport and stability of the organic semiconductor materials, as they need to rapidly switch states without significant energy loss. The performance and efficiency of these devices depend heavily on the quality of the organic semiconductor, including its crystallinity, molecular alignment, and interaction with other materials in the device.

2. Challenges in Organic Electronics

Despite organic semiconductors having shown great potential for use in flexible and lightweight electronic devices, their implementation is often hindered by several intrinsic challenges, including low charge-carrier mobility, susceptibility to environmental degradation, difficulty in achieving uniform thin-film morphology and crystallinity, poor interface quality, and issues with scalability and reproducibility. Insulating polymers, when employed as additives, can form a hybrid system with the organic semiconductor and crucially enhance the performance of organic electronics by optimizing charge transport, increasing stability, refining film structure, improving interface interactions, and ensuring consistent manufacturing quality. While conjugated and semicrystalline polymers play important roles in organic electronics, our emphasis in this review is on insulating polymers due to their proven effectiveness in enhancing charge transport and improving device performance. Therefore, throughout the manuscript, all references to polymer additives pertain specifically to insulating polymers. This section discusses the key challenges faced by organic semiconductors, their root causes, and how polymer additives can, in general, mitigate these issues to enhance device performance. It is important to note that while polymers can also be applied to other categories of organic semiconductors [165,166], the examples reviewed in this paper predominantly highlight their effectiveness in small molecular systems. This distinction highlights the tailored role of insulating polymers in optimizing small molecular semiconductors.

2.1. Charge Carrier Mobility and Trap States

The charge carrier mobility in organic semiconductors is often lower compared to that in inorganic semiconductors [167–169]. Since the interface between the semiconductor and dielectric layers plays a pivotal role in determining the efficiency of charge transport, the presence of trap states at the semiconductor interface, caused by surface roughness, impurities, or disordered molecular packing, can capture charge carriers, hinder their free movement, and further reduce the overall electrical performance of organic semiconductors [170–173]. Reduced charge carrier mobility directly affects the efficiency and speed of organic electronic devices. In OTFTs, for example, low mobility leads to slower switching speeds and reduced current output, limiting the application of these devices in high-speed electronics. Insulating polymer additives can be utilized to create smoother interfaces that reduce the density of trap states; by introducing polymer additives during fabrication, the morphology of the interface can be modified to reduce surface roughness and minimize the density of trap states [174]. This smoother, more uniform interface mitigates the formation of localized energy states that trap charge carriers, thereby improving charge mobility, lowering threshold voltages, and enhancing operational stability. This demonstrates the crucial role of polymer additives in optimizing interfacial properties to achieve superior functionality in organic electronic devices. In addition to their role in improving thin-film morphology and reducing charge trapping in devices like OTFTs, certain insulating polymers, such as P α MS, can also serve as electrets with charge storage capabilities, which

are critical for organic memory applications. For example, Baeg et al. demonstrated the electret nature of polymers in organic non-volatile memory devices, where the polymeric gate electret serves as a charge-trapping site and modulates the field-effect behavior of the device [175]. This highlights the dual functionality of insulating polymers, not only for enhancing mobility in organic semiconductors but also for enabling charge storage in memory devices. By distinguishing between these applications, we clarify the broader utility of insulating polymers in organic electronics.

2.2. Stability and Degradation

Organic semiconductors are highly vulnerable to environmental factors, including exposure to oxygen, moisture, and UV light, which can induce chemical degradation. This degradation is a significant concern as it often leads to the formation of new trap states within the semiconductor material, along with alterations in the molecular structure. Over time, these degradative processes can cause substantial drops in performance of the organic electronic devices, which directly correlates with a shortened operational lifespan and decreased reliability. This is particularly problematic for commercial applications where devices are expected to maintain consistent performance over extended periods [176–178]. To address these challenges, polymers can be strategically employed to enhance the stability of organic semiconductors [179]. One approach involves using polymers as protective layers that physically shield the semiconductor from harmful environmental impacts [180]. These protective coatings can effectively prevent oxygen, moisture, and UV light from penetrating the semiconductor, thereby mitigating the onset of chemical degradation. Another approach involves incorporating polymers directly into the semiconductor matrix [181], where they can improve the material's intrinsic stability by reinforcing the molecular structure and reducing the likelihood of trap state formation. This incorporation can also help to maintain the electrical properties of the semiconductor over time, ensuring more stable device performance. Thus, by using polymers as protective layers or as components within the semiconductor matrix, the stability and longevity of organic semiconductors can be significantly improved, ensuring that they meet the demands of commercial applications where long-term stability is essential.

2.3. Morphological Control and Crystallinity

The performance of organic semiconductors is highly dependent on their thin-film morphology and crystallinity. Achieving uniform and well-ordered crystalline films is challenging due to the flexible nature of organic molecules and the sensitivity of their crystallization process to processing conditions. Organic crystals have been reported to form misoriented crystals with poor alignment in long range. For example, TIPS pentacene [182–189] have a tendency to grow into dendritic crystals with random orientation and poor substrate coverage. Additionally, organic crystals also exhibit considerable amounts of grain boundaries when drop-casted and crystallized in solution [190,191]. Grain boundaries are known to be located with defects and charge trap centers and are therefore detrimental to the electrical charge transport of organic semiconductors [192–197]. Furthermore, non-uniform film morphology and poor crystallinity lead to inconsistent charge transport properties, increased trap densities, and overall reduced device performance. This is particularly problematic in large-area devices where uniformity is critical for consistent functionality across the entire device [198,199]. Polymers can be used to control the crystallization and morphology of organic semiconductor films. In particular, the addition of polymers helps eliminate de-wetting issues [200–202] and leads to the formation of a more uniform and crystalline film, which enhances charge-carrier mobility. Additionally, polymer additives, when mixed with organic semiconductors in solution, can induce phase segregation that promotes the growth of larger, more ordered crystalline domains, thereby improving the overall film quality and device performance [203–205].

2.4. Interface Engineering

The interfaces between organic semiconductors and other device components, such as dielectric layers or electrodes, play a crucial role in determining charge injection and transport properties [206–211]. Poor interface quality can lead to increased energy barriers, charge recombination, and higher trap densities [212,213]. Inefficient charge injection and transport across interfaces can significantly reduce the efficiency of organic electronic devices, leading to higher power consumption, lower on/off ratios, and reduced device performance [214–218]. Polymers can either be mixed with the organic semiconductor as an additive or deposited as a polymer layer before the deposition of the organic semiconductor to effectively modify and improve the interfaces in organic electronic devices. One approach to achieving such improved interfaces is to mix the organic semiconductors with polymer additives, which allows the formation of a hybrid system [219–225]. This semiconductor/polymer hybrid system may further become vertically phase-segregated and/or laterally phase-segregated, which offers additional merits to control the morphologies and charge transport [226–231]. Another approach is to deposit a polymer additive layer (i.e., on top of the hydrophilic silicon dioxide film) prior to the deposition of the organic semiconductor as the active layer [179]. This relocates the charge transport pathway at the polymer interface from the silicon dioxide interface, which successfully passivates the silanol groups on silicon dioxide in these cases [232,233], and can be especially beneficial for the charge transport in *n*-type organic semiconductors such as PDIF-CN₂ molecules [234–237].

2.5. Scalability and Reproducibility

Scaling up the production of organic semiconductor devices while maintaining consistent quality is challenging due to the sensitivity of organic materials to processing conditions. Variations in film thickness, crystallinity, and molecular alignment can lead to significant batch-to-batch variability, resulting in inconsistent device performance across large-area production runs, which limits the commercial viability of organic electronics [129,238,239]. Poor reproducibility can lead to higher manufacturing costs and lower yield rates, posing major obstacles for large-scale applications. Incorporating additional polymers can improve the reproducibility and scalability of organic semiconductor device fabrication by offering more precise control over key parameters such as film morphology, crystallinity, and interface quality. Polymers can be used to regulate film thickness during the deposition process, ensuring uniform coverage across large substrates [240,241]. By incorporating a polymer with appropriate viscosity and solubility properties, the coating process can achieve a more consistent film thickness, reducing the likelihood of defects that arise from uneven layers [242–244]. Furthermore, polymers can influence the crystallinity of organic semiconductors by acting as nucleating agents or by modulating the crystallization kinetics [245–249]. This control over crystallization helps produce films with uniform crystal sizes and orientations, which is crucial for achieving consistent electronic properties across different batches. Additionally, polymers can aid in the alignment of molecular chains within the semiconductor layer, promoting a uniform molecular orientation that enhances charge transport and reduces variability in device performance [250–254]. By improving the reproducibility of film thickness, crystallinity, and molecular alignment, polymers play a vital role in scaling up the production of organic semiconductor devices, making the fabrication process more reliable and economically viable for large-scale applications.

3. Hybrid System of PS and Organic Semiconductors

Building on the discussion of the challenges faced by organic semiconductors and the utilization of polymers to address these issues, this section reviews the specific strategies for overcoming these obstacles through the integration of PS with various organic semiconductors. PS serves as a representative example of how an insulating polymer can be effectively employed to modify and improve the properties of organic semiconductors such as pentacene [255–257], TIPS pentacene [90,258–260], rubrene [87,261,262], and others [200,263–265] (Table 1). The incorporation of PS into these organic semiconductors

has emerged as a versatile strategy to enhance the performance of OTFTs: PS can be used in various roles, such as a surface treatment material, a polymer additive, or as part of a composite with organic semiconductors. The interaction between PS and these semiconductors has been shown to influence critical factors such as film morphology, crystallinity, molecular alignment, and interface quality, all of which are pivotal in determining the electrical performance of the devices. By modifying these parameters, PS can help reduce charge-trapping sites, improve charge-carrier mobility, and stabilize device performance over time. This section will review several studies that demonstrate the effectiveness of PS in enhancing the properties of various organic semiconductors, highlighting its role in improving crystallinity, reducing electronic defects, and optimizing the overall functionality of OTFTs through different mechanisms and processing techniques. Figure 2 shows the molecular structures of (a) PS polymer additive, (b) pentacene, (c) rubrene, (d) TIPS pentacene, (e) diF-TESADT, and (f) C₈-BTBT, which are discussed as the benchmark semiconductors in this section.

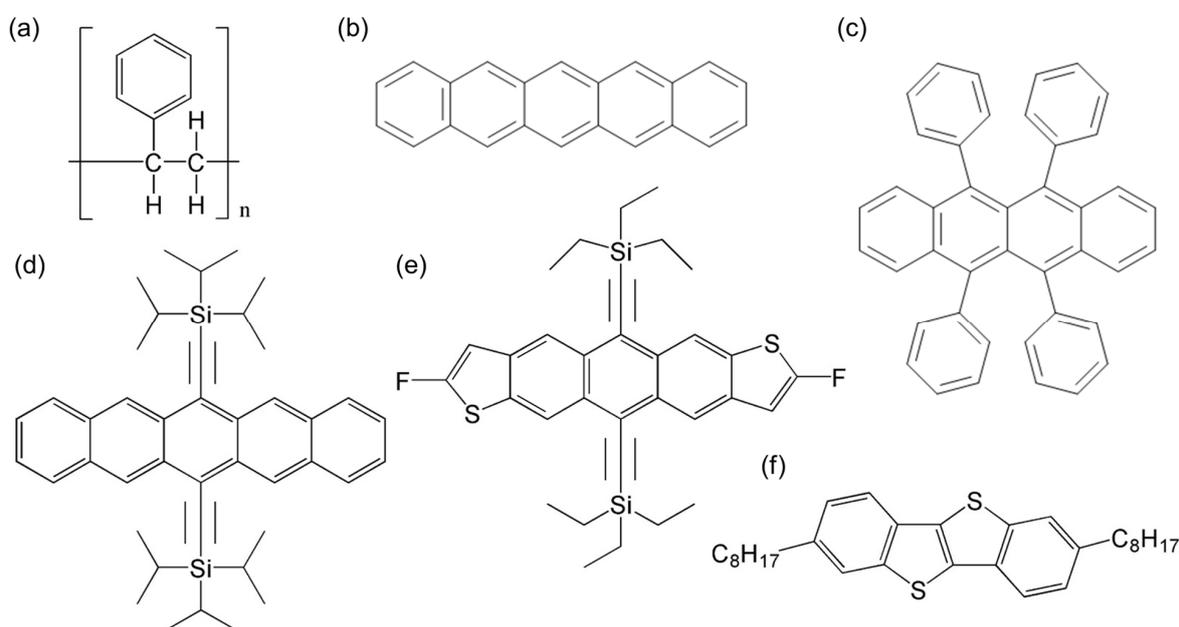


Figure 2. Molecular structures of (a) PS polymer additive, and of various organic benchmark semiconductors discussed in this review, including (b) pentacene, (c) rubrene, (d) TIPS pentacene, (e) diF-TESADT, and (f) C₈-BTBT.

3.1. PS Mixing with Pentacene

Pentacene is a widely studied organic semiconductor composed of five benzene rings fused in a linear arrangement [266–270]. Pentacene is frequently utilized in OTFTs due to its good field-effect mobility and efficient π - π stacking, which promote effective charge carrier movement. Myny et al. reported the solution deposition of PS (Mw 700 K) polymer as a surface treatment material for pentacene-based thin-film transistors [271]. In this work, self-assembled monolayers (SAMs) of 3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,10-heptadecafluoro-1-decanethiols were deposited onto the gold contact electrodes. PS was spin coated onto the gate dielectric layer in toluene and then baked for drying out at 120 °C. A control device comprising an octadecyltrichlorosilane (OTS) treatment was fabricated. Atomic force microscopy (AFM) imaging results revealed a large grain of pentacene on the PS layer but a relatively much smaller grain on the SAM-treated gold contacts. Electrical characterization showed that while the control device had an onset voltage of 3.7 V, the PS-based thin-film transistor exhibited an onset voltage of 0.3 V, indicating a negligible number of electrons were trapped at the charge transport interface between the organic semiconductor pentacene and PS polymer layer. As compared to a lower mobility of 0.294 cm²/Vs from

the control device, the PS-based thin-film transistor exhibited an enhanced hole mobility of $0.44 \text{ cm}^2/\text{Vs}$, which was attributed to the reduced electronic defects at the smooth polymeric interface.

Wang et al. studied the impact of the phenyl ring orientation of PS (Mw 280 K) on the charge transport of pentacene-based thin-film transistors [255]. The tilting angle of untreated PS film and of PS film treated at an elevated temperature of 80°C and 120°C exhibited a tilting angle of 27° , 39° , and 62° , respectively. A larger tilting angle indicates a flatter orientation of the phenyl ring at the surface, indicating that the rings are oriented more towards the substrate surface. Accordingly, the optimized surface energy of PS becomes a good match with that of pentacene. X-ray diffraction (XRD) results indicated that the peak intensities increase with annealing temperature, pointing to enhanced crystallinity of pentacene. The pentacene thin-film transistor-based on the PS film treated at 120°C demonstrated a hole mobility of $4 \text{ cm}^2/\text{Vs}$ as well as a high on/off current ratio of $10^7\sim 10^8$. The enhanced charge-carrier mobility of pentacene was attributed to a combined effect of higher crystallinity, larger grain size, and enhanced interconnection.

Jung et al. utilized the PS polymer additive (Mw 48 K) along with a “scanning corona-discharge coating (SCDC)” method to grow ultrathin TIPS pentacene crystals [256]. In this work, a voltage was applied to a sharp tip adjacent to the substrate, which induced corona discharge that interacted with the anode and shifted towards the electrode. The momentum transfer from the ionized gases to the surrounding gases caused a directional flow of ionized gas molecules, known as an electric wind [272,273]. As the wetting condition of the TIPS pentacene solution was enhanced due to the directional electric wind, its driving force allowed the preferential growth of uniform thin crystals with a thickness between 50 nm and 200 nm. The crystals were aligned in a parallel orientation with the scanning direction of the SCDC. As compared with the pristine semiconductor, the incorporation of PS as a polymer additive was observed to greatly reduce the film roughness. Additionally, the different solubility between TIPS pentacene and PS caused a phase segregation in the vertical profile, resulting in a top semiconductor and bottom polymer bilayer structure. Thin-film transistors were fabricated comprising different weight ratios of the PS additive. The highest mobility of $0.23 \text{ cm}^2/\text{Vs}$ was obtained with 10% loading of PS, whereas an elevated content of PS caused a larger PS thickness in contact with the contact electrodes, increased the contact resistance, and thereby reduced the mobility.

Huang et al. reported the effect of UV ozone treatment on the dielectric property of PS polymer (Mw 280 K) for application in pentacene-based thin-film transistor fabrication [257]. Different UV ozone treatment time was tested on the PS polymer surface which ranged from 0 s to 240 s. The UV ozone treatment can clean the dielectric surface of PS and reduce the amount of trap sites of charge carriers. The AFM imaging indicated a flat surface for these PS dielectric layers around 270 pm. For all treatment time, similar capacitance value of $4.5 \text{ nF}/\text{cm}^2$ was measured at 100 kHz, and low leakage current between $10^{-10}\sim 10^{-9} \text{ A}$ was obtained, implying that the UV ozone treatment does not damage the capacitance and insulation property of the PS dielectric layer. The pentacene organic semiconductor deposited on the PS dielectric layer showed different thin-film morphologies, dependent on the different UV ozone treatment times. In particular, for a short treatment time of less than 60 s, no significant change in the pentacene morphology was observed. For a long treatment time of more than 120 s, the pentacene morphology begins to change drastically. A mobility of up to $0.52 \text{ cm}^2/\text{Vs}$ was demonstrated from the pentacene-based thin-film transistors with UV ozone-treated PS dielectric layers for 5 s.

3.2. PS Mixing with Rubrene

Rubrene, derived from tetracene, is known for its notable photophysical properties and excellent charge-carrier mobility [274–278]. Its molecular structure features four fused benzene rings with attached phenyl groups, leading to robust light absorption and emission. Jo et al. reported the addition of the PS (Mw 100 K) polymer additive, along with poly(4-vinylpyridine) (P4VP) (Mw 60 K), in order to tune the phase segregation and charge

transport of an organic semiconductor rubrene [261]. Each polymer was mixed with rubrene at a ratio of 1:4 by weight in 1,2-dichlorobenzene (o-DCB). The phase segregation of rubrene with PS and subsequent crystal growth can be illustrated by the schematic shown in Figure 3a. Study of the radii of interaction (R_a) between solvent and solute based on the Hansen solubility parameters (HSPs) indicated a more miscible system with addition of PS. Therefore, more residual solvent is expected to remain in the spin-coated rubrene/PS mixture. As the solvent evaporates, it facilitates mobility of the solute rubrene, which migrates towards the interface between the active layer and air. As a result, a vertically phase-segregated film with a top rubrene layer and a bottom PS layer is formed, as shown in Figure 3b. On the other hand, a similar vertical phase segregation was observed in the rubrene/P4VP mixture, as shown in Figure 3c, which can be attributed to the preferential interaction of the hydrophilic P4VP polymer with the hydrophilic substrate surface. Thin-film transistors were fabricated with the rubrene/polymer mixture as active layer (transistor device shown in Figure 3d,e). The addition of PS and P4VP yielded an average mobility of $0.4 \text{ cm}^2/\text{Vs}$ and $0.09 \text{ cm}^2/\text{Vs}$, respectively. This work indicated that the solubility and miscibility as well as surface energy played a vital role in controlling the phase segregation, crystalline microstructure, and charge transport of the organic semiconductor.

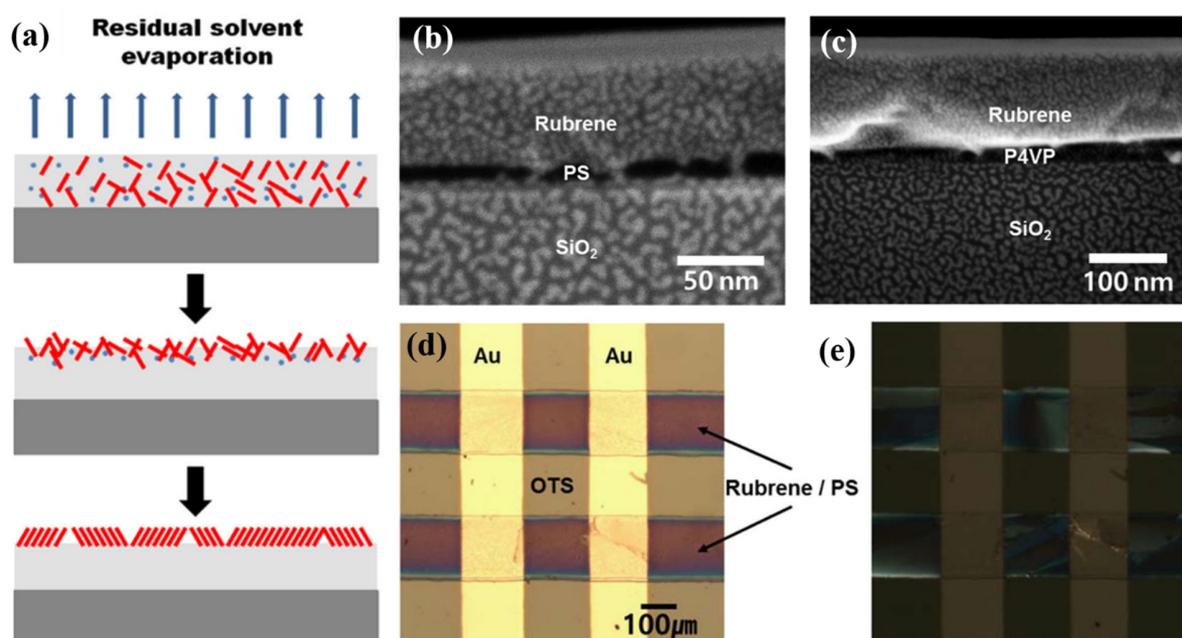


Figure 3. (a) A schematic showing the vertical phase-segregation mechanism between rubrene and PS. The red sticks refer to rubrene and the blue dots represent the solvent; (b,c) shows the cross-sectional SEM image of the vertically phase segregated rubrene film with PS and with P4VP polymer additive, respectively. (d) Optical microscopic image and (e) cross-polarized microscopic image of the as-fabricated thin-film transistor with the rubrene/PS mixture as the active layer and gold (Au) as source and drain contact electrodes. Reproduced from reference [261], with permission from American Chemical Society.

Stingelin-Stutzmann et al. reported the solution-processed rubrene-based thin-film transistor by using a mixing approach [262]. In this work, the mixture system is comprised of four different components, including the organic semiconductor rubrene, a volatile solvent 5,12-diphenylanthracene, a polymer additive PS with high molecular weight, and a “glass-inducing” species. The polymer additive provides good film formation properties and also helps enhance the mechanical properties, whereas the “glass-inducing” species serves as a diluent for the organic semiconductor, hampering crystallization from solution. The thin-film transistor with the four-component mixture demonstrated a saturation mobility of up to $0.7 \text{ cm}^2/\text{Vs}$, a subthreshold slope of 0.5–0.7 V per decade, and an in-

significant hysteresis curve between applying forward and backward voltage scans. These electrical characterization results indicated a very low density of trap sites at the charge transport interface.

Park et al. reported the use of PS as an interfacial layer to modify the topography and charge transport of rubrene [87]. Without the incorporation of a PS interfacial layer, rubrene deposited on the bare silicon dioxide layer exhibited isolated islands with a large thickness variation. In contrast, the film deposited on the PS layer showed smaller islands with a much more uniform thickness. Electrical characterization showed a mobility of $6.8 \times 10^{-5} \text{ cm}^2/\text{Vs}$ and $9.9 \times 10^{-3} \text{ cm}^2/\text{Vs}$ from the rubrene thin-film transistor without and with the inclusion of a PS interfacial layer. Additionally, the hole mobility was found to be independent of the rubrene layer thickness after 50 nm percolation of the rubrene islands. Apart from the hole transport, electron transport with a mobility of $7.9 \times 10^{-5} \text{ cm}^2/\text{Vs}$ was also observed from the rubrene thin-film transistor due to the low density of trap sites on the PS interfacial layer, implying ambipolar performance of the devices.

3.3. PS Mixing with Ph-BTBT-Based Semiconductors

Ph-BTBT-based semiconductors, notable for their exceptional charge transport properties and structural stability, share a common core structure of benzo[thieno[3,2-b]thiophene (BTBT) with phenyl groups and alkyl chains that enhance molecular packing and solubility [279–282]. The combination of phenyl and decyl substituents promotes strong π - π stacking interactions, leading to high charge carrier mobility in OTFTs. These semiconductors are particularly valued for their ability to maintain stable performance under various environmental conditions, making them suitable for a range of organic electronic applications. Park et al. reported the addition of PS brush (Mw 19.5 K) in order to improve the electrical performance of two organic semiconductor blends, composed of a *p*-type 2-decyl-7-phenylbenzo[*b*]benzo [4,5]thieno [2,3-*d*]thiophene and an *n*-type *N,N'*-di-*n*-octyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C8) [88]. PS brush was first coated onto the substrate followed by the formation of the organic semiconductor layer. Two types of device configurations were studied in this work, including a bilayer structure and a bulk-heterojunction (BHJ) structure. The bilayer-structured device based on the thermal evaporation of the semiconductor layers showed low mobility, which was attributed to the poor interface contact between these two layers. In contrast, the BHJ device based on a solution-shearing deposited semiconductor layer demonstrated an enhanced hole and electron mobility of $0.22 \text{ cm}^2/\text{Vs}$ and $0.038 \text{ cm}^2/\text{Vs}$, respectively, which was one order of magnitude higher than the mobility from the bilayer device. The superior device performance of the BHJ device was also attributed to the enlarged grain size as compared to the bilayer structured counterpart. Complementary inverters based on the BHJ-structured OTFTs demonstrated a high voltage gain of 96.

Li et al. reported the fabrication of thin films of the organic semiconductor 7-decyl-2-phenyl[1]benzothieno[3,2-*b*][1]benzothiophene (Ph-BTBT-10) and its blends with three different binding polymers: PS, poly(pentafluorostyrene) (PFS), and poly(methyl methacrylate) (PMMA) [283]. The thin films were characterized using AFM, as shown in Figure 4. The type of binding polymer used results in distinct morphologies for the thin films. For PFS-based films, more incomplete molecular layers are present, leading to a greater number of terraces. Additionally, the crystalline domains in the PMMA blend films are notably smaller compared to those in the other blends. Steps of around $2.9 \pm 0.2 \text{ nm}$ and $5.9 \pm 0.3 \text{ nm}$ in height are observed across all samples, corresponding to extended molecular monolayers and bilayers, respectively. This indicates that the organic semiconductor is crystallizing on the upper surface of the films, consistent with previous observations. In particular, films based on PS demonstrated the best performance, featuring the highest mobility, a threshold voltage (V_{th}) near zero, minimal interfacial traps, and excellent bias stress stability. In contrast, the PMMA blends performed the worst, primarily due to a higher concentration of interfacial hole traps (i.e., majority carriers). Regarding UV photo-response, a different trend was observed; pristine films and PFS blends exhibited

the highest response. This was attributed to the greater density of electron traps (i.e., minority carriers), which enhanced the measured hole current following exciton generation and dissociation.

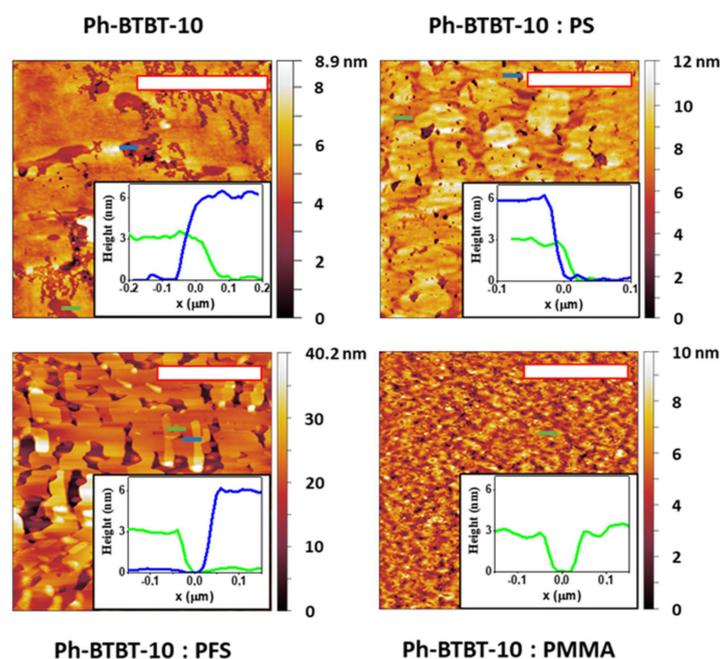


Figure 4. AFM topography photos of Ph-BTBT-10 thin films with and without the various polymer binders, including PS, PFS, and PMMA. The inset shows the height profiles along the blue and green lines marked in the images. These lines represent molecular bilayer and monolayer structures, respectively. The scale bar indicates a length of 2 μm . Reproduced from reference [283], with permission from The Royal Society of Chemistry.

Tamayo et al. reported a solution shearing technique for growing the organic semiconductor Ph-BTBT-10 with the PS additive (Mw 280 K) [263]. When prepared using two deposition speeds of 1 mm/s (low) and 10 mm/s (high), the organic semiconductor consistently crystallized in the bulk phase, adopting a 2D herringbone structure. As shown in the optical images of Figure 5a,b, the Ph-BTBT-10 films prepared at a high shearing speed of 10 mm/s exhibit more uniform coverage without a clear preferential orientation. In contrast, the Ph-BTBT-10/PS mixture film shows slightly larger domain size. The nanoscale morphology of the thin-film surfaces was characterized using AFM, as shown in Figure 5c,d. All films displayed smooth mesoscopic areas with similar nanostructures. Additionally, at a low coating speed, films grew with the a-axis aligned to the coating direction, while films coated at high speed did not show alignment in the ab plane, resulting in isotropic charge transport mobilities. As a result, the Ph-BTBT-10/PS blended films exhibited high mobilities of 1.46 cm^2/Vs .

Suzuki et al. reported using high-speed blade-coating at a rate of 140 mm/s to grow uniform liquid crystalline 2-decyl-7-phenyl[1]benzothieno[3,2-b][1]benzothiophene films incorporating the PS polymer additive [264]. These semiconductor films were produced at temperatures exceeding 50 $^{\circ}\text{C}$, the liquid crystal phase temperature, without encountering issues of uneven recrystallization despite the rapid blade-coating process. Microscopic observations and XRD analysis demonstrated that producing thin films at liquid crystal phase temperatures can result in uniform films without recrystallization, even at high speeds exceeding 100 mm/s. Transistors with the semiconductor/PS polycrystalline thin films, fabricated at these temperatures, displayed uniformity and high mobility of $4.8 \pm 0.35 \text{ cm}^2/\text{Vs}$. The mobility and grain size were found to be isotropic, irrespective of the coating direction. PS with a low trap density phase separated and coated the surface of the gate insulator, resulting in a threshold voltage close to 0 V and enabling low-voltage operation.

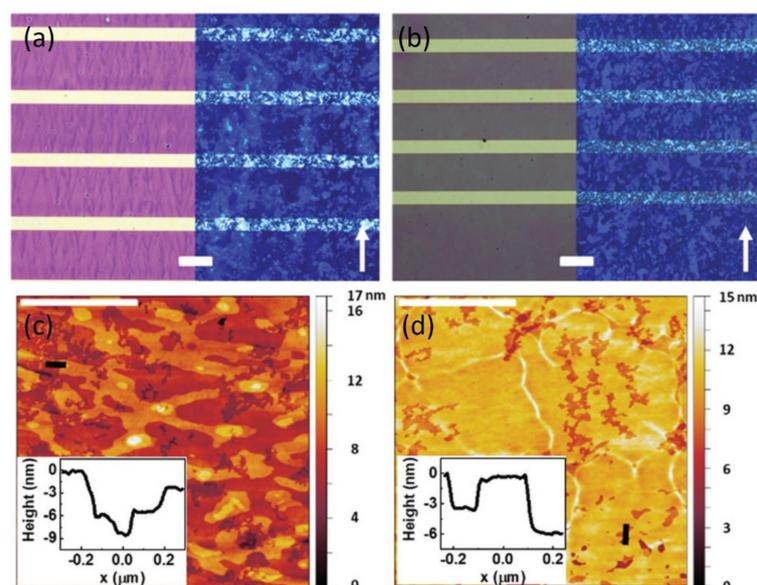


Figure 5. The non-polarized (**left**) and polarized (**right**) microscopy images of (a) pristine Ph-BTBT-10 and (b) Ph-BTBT-10/PS mixed thin films, prepared from PhCl solutions on interdigitated gold electrodes. The scale bar in (a,b) represents 100 μm , and the white arrow shows the shearing direction. AFM topography images of (c) pristine Ph-BTBT-10 and (d) Ph-BTBT-10/PS mixed thin films. The scale bar in (c,d) is 2 μm , with insets displaying the height profiles along the black lines marked in the images. The solution shearing coating speed is at 10 mm/s. Reproduced from reference [263], with permission from The Royal Society of Chemistry.

He et al. reported the addition of PS into a binary small-molecular semiconductor blends composed of 2-phenyl[1]benzothieno[3,2-b][1]benzothiophene (Ph-BTBT) and 2-(4-dodecylphenyl) [1]benzothieno[3,2-b]benzothiophene (C12-Ph-BTBT) [284]. Both the optical images and AFM images indicated that while the pristine Ph-BTBT semiconductor has an inhomogeneous and discontinuous film, the uniformity of the blend was significantly enhanced as a result of the excellent film formation property from the C12-Ph-BTBT component. Moreover, the blend film showed enlarged grain sizes with reduced grain boundaries, which can be favorable for charge transport in the blend film. The polymer PS was further mixed with the Ph-BTBT/C12-Ph-BTBT blend at a ratio of 1:3.06 in order to enhance the charge transport. The addition of PS was found to reduce interfacial trap and defects as well as enhance the inter-grain connectivity. As a result, a highest mobility of 1.5 cm^2/Vs and 2.25 cm^2/Vs was demonstrated from the Ph-BTBT/C12-Ph-BTBT blend-based OTFTs without and with PS polymeric additive, respectively.

3.4. PS Mixing with TIPS Pentacene

TIPS pentacene [285–287] is a soluble derivative of pentacene designed to merge pentacene's high mobility with improved processability. The incorporation of triisopropylsilylethynyl groups increases solubility, enabling solution-based processing techniques while preserving the vital π - π interactions necessary for effective charge transport in OTFTs. Lin et al. studied the thin-film morphology and charge transport of TIPS pentacene organic semiconductor deposited by using a slot-die coating technique [258]. In this work, different polymers, including PS (Mw 35 K), PMMA (Mw 15 K), and PVP (Mw 25 K), were first deposited as a gate dielectric layer. AFM measurements on the polymer dielectric layer indicated a surface root mean square (RMS) roughness of 0.32 nm, 0.39 nm, 0.62 nm, and 0.65 nm for the bare substrate, PS, PMMA, and PVP polymer dielectric layer, respectively. Accordingly, the capacitance was measured to be 2.2 nF/cm^2 , 6.8 nF/cm^2 , and 9.5 nF/cm^2 , for the PS, PMMA, and PVP polymer dielectric layers, respectively. The formation of TIPS pentacene organic crystals was based on a mixture of double solvents, which comprised a poor solvent, anisole, and a good solvent, toluene. The resultant thin-film morphol-

ogy of TIPS pentacene organic crystals based on the bare substrate, PS, PMMA, and PVP polymer dielectric layer was shown in the Figure 6a–c. Excellent crystal alignment has been demonstrated for all types of substrates, and, in particular, the crystals based on the PS polymer dielectric showed an enlarged crystal size, indicating lower amounts of charge carrier traps. The out-of-plane XRD patterns for the TIPS pentacene crystalline film deposited on the different polymer dielectrics was shown in Figure 6e. The strongest (001) intensity was observed for the TIPS pentacene film based on the PS dielectric surface. TIPS pentacene-based thin-film transistors show an average mobility of $4.2 \text{ cm}^2/\text{Vs}$, $2.4 \text{ cm}^2/\text{Vs}$, and $1.28 \text{ cm}^2/\text{Vs}$ based on PS, PMMA, and PVP polymer dielectric, respectively, as well as and a mobility of $6.5 \text{ cm}^2/\text{Vs}$ based on the PS dielectric (Figure 6f). Figure 6g shows the charge-carrier mobility of a TIPS pentacene thin-film transistor based on the PS dielectric, as a function of different coating speeds.

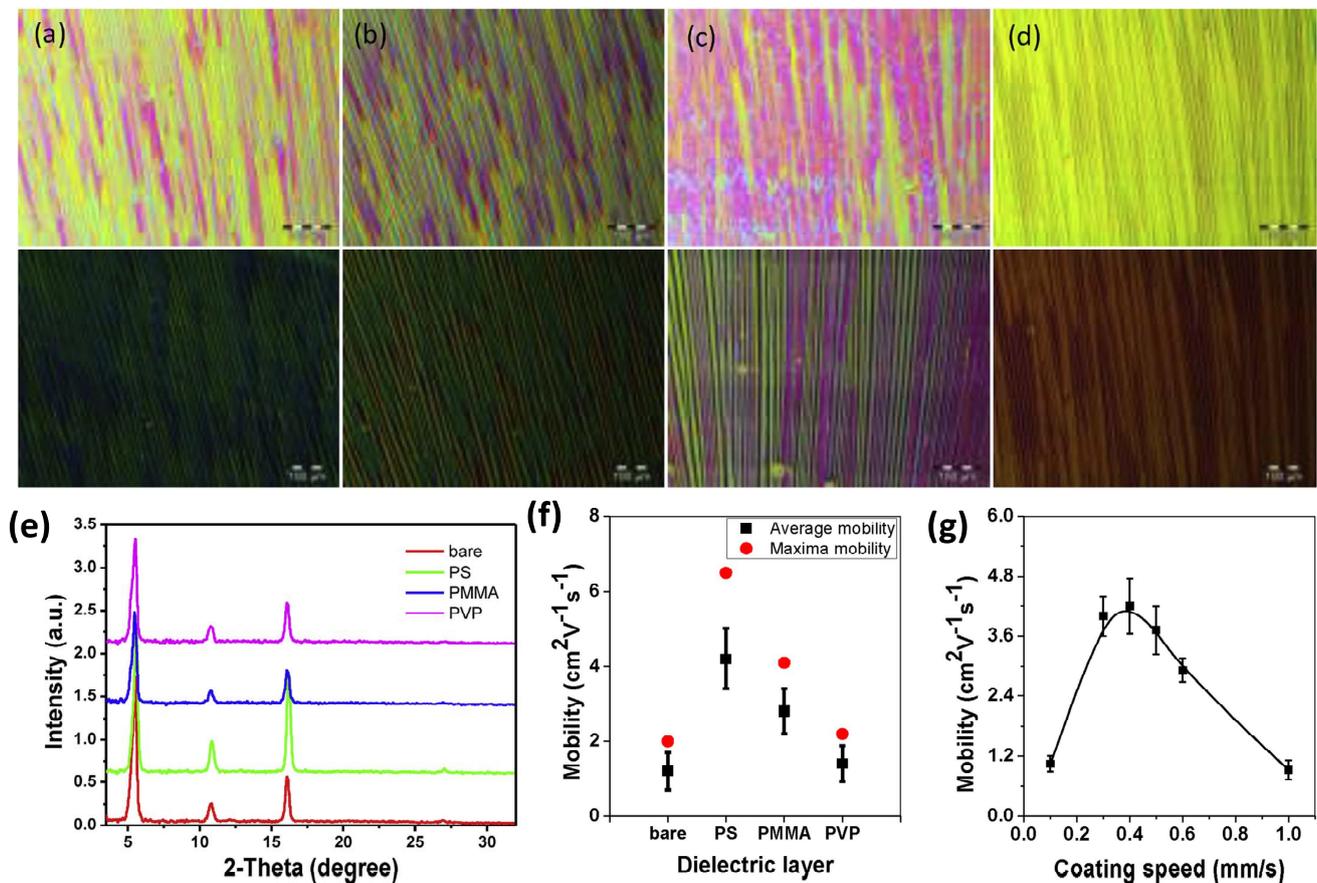


Figure 6. Polarized optical microscopic images of TIPS pentacene organic semiconductor deposited on (a) bare substrate, (b) PS, (c) PMMA, and (d) PVP polymer without and with polarizer. (e) Out-of-plane XRD patterns for the TIPS pentacene crystalline film based on the different polymer dielectrics. (f) The average and maximal charge-carrier mobility with different polymer dielectrics. (g) The charge-carrier mobility of TIPS pentacene organic semiconductor based on the PS dielectric, as a function of different coating speeds. Reproduced from reference [258], with permission from Elsevier.

Feng et al. reported the mixing of TIPS pentacene with PS for fabricating all inkjet-printed low-voltage thin-film transistors on flexible substrates [259]. The flexible transistor device is comprised of a cross-linkable PVP polymer layer as the gate dielectric, the TIPS pentacene/PS mixture as the active layer, and a CYTOP layer as the encapsulation layer. The organic semiconductor and polymer mixture was believed to induce a vertical phase segregation, which further resulted in better semiconductor crystallization and a reduced interface trap density (N_{SS}). The device exhibited a hole mobility of $0.26 \text{ cm}^2/\text{Vs}$, a low

threshold voltage of -0.17 V, and a N_{SS} value of $3.7 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. The low-voltage operation of the thin-film transistor was attributed to the enlarged dielectric capacitance and reduced N_{SS} .

Lada et al. reported the mixing of PS (Mw 350 K) with TIPS pentacene in order to enhance the crystal morphology and tune the mobility of the organic semiconductor [260]. Additionally, a double-solvent scheme was employed in this work to tune the crystallization. Hansen solubility parameters of the solute and solvent were considered in order to choose the compatible solvents for TIPS pentacene. In particular, anisole is considered a compatible solvent for PS but a poor solvent for TIPS pentacene, whereas mesitylene is a compatible solvent for TIPS pentacene. Without the double solvent, TIPS pentacene dissolved in a single solvent of mesitylene grew into a small crystalline size as a result of relatively small mobility of the PS polymer chain in the solvent that restricts the semiconductor migration during crystallization. At a 1:1 mixing ratio of TIPS pentacene and PS in the double solvent of anisole and mesitylene, a saturation mobility of $1.16 \text{ cm}^2/\text{Vs}$ was obtained, which was attributed to the enlarged crystallite size due to the addition of anisole. In addition, at a 3:1 mixing ratio of TIPS pentacene and PS, a larger saturation mobility of $1.82 \text{ cm}^2/\text{Vs}$ was demonstrated as a result of reduced surface roughness as well as enlarged crystal domains.

Bharti et al. reported the mixing of PS (Mw 280 K) with TIPS pentacene for fabricating thin-film transistors with enhanced electrical stability [90]. The resultant mixture film is comprised of a tri-layer structure with a TIPS pentacene film in the top, a PS film in the middle, and, again, a TIPS pentacene film in the bottom. For thin-film transistors without incorporating the PS additive, the devices suffered from a monotonic 80% decrease in the saturation current measured under a constant bias stress, which was caused by the charge trapping sites on the hydrophobic silicon dioxide gate dielectric. In comparison, the counterparts based on the TIPS pentacene/PS mixture exhibited a much lower 30% decay of saturation current due to the passivation effect of the hydroxyl group's free PS layer on the silicon dioxide surface. Accordingly, a hole mobility of up to $0.2 \text{ cm}^2/\text{Vs}$ and $2.6 \text{ cm}^2/\text{Vs}$ were obtained from the TIPS pentacene thin-film transistors without and with the PS polymer additive, respectively.

3.5. PS Mixing with diF-TES-ADT

DiF-TES-ADT is a high-performance organic semiconductor recognized for its stability and substantial field-effect mobility [288,289]. The addition of fluorine atoms and triethylsilylethynyl groups enhances the crystallinity and charge transport properties of the anthradithiophene core, making it an excellent choice for OTFTs and other organic electronic devices. Salzillo et al. reported solution-sheared organic thin-film transistors made from diF-TES-ADT blended with four distinct polymer binders (PS with Mw of 10 K and 100 K, and PMMA with Mw 25 K and 120 K) [290]. Blends incorporating PMMA result in films with a rougher texture and smaller crystalline domains compared to those made with PS blends. Electrically, the best performances were observed in the PS blends, which exhibited improved mobility exceeding $1 \text{ cm}^2/\text{Vs}$ and reduced hysteresis. This is attributed to the less polar nature of PS, which minimizes charge trapping. Regarding molecular weight, while minor differences were noted in the PMMA films, a significant increase in mobility was seen in the lower molecular weight PS films. Therefore, the differences in electrical performance are likely due to morphological factors, such as film smoothness, homogeneity, and crystalline domain sizes, influenced by the interactions between the organic semiconductor and the polymer as well as the interfaces during the crystallization process. The results from this work shed light on how the type of polymer binder and its molecular weight affect the morphology of the thin films and the performance of the devices.

Naden et al. reported the nucleation and growth mechanisms that result in four distinct structural regimes of the diF-TES-ADT semiconductor film [288]. These regimes are formed due to the 'natural length scales' of growth determined by five key kinetic parameters: the heterogeneous nucleation rate on electrodes, the crystal growth rate, the solvent evaporation rate, the diffusion rate of organic semiconductors (OSC) in the solvent, and the

homonucleation rate. In this work, the active layer was formed by spin-casting a mixture of diF-TES-ADT and an insulating, amorphous PS-based polymer binder. Figure 7a presents a magnified, polarized optical micrograph taken from the center of the channel in a typical diF-TES-ADT transistor device. Figures 7b, 7c and 7d display the AFM topography, the scanning Kelvin probe microscopy (KPM) surface potential, and the gradient of the surface potential, respectively. A comparison between the polarized optical and AFM images easily identifies the boundaries separating the domains, with some domain ends adorned with needle-shaped crystallites. The contour map of the KPM surface potential in Figure 7c illustrates a connection between the topography and electrical performance, revealing a gradual potential drop across the channel influenced by the domain boundaries. Figure 7d depicts the gradient of the surface potential derived from the KPM data, which emphasizes all the domain boundaries, especially in regions with needle-like protrusions shown in Figure 7b. As a result, devices achieving a peak saturation mobility of $1.5 \text{ cm}^2/\text{Vs}$ and a maximum current modulation ratio ($I_{\text{on}}/I_{\text{off}}$) of 1.20×10^5 are examined through atomic force microscopy, revealing excellent domain connectivity and aligned crystallography across the channel. Conversely, underperforming devices often exhibit a phase change in semiconductor crystallinity at the channel center.

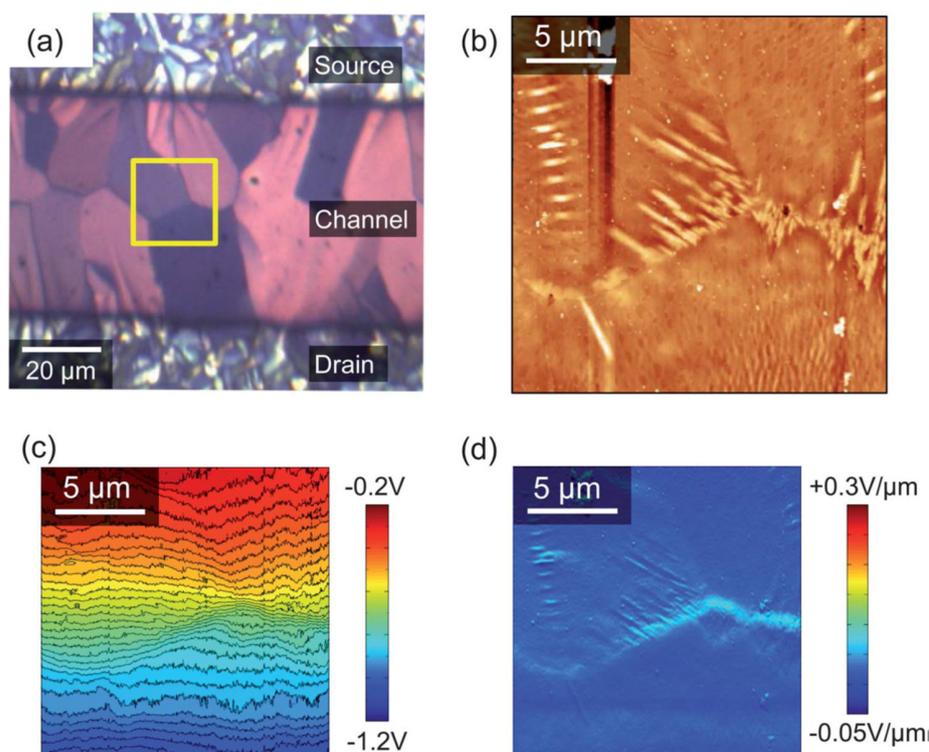


Figure 7. (a) Displays a polarized optical micrograph of a typical diF-TES-ADT transistor device's channel. (b) AFM topography within the yellow box from (a), highlighting the domain boundaries and needle-like crystallites. (c) Contour map of the surface electrical potential measured via KPM. (d) Depicts the potential gradient calculated from (c) along the fast-axis scan direction and perpendicular to the electrodes. Reproduced from reference [288], with permission from The Royal Society of Chemistry.

Niazi et al. introduced an approach of utilizing blade-coating of a blend of conjugated small molecule diF-TES-ADT and amorphous insulating polymers (PS and P α MS) for achieving mobilities comparable to single crystals [291]. The resultant bilayer structure consists of an ultrathin, approximately 10 nm thick single-crystal-like diF-TES-ADT layer on top, with the polymer beneath. The PS polymer in the diF-TES-ADT blend acts as a binder, improving the organic semiconductor's long-range lamellar order, phase separation,

and overall device performance by reducing the interfacial trap density. They consistently demonstrate high carrier mobility of $6.7 \text{ cm}^2/\text{Vs}$ over a broad range of processing conditions, with exceptional merits such as an on-off ratio exceeding 10^6 , a low threshold voltage of 0.1 V, and a low subthreshold swing of 0.3 V/decade. The exceptional mobility is evident when analyzing and contrasting polarized optical and AFM images of the pure film of diF-TES-ADT with those of the low-Mw (2.2 K) and high-Mw (900 K) blends. The micrographs show significantly larger domains forming in the high-Mw blend compared to the neat diF-TES-ADT or low-Mw blends. The optimal films display a smoother topography, are free of cracks, and exhibit well-defined domains and grain boundaries, as highlighted by the AFM analysis.

3.6. PS Mixing with C₈-BTBT

C₈-BTBT is an organic semiconductor praised for its outstanding charge transport capabilities and significant thermal stability [292–294]. The BTBT core, paired with octyl side chains, encourages strong π - π stacking and improved solubility, resulting in high mobility within OTFTs. Shen et al. reported the addition of PS (Mw 3.5 K) into C₈-BTBT in order to tune the phase segregation, modify the charge transport interface, and improve mobilities [200]. PS was mixed with C₈-BTBT at different weight ratios, including 10:1, 5:1, and 2:1. As shown in the polarized optical images of Figure 8a and AFM images of Figure 8c, the addition of PS successfully eliminated the issue of C₈-BTBT de-wetting and the formation of pin holes. In particular, at 5:1 loading, the blend film exhibited a smooth thin-film morphology with an enlarged domain size. In contrast, the blend film showed a rough 10:1 surface ratio and increased grain boundaries at 2:1 loading. Highest peak intensity was observed from the blend film at a 5:1 ratio, according to the XRD spectra (Figure 8b), indicating enhanced film crystallinity. XPS was employed to investigate the film composition of the C₈-BTBT/PS blends, which revealed a vertically segregated bilayer structure with a top C₈-BTBT film and a bottom PS layer. Additionally, the spin-coating speed was demonstrated as a critical parameter that can significantly impact the film structure and charge transport. In particular, a high spin-coating speed of between 3 Krpm and 6 Krpm can attribute to greater than one order of magnitude enhancement in the mobilities as compared to a low speed of below 3 Krpm. The maximum mobility of $6.8 \text{ cm}^2/\text{Vs}$ and an on/off current ratio greater than 10^7 were demonstrated from the C₈-BTBT/PS blend-based OTFTs with a 5:1 loading ratio, which was attributed to the enlarged domain size, reduced grain boundary, and smooth phase-separated interface.

Shen et al. reported the use of a pre-deposited PS layer (Mw 3.5 K) and PMMA layer (Mw 996 K) in order to tune the crystallization and charge transport of the C₈-BTBT organic semiconductor [265]. In this work, the C₈-BTBT/PMMA mixture was deposited onto a pre-deposited polymer layer including PMMA and PS. The organic semiconductor/polymer mixture deposited on both the pristine silicon dioxide layer and the re-deposited PMMA layer exhibited wide grain boundaries, whereas the counterpart deposited on the PS pre-deposited polymer layer showed more uniform grains without visible boundaries. C₈-BTBT-based thin-film transistors were fabricated, and a highest hole mobility above $7 \text{ cm}^2/\text{Vs}$ was demonstrated from the devices with the pre-deposited PS layer. The enhanced electrical performance of thin-film transistors was attributed to the improved crystallization of the C₈-BTBT organic semiconductor and also to the modification of the charge transport interface with reduced crystalline defects and trap centers.

Huang et al. studied how the PS additive improved the film topography and charge transport of spin-coated C₈-BTBT crystalline film [295]. Two different spin-coating configurations were employed in this work, including center spin coating and off-center spin coating, as illustrated in Figure 9g,h. Two different spin speeds of 3 Krpm and 5 Krpm were used for center spin coating. For the off-center spin coating, different spin profiles were used, as shown in Figure 9i. In particular, the ramping up speed gradually increases for the spin profiles A, B, C, and D. The resultant film topography corresponding to each spin-coating condition is shown in Figure 9a–f. The incorporation of PS into C₈-BTBT yielded

continuous large crystalline film based on off-center spin coating, and the lowest RMS of 3.65 nm was obtained from Figure 9d, corresponding to speed B. XPS results indicated a vertical phase segregation between C₈-BTBT and PS, and PS moved towards the substrate and formed a smooth interface with reduced trap sites of charge carriers. An enhanced mobility of 3.56 cm²/Vs was demonstrated from the C₈-BTBT/PS thin-film transistors based on the spin-coating profile B.

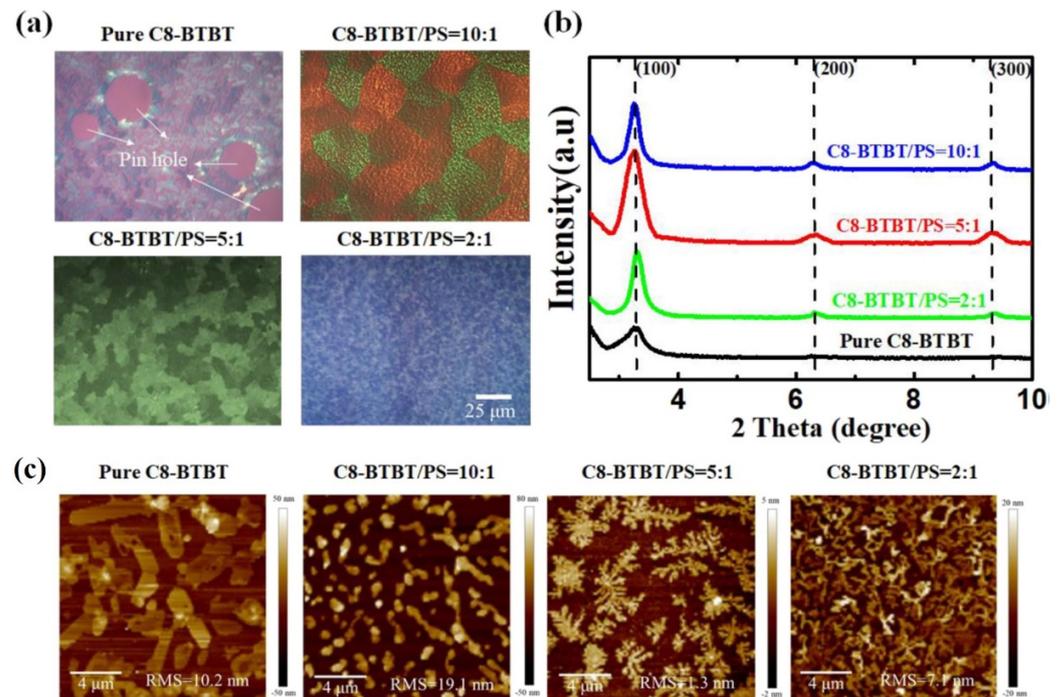


Figure 8. (a) Polarized optical images of C₈-BTBT/PS blend films with different weight ratios. The corresponding (b) XRD spectra and (c) AFM images. All types of films were based on the spin-coating speed of 5 Krpm. Reproduced from reference [200], with permission from Elsevier.

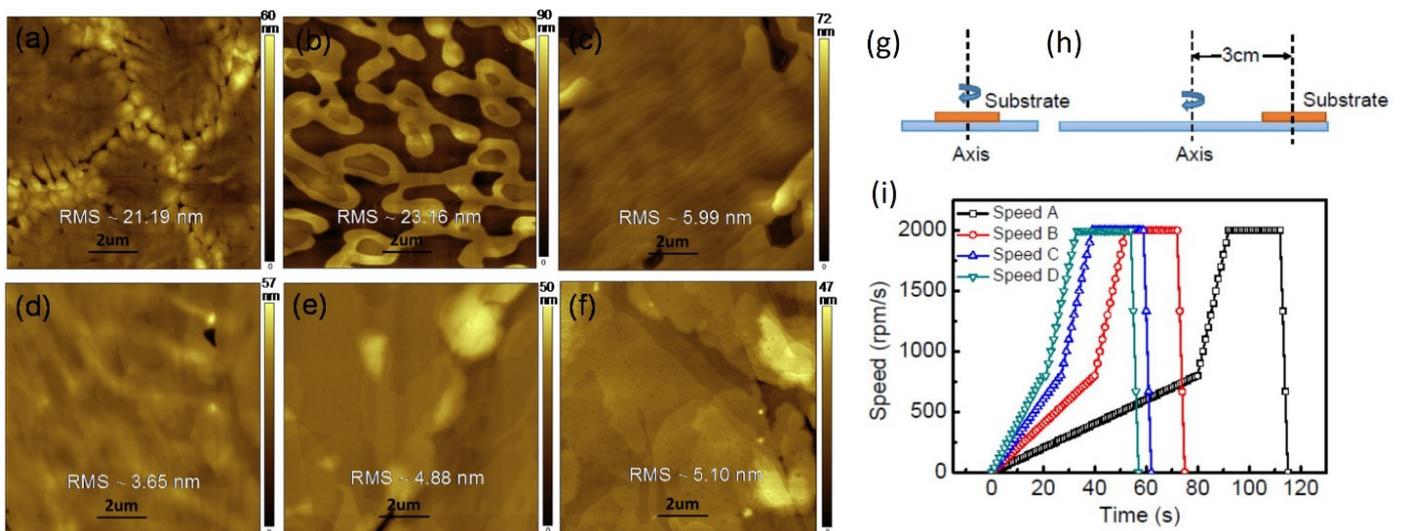


Figure 9. AFM images of C₈-BTBT/PS crystalline films based on (a,b) center spin coating at 3 Krpm and 5 Krpm, respectively; (c–f) off-center spin coating with different spinning speeds corresponding to the curves indicated in (i); (g,h) show the schematic of center spin coating and off-center spin coating, respectively. Reproduced from reference [295], with permission from Elsevier.

Table 1. Summary of the different works reviewed in this section, including the author, the different benchmark organic semiconductors, molecular weight of the PS polymer additive, experiments and results, as well as the charge-carrier mobility.

Author	Material	PS M_w	Result	Mobility
Myny et al. [271]	Pentacene	700 K	PS was coated as a surface treatment on the gate dielectric to form a smooth polymeric interface with reduced electron defects	Enhanced hole mobility of $0.44 \text{ cm}^2/\text{Vs}$
Wang et al. [255]	Pentacene	280 K	Thermal annealing of PS changes the phenyl ring orientation, morphology, and charge transport of pentacene	$4 \text{ cm}^2/\text{Vs}$ at 120°C annealing of PS
Jung et al. [256]	Pentacene	24 K	PS mixed with TiO_2 -PS to tune the permittivity of the gate dielectric layer	$1.3 \pm 0.4 \text{ cm}^2/\text{Vs}$ with 100% TiO_2 -PS
Huang et al. [257]	Pentacene	280 K	Effect of UV ozone-treated PS on morphology and charge transport was studied	$0.52 \text{ cm}^2/\text{Vs}$ with 5 s UV ozone treatment
Jo et al. [261]	Rubrene	100 K	PS with mixture with rubrene to control the vertical phase segregation, microstructure, and mobility	Average mobility of $0.4 \text{ cm}^2/\text{Vs}$ with the PS additive
Stingelin-Stutzmann et al. [262]	Rubrene	Not reported	PS provides good film formation properties and also helps enhance the mechanical properties	Up to $0.7 \text{ cm}^2/\text{Vs}$
Park et al. [87]	Rubrene	Not reported	PS served as an interfacial layer to modify the topography and charge transport of rubrene	Hole mobility up to $9.9 \times 10^{-3} \text{ cm}^2/\text{Vs}$
Park et al. [88]	Ph-BTBT based semiconductors	19.5 K	The <i>p</i> -type and <i>n</i> -type blends based on the PS brush and a BHJ structure showed enlarged grain size	Hole and electron mobility of $0.22 \text{ cm}^2/\text{Vs}$ and $0.038 \text{ cm}^2/\text{Vs}$
Li et al. [283]	Ph-BTBT based semiconductors	Not reported	PS results in the highest mobility, near-zero threshold voltage, minimal interfacial traps, and excellent bias stress stability.	Not reported
Tamayo et al. [263]	Ph-BTBT based semiconductors	280 K	PS blending and coating speed significantly influence the crystallinity, morphology, and electrical properties of Ph-BTBT-10	$1.46 \text{ cm}^2/\text{Vs}$
Suzuki et al. [264]	Ph-BTBT based semiconductors	Not reported	PS with a low trap density phase separated and coated the surface of the gate insulator, enabling low-voltage operation.	$4.8 \text{ cm}^2/\text{Vs}$
He et al. [284]	Ph-BTBT based semiconductors	Not reported	PS additive reduced interfacial traps and enhanced the inter-grain connectivity	Up to $2.25 \text{ cm}^2/\text{Vs}$ from Ph-BTBT/C12-Ph-BTBT OTFTs
Lin et al. [258]	TIPS pentacene	35 K	PS was mixed with TIPS pentacene to align crystal growth with a slot-die coating technique	An average mobility of $4.2 \text{ cm}^2/\text{Vs}$
Feng et al. [259]	TIPS pentacene	Not reported	PS was blended with TIPS pentacene to induce phase segregation and better crystallization with reduced interface traps	$0.26 \text{ cm}^2/\text{Vs}$
Lada et al. [260]	TIPS pentacene	350 K	PS was mixed with TIPS pentacene in double solvents to tune crystal morphology and mobility	$1.82 \text{ cm}^2/\text{Vs}$ at 3:1 mixing ratio
Bharti et al. [90]	TIPS pentacene	280 K	The vertically phase-segregated PS polymer passivated the charge trapping sites on the silicon dioxide gate surface, contributing to enhanced electrical stability	$2.6 \text{ cm}^2/\text{Vs}$ with the PS polymer additive
Salzillo et al. [290]	diF-TES-ADT	10 K, 100 K	PS with different M_w led to varying film smoothness, homogeneity, and crystalline domain sizes during crystallization	Above $1 \text{ cm}^2/\text{Vs}$
Naden et al. [288]	diF-TES-ADT	Not reported	PS was mixed as polymer binder to study the growth mechanisms of diF-TES-ADT and resulted in four distinct structural regimes.	$1.5 \text{ cm}^2/\text{Vs}$
Niazi et al. [291]	diF-TES-ADT	2.2 K, 900 K	PS acts as a binder, improves the long-range lamellar order, and reduces the interfacial trap density	$6.7 \text{ cm}^2/\text{Vs}$
Shen et al. [200]	C_8 -BTBT	3.5 K	PS was pre-deposited to modify the crystallization and charge transport of C_8 -BTBT	Above $7 \text{ cm}^2/\text{Vs}$
Shen et al. [265]	C_8 -BTBT	3.5 K	Vertically segregated bilayer structure with a top C_8 -BTBT and a bottom PS layer	Up to $6.80 \text{ cm}^2/\text{Vs}$ from C_8 -BTBT/PS blend based OTFTs
Huang et al. [295]	C_8 -BTBT	Not reported	PS was mixed with C_8 -BTBT to improve spin-coated film topography	$4.56 \text{ cm}^2/\text{Vs}$

4. Conclusions and Outlook

In this review, we have discussed the major challenges faced by organic semiconductors, such as low charge-carrier mobility, environmental degradation, difficulties in achieving uniform thin-film morphology and crystallinity, poor interface quality, and scalability and reproducibility issues. The integration of PS into these systems has proven to be an effective strategy for addressing these challenges. PS has been shown to enhance

film morphology, improve crystallinity, and optimize molecular alignment, which leads to improved performance, stability, and scalability in OTFTs and other semiconductor devices. These improvements reduce charge trapping, mitigate environmental degradation, and ensure more consistent device fabrication, thereby overcoming key barriers to large-scale production. By focusing on various benchmark semiconductors such as pentacene, rubrene, TIPS pentacene, diF-TES-ADT, and C₈-BTBT, we have demonstrated the versatility of PS in enhancing the overall material properties and device performance. These results highlight the significant impact of PS as a polymer additive in advancing the field of organic electronics, paving the way for the broader implementation of organic semiconductors in next-generation electronic devices.

Further research is needed to explore the full potential of PS and other polymers in organic electronics, particularly in the context of emerging materials and device architectures. As the field continues to evolve, the development of new polymer-based strategies to enhance the performance and reliability of organic semiconductors will be crucial. By continuing to refine these approaches, the broader adoption of organic electronic devices in commercial applications, such as flexible displays, wearable technologies, and energy harvesting systems, is likely to become increasingly feasible. The insights gained from this work provide a solid foundation for future advancements in the design and manufacture of high-performance, stable organic semiconductor devices.

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