Article

Modified SPWM Control for a Single-Stage Differential Boost Inverter Applied in a BESS

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Abstract: This study aims to implement a single-stage differential boost inverter (SSDBI) applied in a single-stage battery energy storage system (BESS) topology that can supply power from a lower-voltage battery module to an alternating current (AC) load. Compared with the common two-stage topology, which has a two-stage converter and higher-voltage battery module array, the single-stage topology can reduce the number of cells and components and improve the power density. In addition, a modified sinusoidal pulse-width modulation (SPWM) control was proposed to reduce the control complexity of the SSDBI while improving the total harmonic distortion (THD) of the inverter. The modified SPWM control can reduce the duty ratio of the SSDBI and the stress on the components in order to improve the AC voltage output waveform and reduce the THD.

Keywords: boost inverter; modified SPWM; differential inverter

1. Introduction

Nowadays, the technology of inverters has been increasingly developed because they are widely used in numerous applications, such as in PV and power grids. Inverters and battery storage systems are some of the most popular combinations. The inverter plays an important role in a BESS, where the inverter is responsible for the energy transmission. Figure 1 shows the most familiar block diagram of a BESS, which includes a battery module array, a battery charger, and an inverter [1–3]. First, the AC source (utility power) can charge the battery pack through the battery charger. Next, the inverter can extract the energy from the battery pack to the AC load. Finally, the battery pack is responsible for the whole power supply when the AC source is removed.
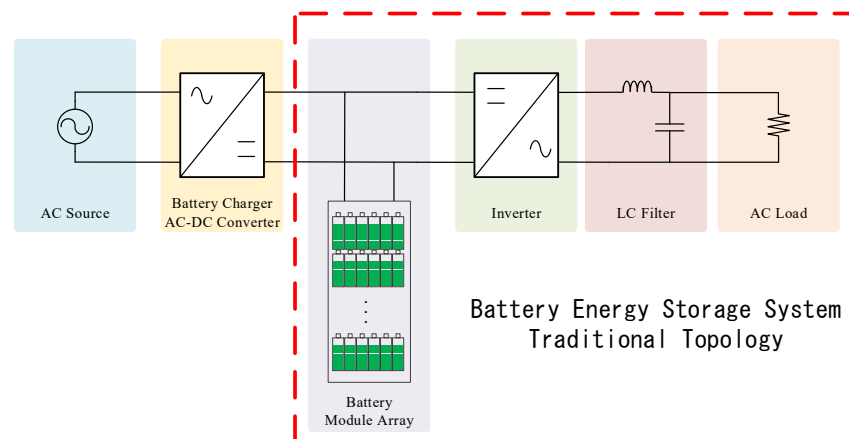

Figure 1. A block diagram of a BESS with a battery charger.

However, it does not make economic sense to use the BESS structure shown in Figure 1. The first reason is that a single cell's voltage is quite low. For example, the voltages of lead–acid, Ni-Cd, and lithium-ion batteries are 2.0, 1.2, and 3.7 V, respectively. A common BESS also needs high voltage, such as 380–400 V_{dc}, for the inverter to supply power to the AC load. Under this condition, the battery module array should be composed of numerous cells connected in series. A high-voltage battery module array will also lead to another problem, which is the cell state of charge (SOC) imbalance. If the imbalance problem occurs, some of the cells will be overcharged or over-discharged as a result of long-term work. Their state of health (SOH) will also decrease, and can even be permanently damaged [4–6]. Furthermore, the battery management system (BMS) will be more difficult, more expensive, and more dangerous when the battery module array's voltage becomes higher.

To overcome the aforementioned problem, the two-stage topology has been proposed [7,8]. The structure includes a battery module, a DC-DC converter, an inverter, DC bus capacitors, and AC load, as shown in Figure 2. The topology uses a battery module with an additional DC-DC boost converter instead of a high-voltage battery module array. However, large DC bus capacitors are a must for these topologies in order to connect the DC-DC converter with the inverter. Compared with the traditional topology, the two-stage topology is easy to implement and has quite mature technology in spite of the number of the components, their short lifetime, and large size.
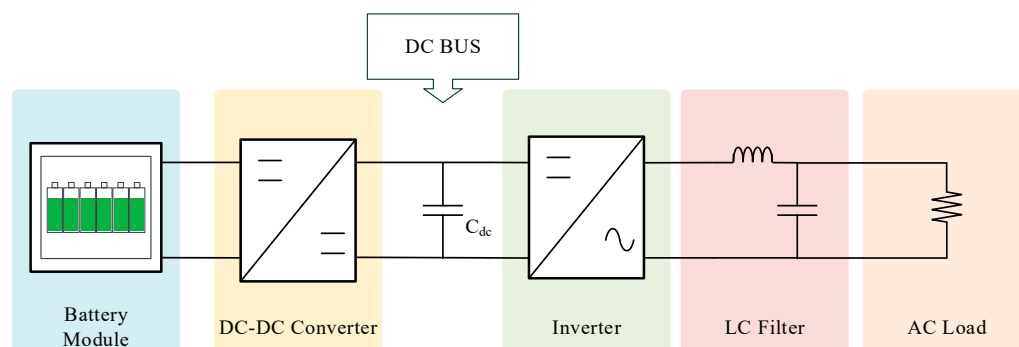

Figure 2. The traditional topology of a BESS.

Figure 3 displays the Pseudo DC-link topology, which includes a low-voltage battery module, DC-DC converter, inverter, and AC load [9,10]. The difference between the two-stage topology and Pseudo DC-link topology is the switch operation of the DC-DC converter. The switching control signal of the DC-DC converter in the Pseudo DC-link topology is based on sinusoidal pulse width modulation (SPWM) instead of traditional pulse width modulation (PWM). Therefore, in the Pseudo DC-link topology, the output of the DC-DC converter and the input of the inverter are a rectified sinusoidal waveform. The topology can convert the low voltage of the battery module into a rectified sinusoidal waveform with the DC-DC converter. The voltage of the rectified sinusoidal waveform is high enough for the inverter to supply power to the AC load. The Pseudo DC-link topology can overcome the need for large capacitors in the traditional two-stage topology. In addition, the operation efficiency of the inverter will increase because of the switching frequency reduction. Nevertheless, the Pseudo DC-link topology is still a two-stage topology in which plenty of the components are the same as those in the traditional two-stage topology.

For further improvement, the single-stage topology was proposed by recent research to minimize the components used [11,12]. Figure 4 shows the single-stage topology, which includes a battery module, a single-stage inverter, and an AC load. The single-stage inverter has good performance in adjusting the voltage and gives an AC output instead of a DC-DC converter and inverter combination. Compared with the two-stage topology, the single-stage inverter in the single-stage topology is not mature enough and is too complicated to implement.
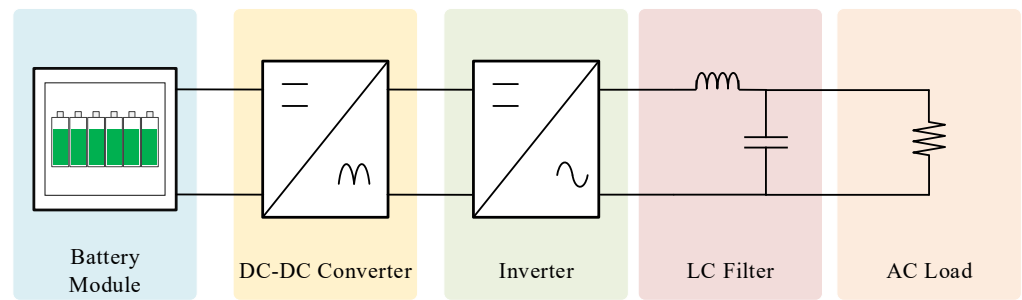
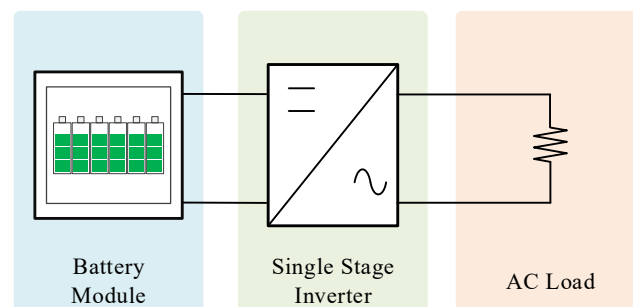**Figure 3.** Pseudo DC-link topology of a BESS.

Figure 4. The single-stage topology of a BESS.

This study proposes a single-stage inverter, as displayed in Figure 5, which is also called a single-stage differential boost inverter (SSDBI). Compared with the others [11,12], the purpose of the proposed inverter is to provide energy from a low-voltage battery module to a 110 V_{ac} AC load, but while connected with the grid. The inverter has fewer components, which only include two inductors, two capacitors, and four switches. Due to the characteristics of the structure, the converter uses high-frequency inductors instead of filter inductors to reduce the cost and the size of the inductors. The capacitors are not used to store an amount of energy, so the capacitance and the size of the capacitors have a lower cost and are smaller.
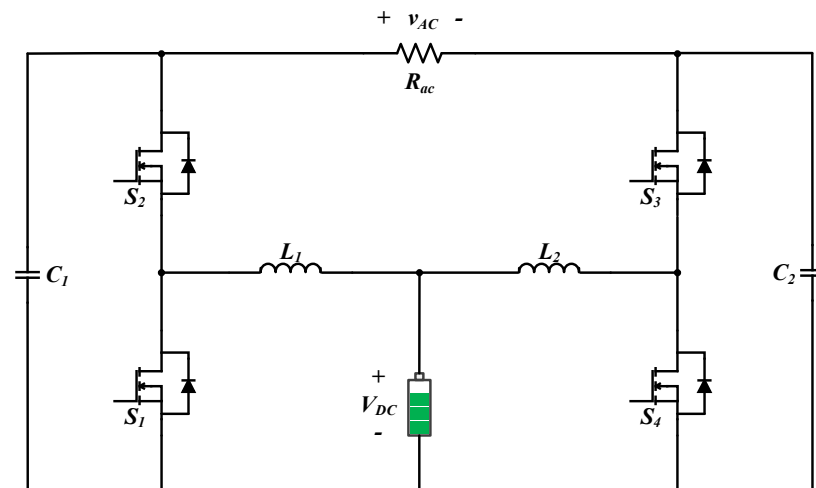

Figure 5. The schematic of the SSDBI.

In previous studies, researchers proposed controls based on the proposed single-stage inverter [13–17]. Damith B. Wickramasinghe Abeywardana and Woei-Luen Chen, respectively, proposed a control combining proportional integral control (PI control) with proportional resonant control (PR control). The control compensated the capacitor's voltage with PR control and then the inductor's current with PI control. This control had better AC

voltage stability while adjusting and limit the inductor's current. However, the control was a double-loop compensator, which made it difficult to stabilize both the outer loop and the inner loop [13,14]. Diana Lopez-Caiza and Oswaldo López-Santos separately proposed sliding-mode control (SMC). Through discontinuous control, SMC keeps adjusting the inductor's current and the capacitor's voltage until the inverter works in stable conditions. SMC is suitable for the SSDBI because it can individually control nonlinear current and voltage. SMC could also reduce the THD of the inverter, but the SMC needs plenty of feedback signals, and the design is also complicated. Kapil Jha used SPWM control, which simplified the design of the control at the cost of THD. Moreover, the control methods, such as space vector pulse width modulation (SVPWM) and the SPWM control with an additional third harmonic, have better utilization of the DC link voltage. However, these control methods are usually used in three-phase buck inverters for driving three-phase motors, and they regard the inverter and the motor as a whole to control the motor's RPM by adjusting the voltage and frequency, but with a constant flux. The traditional SPWM control is not commonly used in real circuits when the load is a motor, but rather when loads have a constant frequency, such as in telecommunication base stations or uninterrupted power supplies.

In view of the above research, this study modified the SPWM for the SSDBI. Through a steady-state circuit analysis, simulations, and hardware experiments, this study verified the proposed inverter's feasibility and the control's modification while considering the system's complication, cost, and THD.

2. System Description of SSDBI

This section describes the steady-state analysis of the SSDBI and the design considerations of the components.

2.1. Steady-State Analysis of the SSDBI

To simplify the analysis, the inverter can be separated into two parts, Converter 1 and Converter 2, because the inverter has a differential architecture. As shown in Figure 6, the directions and symbols of the loops' current and voltage are defined and labeled, where V_{DC} and i_{DC} are the voltage and the current of the DC bus, v_{AC} and i_{AC} are the voltage and the current of the AC load, v_{L1} and i_{L1} are the voltage and the current of the inductor L_1, v_{L2} and i_{L2} are the voltage and the current of the inductor L_2, v_{C1} and i_{C1} are the voltage and the current of the capacitor C_1, and v_{C2} and i_{C2} are the voltage and the current of the capacitor C_2. According to Kirchhoff's Voltage and Current Law, i_{DC} is equal to the sum of i_{L1} and i_{L2}, and v_{AC} is equal to the difference of v_{C1} and v_{C2}.

Since the switching frequency of the inverter is much higher than that required by the AC load, the inverter will perform multiple charging and discharging cycles with the switching frequency in a period of the AC load. Therefore, the following will be introduced with a positive half period and a negative half period, respectively. Table 1 shows the operation modes of Converter 1 and Converter 2, and Figure 7 displays the operation states of the inverter. In the positive half period ($v_{AC} > 0$), Converter 1 works as a boost converter that charges C_1 with v_{DC}, and Converter 2 works as a buck converter that charges V_{DC}. In the negative half period ($v_{AC} < 0$), Converter 1 works as a buck converter that charges V_{DC}, and Converter 2 works as a boost converter that charges C_2. Both Converter 1 and Converter 2 have opposite but similar operation modes in the positive (Mode 1 and Mode 2) and negative (Mode 3 and Mode 4) half periods, respectively. For the steady-state analysis, the positive half period (Mode 1 and Mode 2) will be taken as an example.
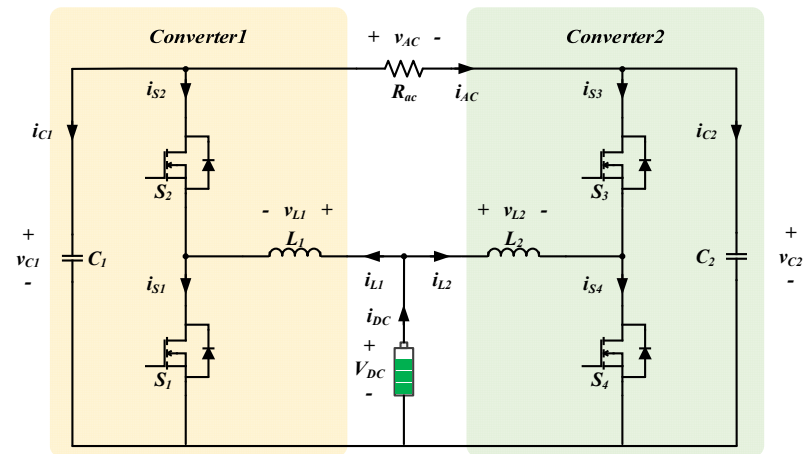
Figure 6. The analytical model of the SSDBI.

Table 1. The operation modes of Converter 1 and Converter 2.

v_{AC}	Mode	Status of Switch	Status of Converter
>0	Mode 1 [$t_0 \sim t_1$]	S_1, S_3 on S_2, S_4 off	Converter 1 : Boost (Charge C_1) Converter 2 : Buck (Charge V_{DC})
	Mode 2 [$t_1 \sim t_2$]	S_2, S_4 on S_1, S_3 off	Converter 1 : Boost (Charge C_1) Converter 2 : Buck (Charge V_{DC})
<0	Mode 3 [$t_2 \sim t_3$]	S_2, S_4 on S_1, S_3 off	Converter 1 : Buck (Charge V_{DC}) Converter 2: Boost (Charge C_2)
	Mode 4 [$t_3 \sim t_4$]	S_1, S_3 on S_2, S_4 off	Converter 1 : Buck (Charge V_{DC}) Converter 2: Boost (Charge C_2)

(a)

(b)

(c)

(d)
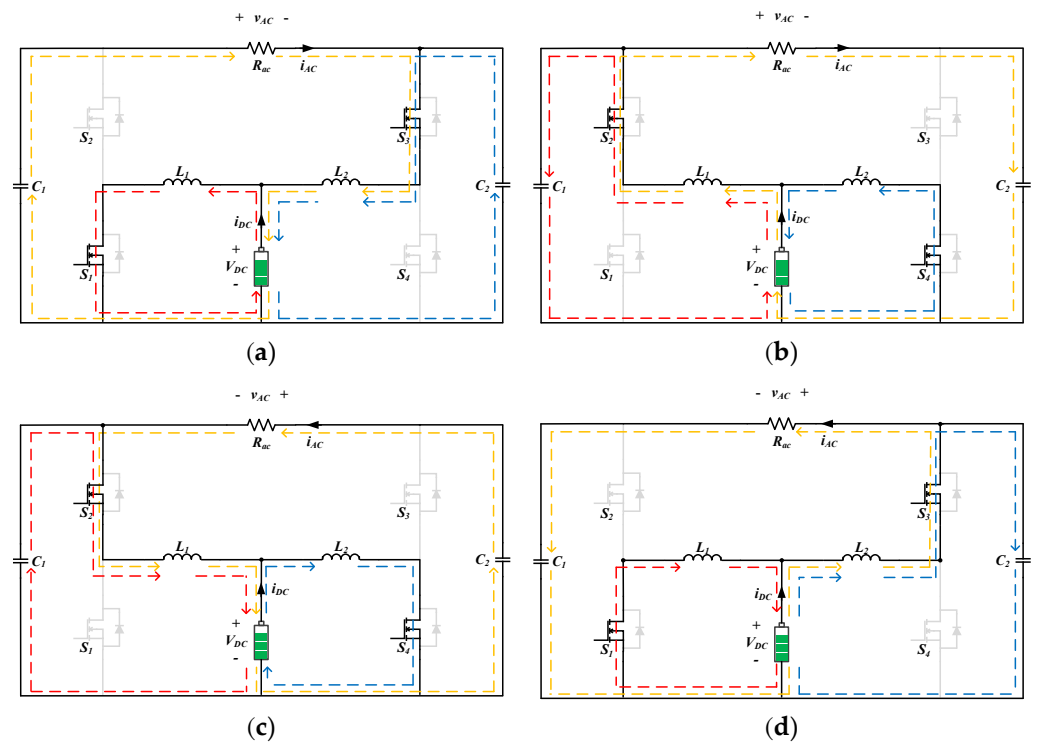
Figure 7. The operation states of the inverter: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4.

Mode 1 [$t_0 \sim t_1$]:

In Mode 1, $v_{AC} > 0$, $i_{AC} > 0$. S_1 (on), S_2 (off), S_3 (on), and S_4 (off). L_1 and L_2 are being charged and C_1 and C_2 are discharging. The voltage across L_1 is V_{DC}, and the voltage across L_2 is $-(v_{C2} - V_{DC})$. The current passed by C_1 is $-i_{AC}$, and that passed by C_2 is $i_{L2} + i_{AC}$. The variations in each of the inductors' current and capacitors' voltage can be obtained as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{DC}}{L_1} \tag{1}$$

$$\frac{di_{L2}}{dt} = -\frac{v_{C2} - V_{DC}}{L_2} \tag{2}$$

$$\frac{dv_{C1}}{dt} = -\frac{i_{AC}}{C_1} \tag{3}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2} + i_{AC}}{C_2} \tag{4}$$

Mode 2 [$t_1 \sim t_2$]:

In Mode 2, $v_{AC} > 0$, $i_{AC} > 0$. S_1 (off), S_2 (on), S_3 (off), and S_4 (on). L_1 and L_2 are discharging, and C_1 and C_2 are being charged. The voltage across L_1 becomes $V_{DC} - v_{C1}$, and the voltage across L_2 becomes V_{DC}. The current passed by C_1 changes to $i_{L1} - i_{AC}$, and that passed by C_2 changes to i_{AC}. The variations in each of the inductors' current and capacitors' voltage are as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{DC} - v_{C1}}{L_1} \tag{5}$$

$$\frac{di_{L2}}{dt} = \frac{V_{DC}}{L_2} \tag{6}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1} - i_{AC}}{C_1} \tag{7}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{AC}}{C_2} \tag{8}$$

Through the aforementioned analysis, Equations (9) and (10) can be obtained by referring to (1), (2), (5), (6), and the volt-second balance theory.

$$v_{C1} = \frac{V_{DC}}{1 - D} \tag{9}$$

$$v_{C2} = \frac{V_{DC}}{D} \tag{10}$$

We already know that v_{AC} is equal to the voltage difference between v_{C1} and v_{C2}. Hence, the relationship between V_{DC} and v_{AC} can be calculated in (11).

$$v_{AC} = \frac{V_{DC}}{1 - D} - \frac{V_{DC}}{D} \tag{11}$$

After rearranging (11), the duty ratio D is expressed as follows:

$$D = \frac{v_{AC} - 2V_{DC} + \sqrt{v_{AC}^2 + 4V_{DC}^2}}{2v_{AC}} \tag{12}$$

The gain of the inverter M is the ratio of V_{DC} and v_{AC}. Rearranging (12) once more, M and the relationship between M and D can be shown by the following.

$$M = \frac{2D - 1}{(1 - D)D} \tag{13}$$

$$D = \frac{M - 2 + \sqrt{M^2 + 4}}{M} \tag{14}$$

2.2. Design Considerations of the Components

Through the analysis, it can be observed that the formula of Converter 1 in the positive half period is the same as the formula of Converter 2 in the negative half period. So, the capacitances of C_1 and C_2 are the same. Therefore, the design formula of C_1 and C_2 can be inferred from (3), as shown in (15), where Δv_{C1} is the ripple of the capacitor's voltage.

$$C = i_{AC} \frac{DT_s}{\Delta v_{C1} V_{C1}} \tag{15}$$

In addition, the design considerations of the inductors are similar to those of the capacitors. The formula of the design considerations can be inferred from (1), as shown in (16), where Δi_{L1} is the ripple of the inductor's current.

$$L = V_{DC} \frac{DT_s}{\Delta i_{L1} I_{L1max}} \tag{16}$$

3. The Analysis of the Control

3.1. The Problem of Applying Traditional SPWM Control to the Proposed Inverter

It is well known that there have already been many types of control proposed for inverters; SPWM is the most mature one of these, and this type of control is usually applied for buck inverters. Figure 8 shows the traditional SPWM control principle applied to a buck inverter, where the duty ratio D_{spwm} is generated by the comparison between a sine wave signal $V_{control}$ and a triangular wave signal V_{tri}, the amplitude and frequency of V_{tri} are $\hat{V}_{tri}$ and f_s, $\hat{V}_{control}$ represents the amplitude of $V_{control}$, and the sine wave's frequency f_1 is the same as the output voltage frequency f [18].
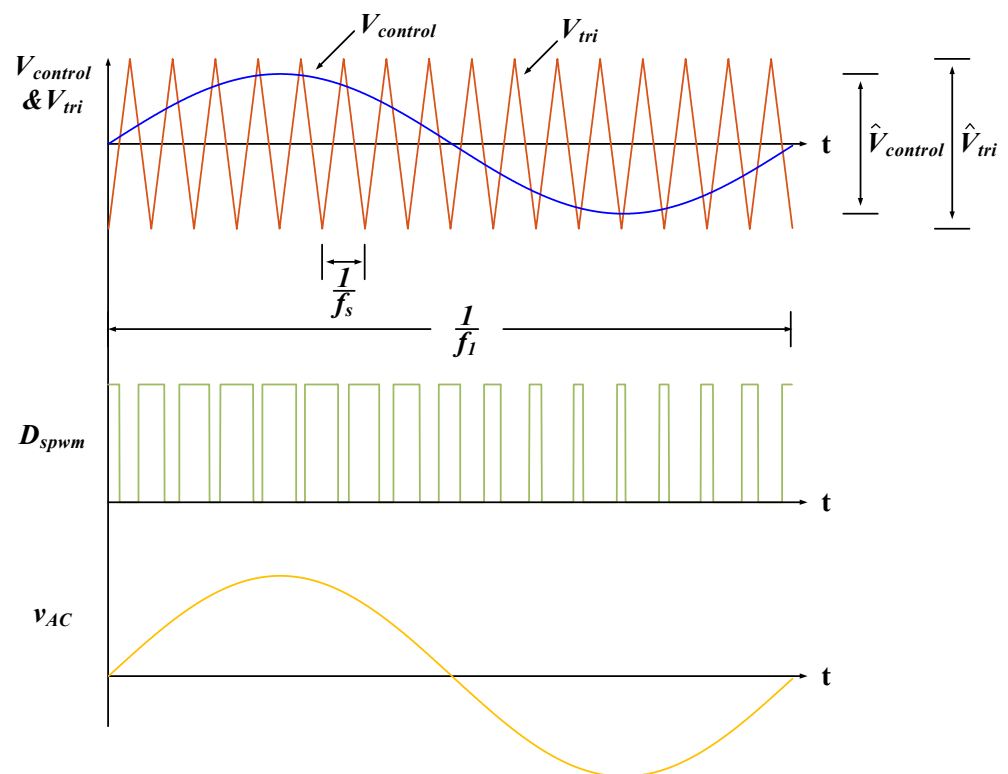
Figure 8. The relationships among the control signal, duty ratio, and AC output v_{AC} in buck inverters with traditional SPWM control.

The amplitude modulation index m_a is the ratio of $\hat{V}_{control}$ and $\hat{V}_{tri}$. m_a can determine D_{spwm}, as shown in (17).

$$D_{spwm}(t) = \frac{1}{2} + \frac{V_{control}(t)}{2} = \frac{1}{2} + \frac{m_a \sin \omega t}{2} \tag{17}$$

Since SPWM is mainly used in buck inverters, the gain M must be less than 1, which is half of m_a. The formulas of M and the rearranged D_{spwm} are shown in (18) and (19).

$$M = \frac{v_{AC}}{V_{DC}} = \frac{1}{2}m_a = \frac{1}{2}\frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{18}$$

$$D_{spwm}(t) = \frac{1}{2} + \frac{V_{control}(t)}{2} = \frac{1}{2} + \frac{m_a \sin \omega t}{2} = \frac{1}{2} + M\sin\omega t = \frac{1}{2} + \frac{v_{AC}(t)}{V_{DC}} \tag{19}$$

If the DC voltage is assumed as a stable power supply, its value will be constant. Through the aforementioned formula, D_{spwm}, $v_{AC,}$ and M will increase while $V_{control}$ (t) increases. So, $\hat{V}_{control}$ can be regarded as v_{AC} (t) with an equally scaled reduced amplitude. M has a linear relationship with D_{spwm}.

However, if the above SPWM control is directly used in the SSDBI [17], the voltage of the AC output will be distorted. As shown in Figure 9, the expected sinusoidal waveform of the AC output will become a waveform that is similar to a triangular waveform.
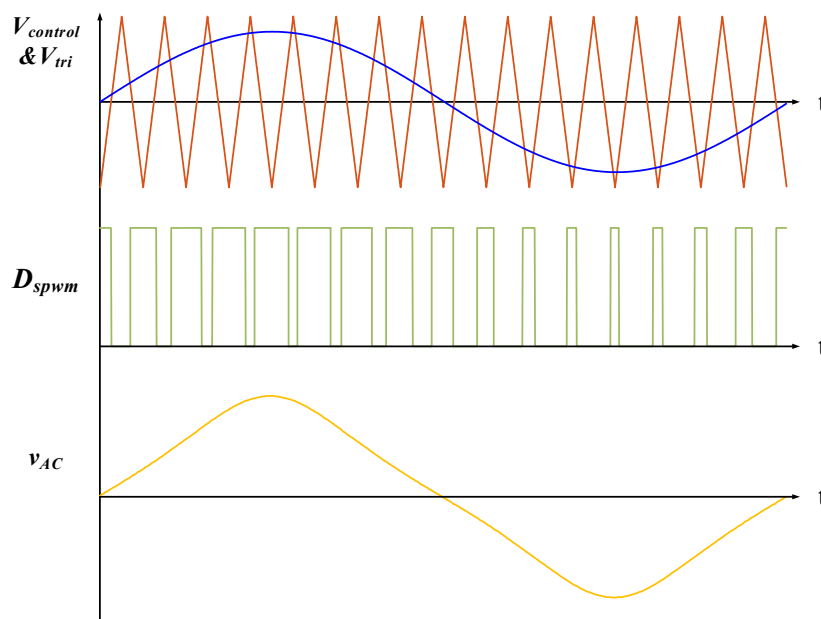
Figure 9. v_{AC} waveform generated by the proposed inverter with SPWM control.

The reason for the distortion is that $V_{control}$ still has the same relationship with v_{AC}, D_{spwm}, and $V_{control}$. However, the formulas among these parameters, as shown in (12) and (14), are different from those of the buck inverter.

3.2. The Proposed Modified SPWM Control

To overcome this distortion, this study generated a modified SPWM control for the proposed inverter. The proposed SPWM modifies a new formula for the new duty ratio $D_{modified\_spwm}$, which can be obtained from (12).

$$D_{modified\_spwm}(t) = \frac{v_{AC}(t) - 2V_{DC} + \sqrt{v_{AC}^2(t) + 4V_{DC}^2}}{2v_{AC}(t)} \tag{20}$$

We can get the modified $V_{control}(t)$ by putting (20) into (17), as shown in (21). Although $V_{control}$ has a new relationship with v_{AC}, the inverter driven with $D_{modified\_spwm}$ will have the expected sinusoidal voltage waveform of the AC output.

$$V_{control}(t) = \frac{-2V_{DC} + \sqrt{v_{AC}^2(t) + 4V_{DC}^2}}{v_{AC}(t)} \tag{21}$$

Figure 10 displays the comparison between the traditional SPWM control and the modified SPWM control. In Figure 10a, the comparison is focused on $V_{control}$, where the dotted line and the solid line represent $V_{control}$ in the traditional SPWM control and the modified SPWM control, respectively. Figure 10b shows the voltage waveform's difference in the AC output. According to Figure 10, even if the traditional SPWM control gives a sine wave signal for $V_{control}$ in the proposed inverter, v_{AC} will be distorted. In contrast, the proposed SPWM control will have the expected sinusoidal voltage output with the modified $V_{control}$.

(**a**)

(**b**)
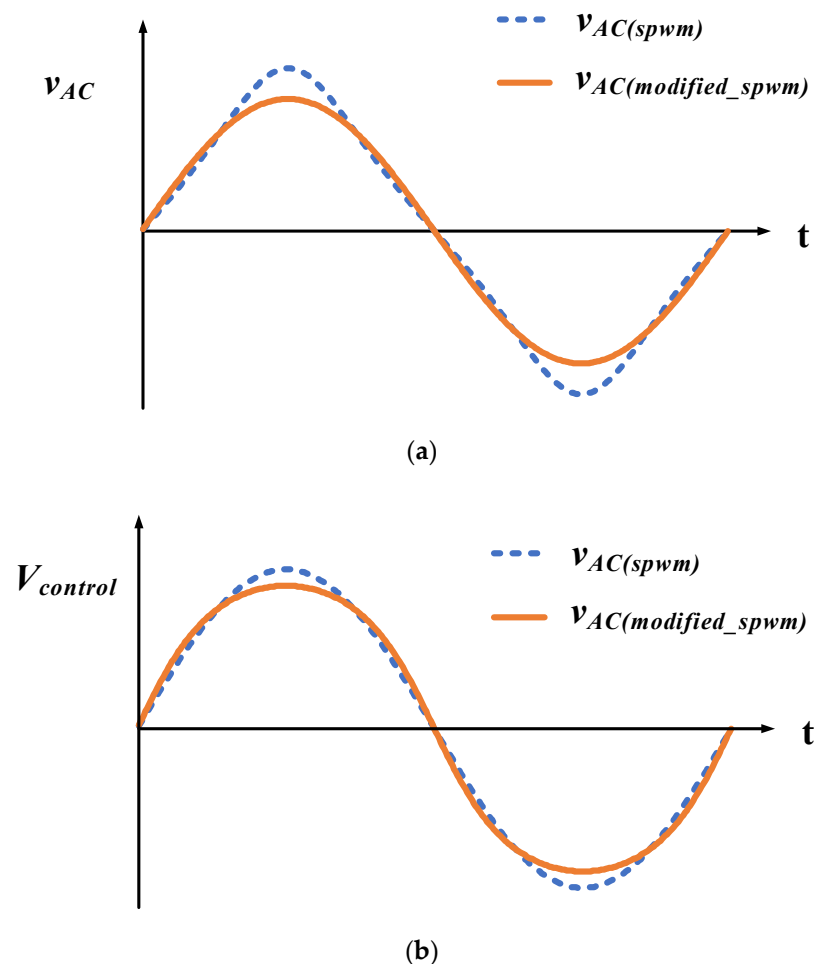
Figure 10. A comparison between the traditional SPWM control and the modified SPWM control: (**a**) $V_{control}$ and (**b**) v_{AC}.

4. Experimental Results

4.1. Description of System Specifications

Figure 11 shows the experimental platform of the SSDBI, and the actual system configuration is displayed in Figure 12. In this study, the DC input was a 16S3P battery module, where the single cells (PC40155) were manufactured by Phoenix Battery Corporation, and the voltage range of the battery module was 33.6–58.4 V_{dc}. The other system specifications

can also be obtained in Table 2, for which the inductors and the capacitors were measured with an LCR meter (WK3255B).
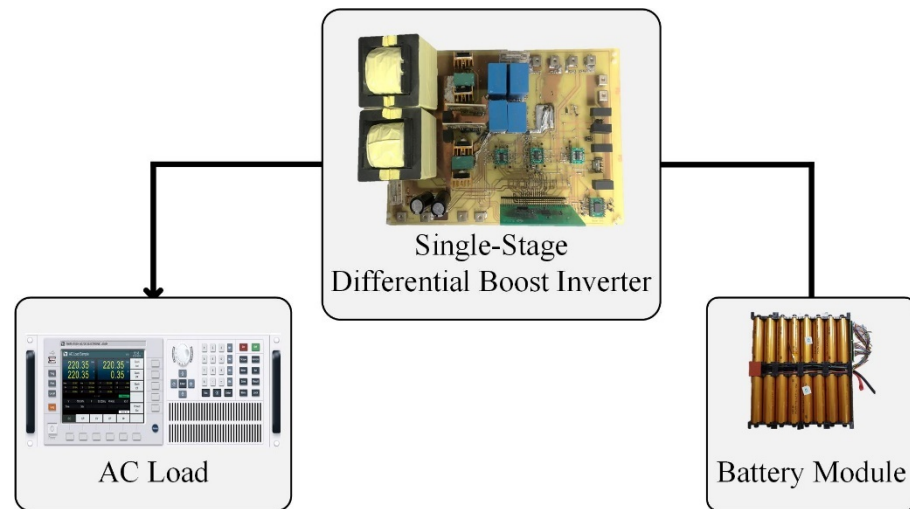
Figure 11. System connections of the SSDBI.
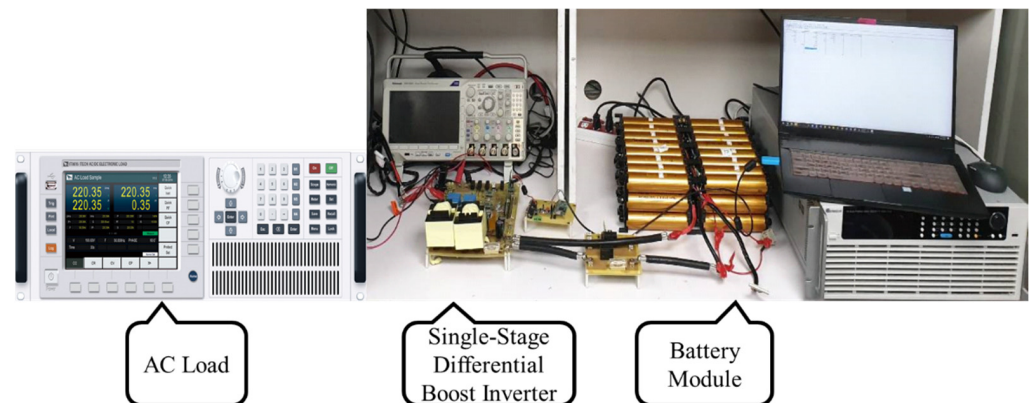
Figure 12. The laboratory setup of the test platform.

Table 2. Specification of the proposed BESS.

Item	Value
Battery module (voltage range)	33.6–58.4 V_{dc}
Battery module (voltage rated)	52.8 V_{dc}
AC output voltage	110 V_{rms}
Power	1000 W
Switching frequency	21.6 kHz
Inductor	120 μH, 120 μH
ESR of Inductor	0.2 Ω, 0.2 Ω
Capacitor	12 μF, 12 μF
ESR of Capacitor	0.02 Ω, 0.02 Ω

4.2. Results of the Simulation and Hardware Experiments

In this section, the proposed modified control is compared with the traditional SPWM using the results of simulation and hardware experiments. The proposed BESS was tested under different test conditions; the AC loads used included: 48 Ω (250 W), 24 Ω (500 W), and 12 Ω (1 kW). The simulation software used in this research, Matlab, was manufactured by MathWorks, Inc. (Natick, MA, USA).

First, this study compared the controls' influence on the output waveforms in simulations, as shown in Figure 13, where the traditional SPWM control is represented by a dotted line, the modified SPWM control is displayed with a solid line, the *X*-axis is for the time, and the *Y*-axis is the amplitude of $V_{control}$. From Figure 13, it can be observed that $V_{control}$ of the modified SPWM was not a sinusoidal waveform.
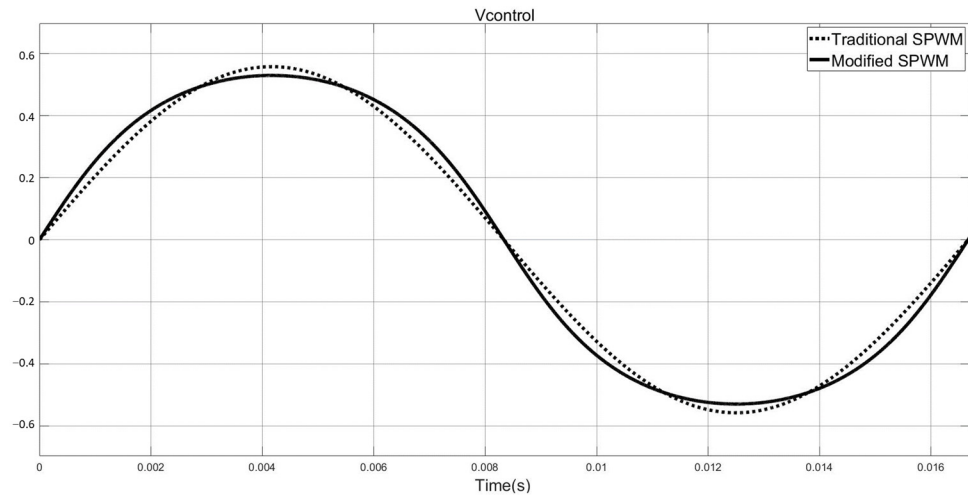
Figure 13. Comparison of $V_{control}$ between the traditional SPWM and modified SPWM controls.

Secondly, the $V_{control}$ of both controls when applied to the control loop to drive the SSDBI in the simulations is shown in Figure 14. The output waveforms are displayed in Figures 15–17, which show the voltage and current waveforms with the traditional SPWM control and the modified SPWM control. By analyzing the differences, it can be easily observed that the proposed inverter with the application of the modified SPWM control had a better output in the simulation.
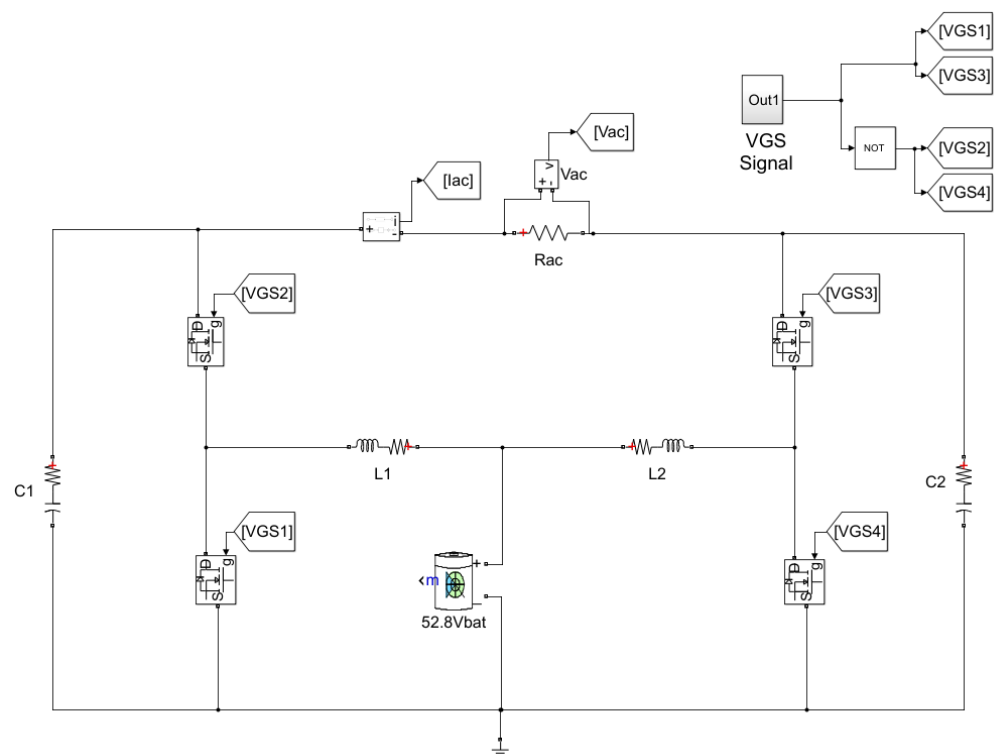
Figure 14. The circuit diagram of the proposed inverter in the simulation.

For further verification, this study tested the SPWM controls in hardware experiments. The waveforms from the hardware experiments are shown in Figures 18–20. The results show that the traditional SPWM control needs a larger peak value of both the voltage and current than the modified control while reaching the same root mean square (RMS). This problem will lead to an increment in the system specifications.

In addition, this study also analyzed the THD of the AC voltage output with simulations; the AC voltage output was the voltage difference between two capacitors and the voltage of the capacitors changed along with the switching frequency. Therefore, the THD was also affected by the switching frequency and the equivalent series resistance of the inductors L_1 and L_2. Figures 21–23 show analyses of the simulation of the THD, where the THD of the traditional SPWM control was above 9%, while the THD of the modified SPWM was lower under 5%. The reason is related to the aforementioned phenomenon, which is shown in Figures 15–20.
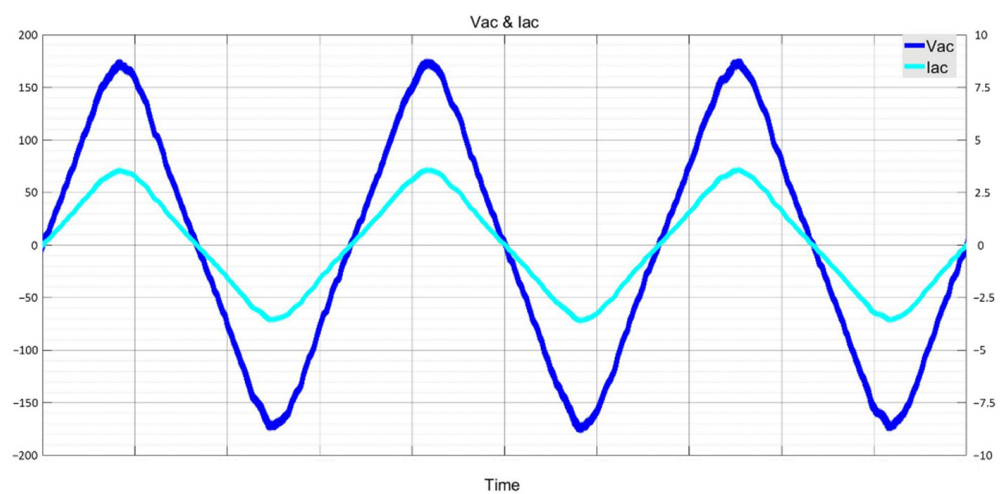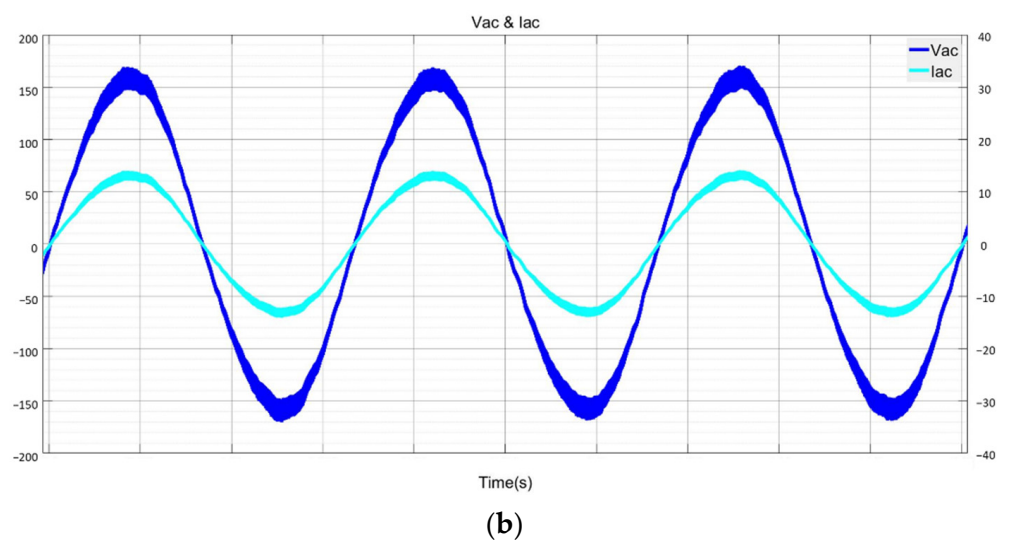

(**a**)
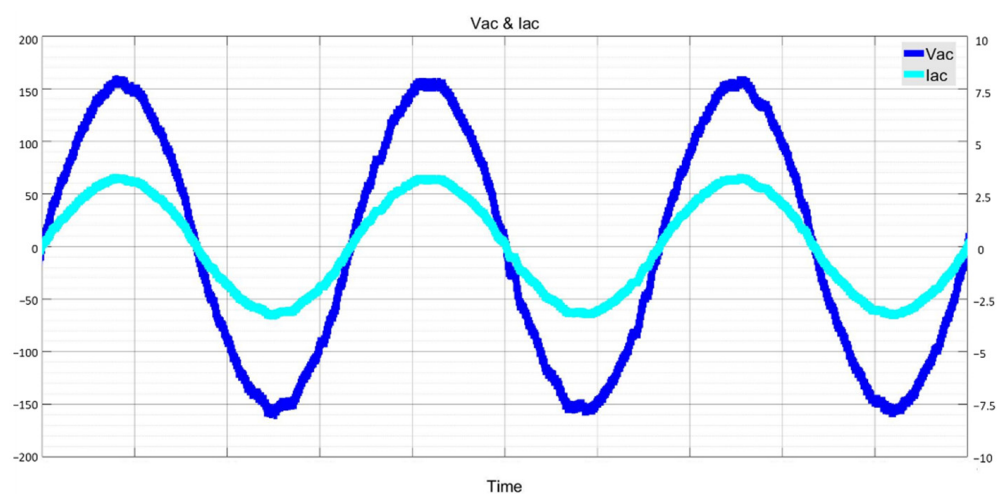
(**b**)

Figure 15. The simulation results (250 W) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

(a)

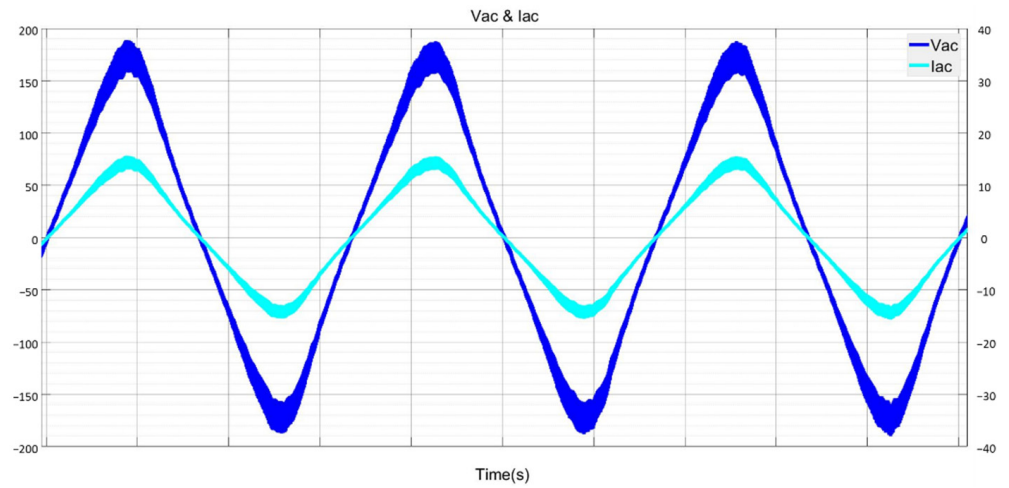
(b)
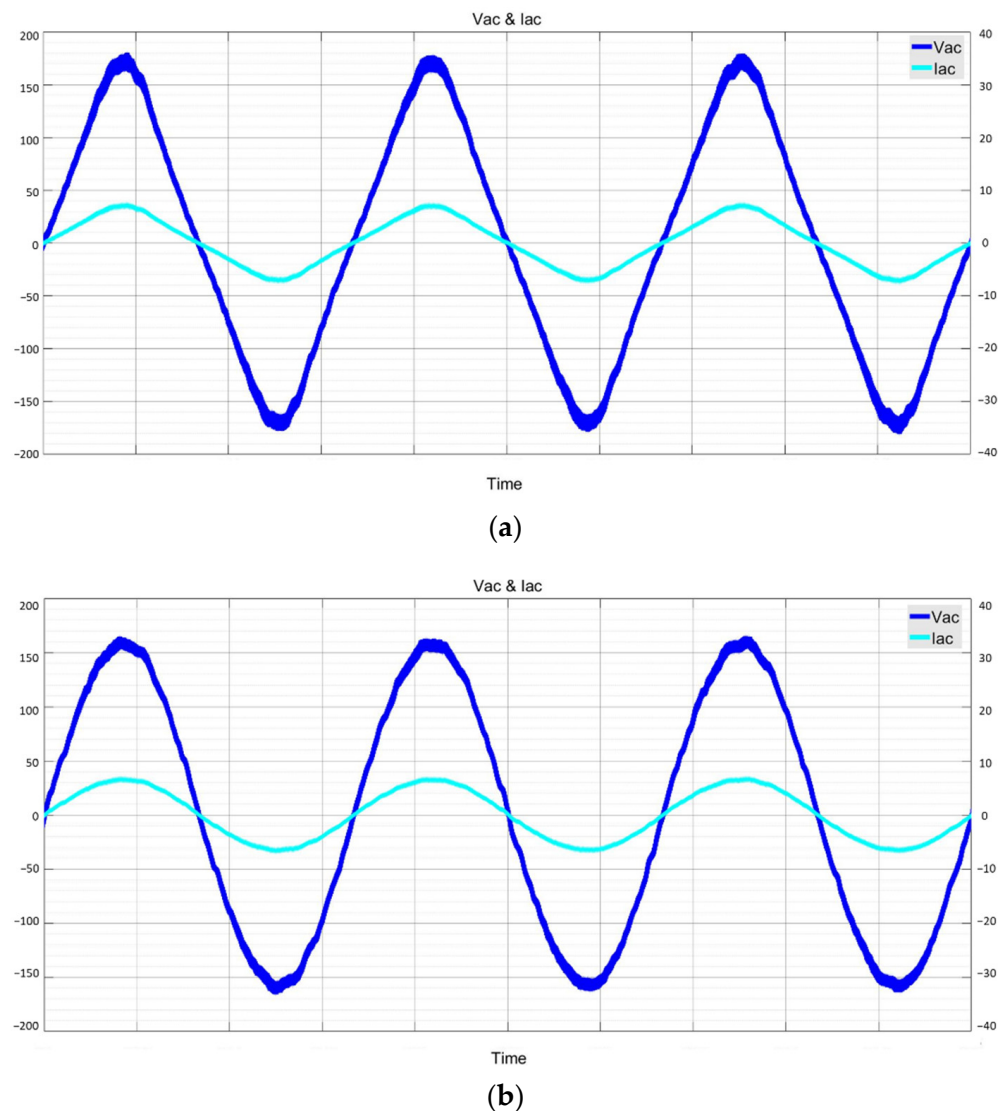
Figure 16. The simulation results (500 W) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

Finally, the actual experiments were implemented with the hardware shown in Figure 12. The THD analysis of the AC output voltage was performed with a Power Analyzer. The results are shown in Figures 24–26, where the THD of the modified SPWM control was lower than the THD of the traditional SPWM control. The results are within the standard, for which there is a 5% limitation in IEEE Std 519-1992 and 8% in IEEE Std 519-2014 [19].

In summary, the SSDBI topology has been proposed and discussed in recent years. Voltage distortion will occur on the AC side when the traditional SPWM control is used with the SSDBI it is operated with high voltage gain [17]. This study certified this phenomenon with simulations and hardware experiments. To overcome this problem, this study analyzed the characteristics of the SSDBI and inferred an appropriate mathematical model of the duty according to the relationship between V_{AC} and V_{DC} (Equations (11) and (12)). Since the derived mathematical model of the duty modified the traditional SPWM control, the use of the modified SPWM control with the SSDBI improved the voltage distortion on the AC side and the THD. The SSDBI was tested under three different loads (25%, 50%, and 100%) to verify the theoretical predictions in both simulations and hardware experiments. After collating the above results, the improvement in the voltage distortion on the AC side can be observed in Figures 15–20, and the comparison of the THD in the

results of the simulations and hardware experiments can be observed in Table 3, where the THD in the simulations was close to that in the hardware experiments. The modified SPWM control had better performance than that of the traditional SPWM control.
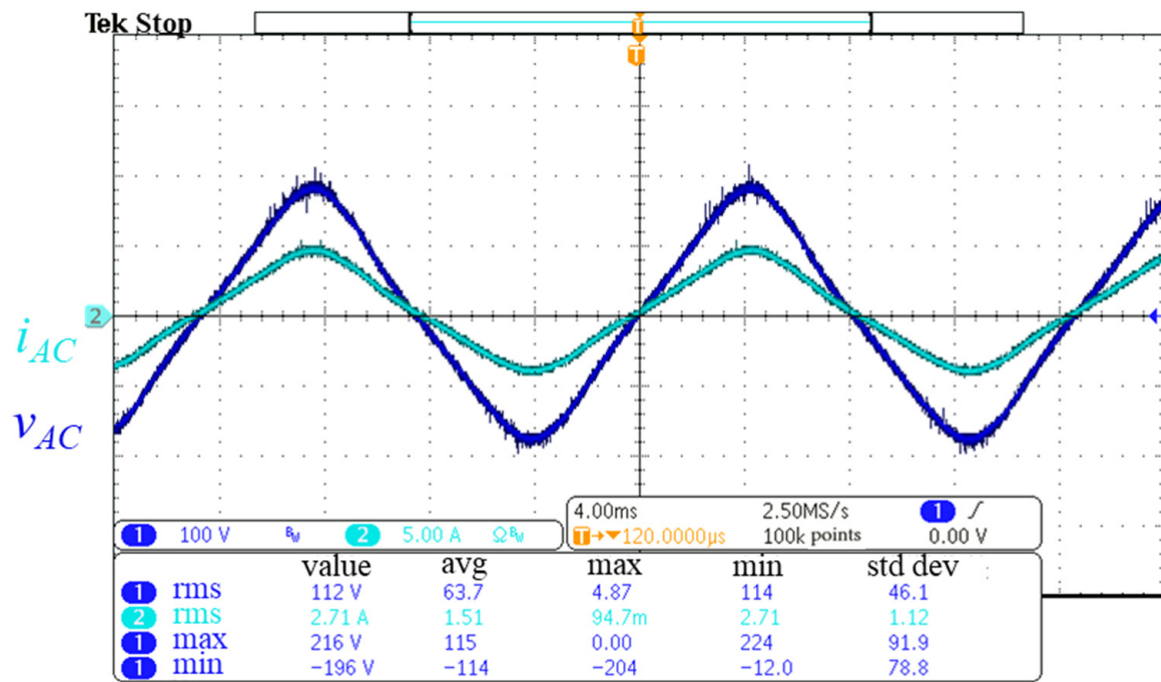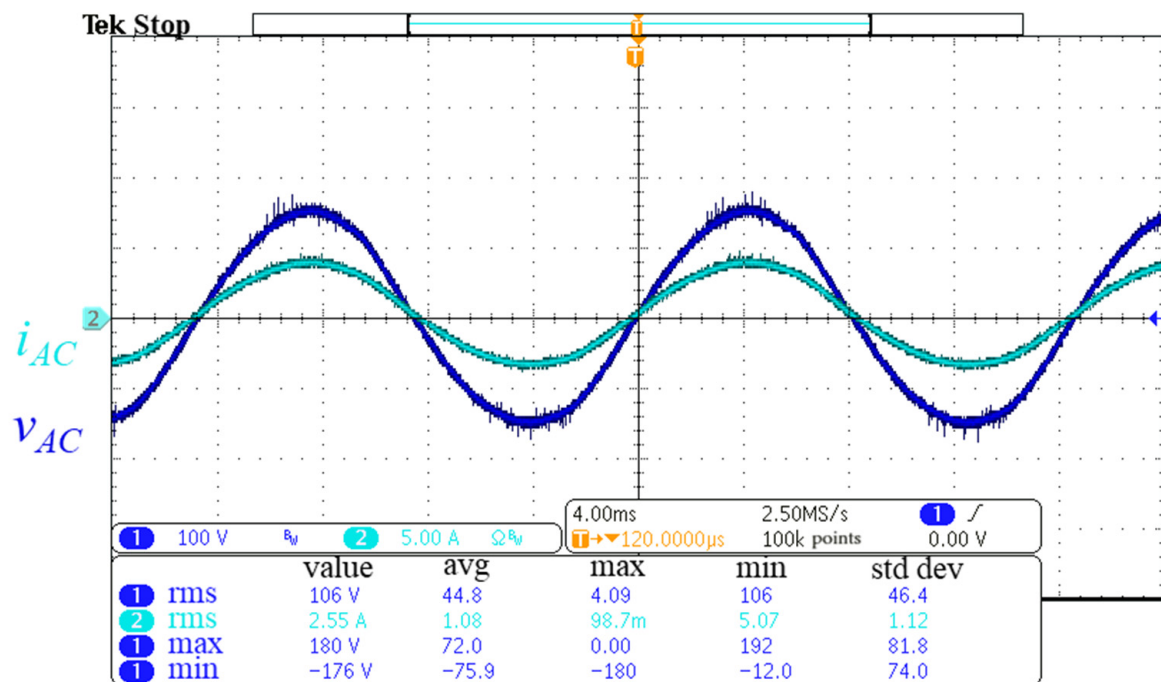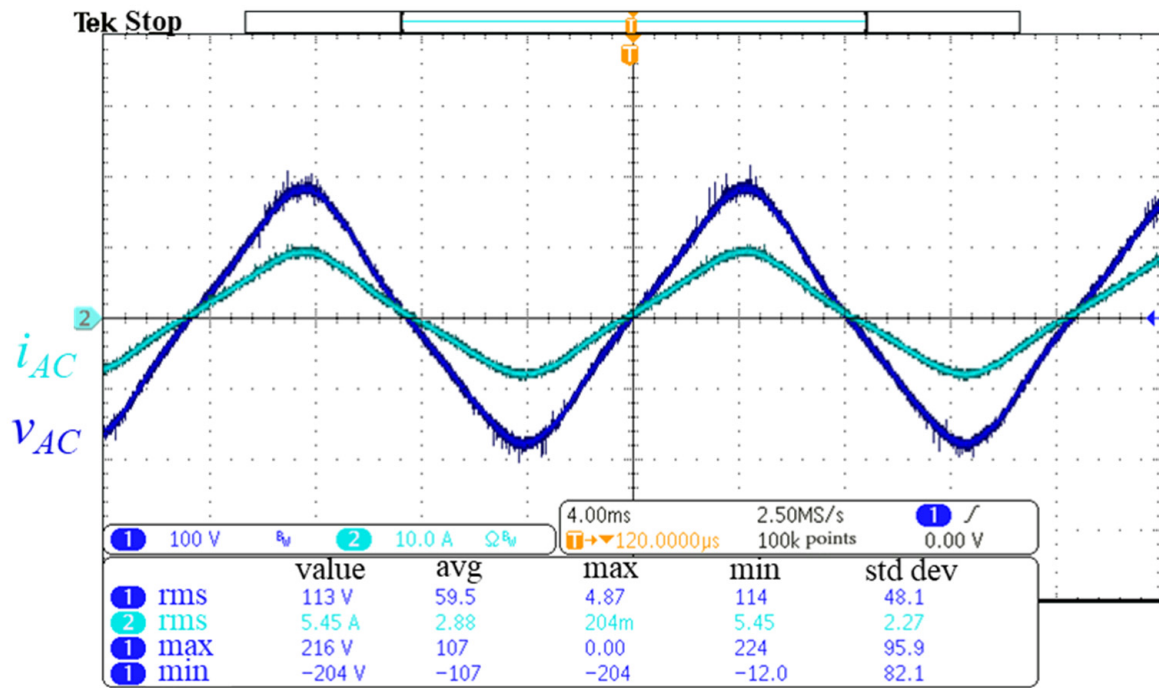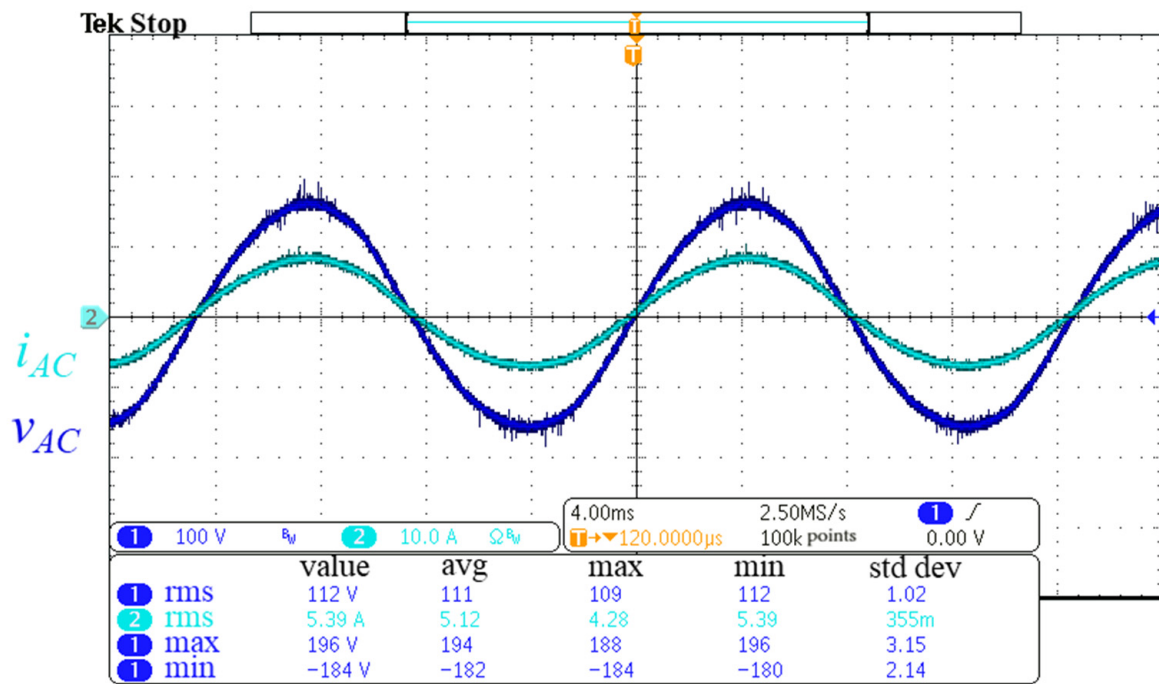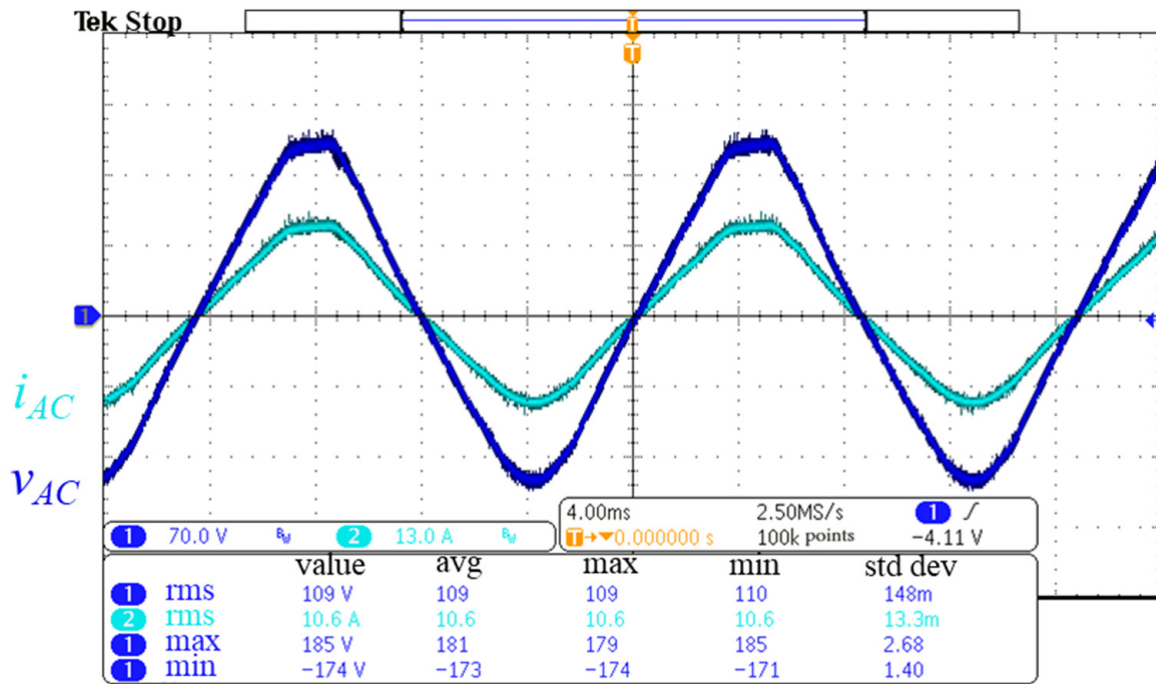

Figure 17. The simulation results (1 kW) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.
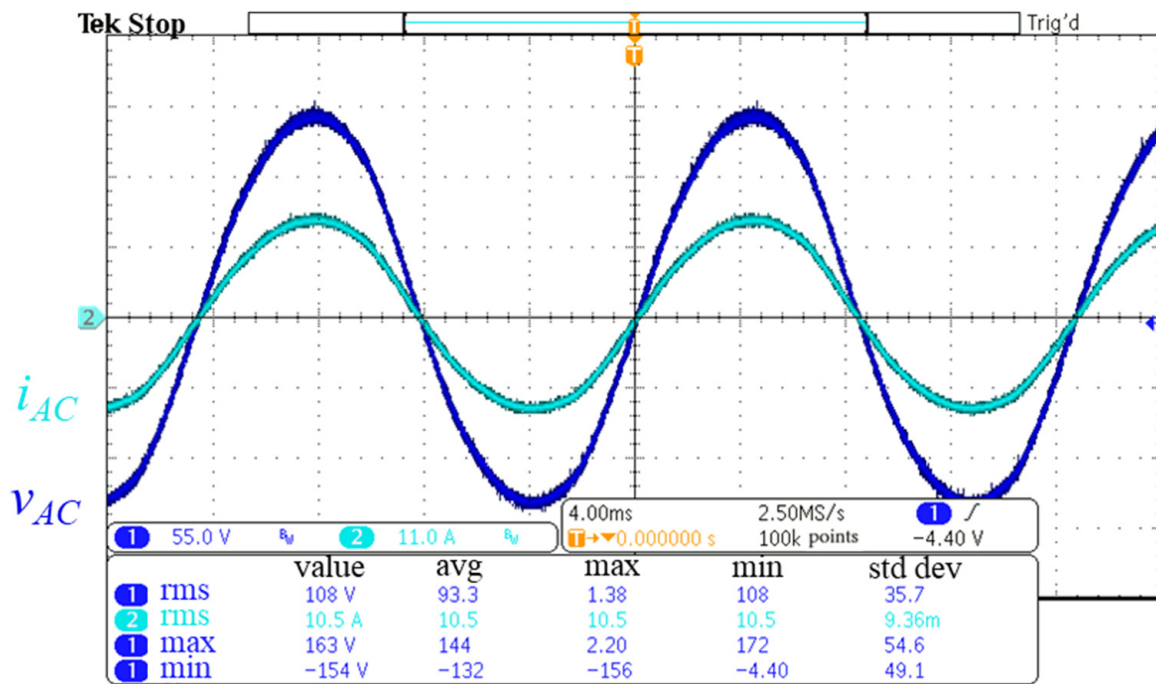
(**a**)

(**b**)

Figure 18. The measured results (250 W) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

(**a**)

(**b**)

Figure 19. The measured results (500 W) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

(**a**)

(**b**)

Figure 20. The measured results (1 kW) of the voltage and current output waveforms when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.
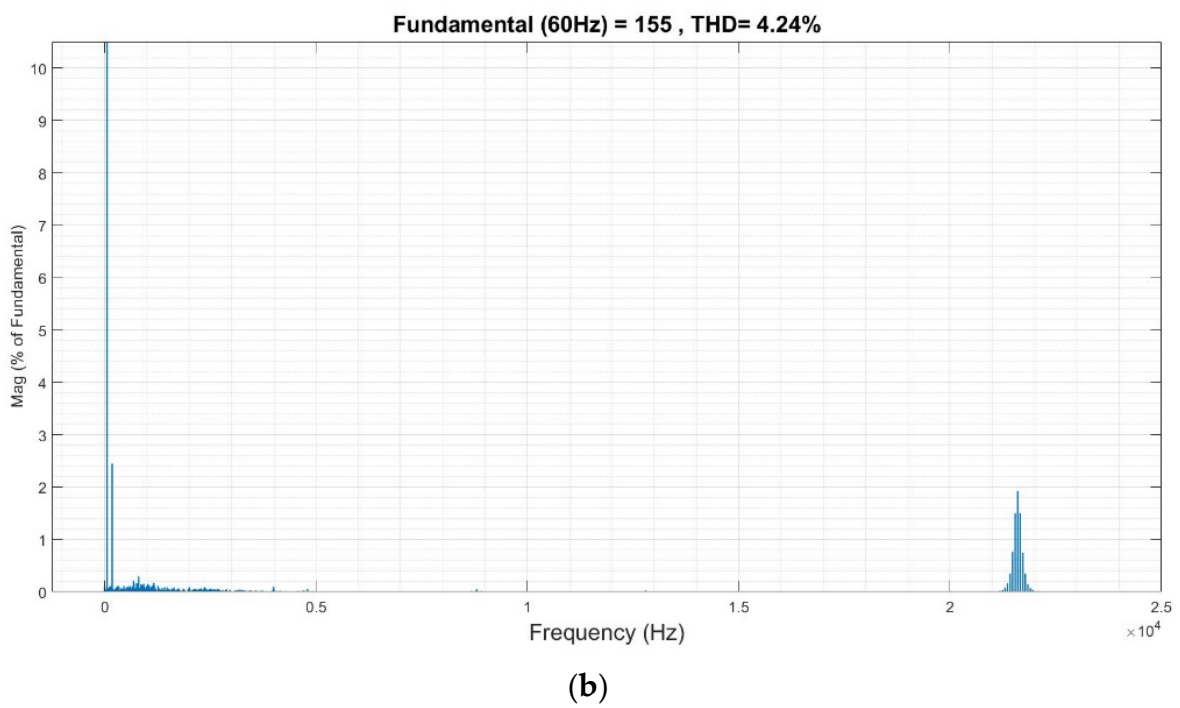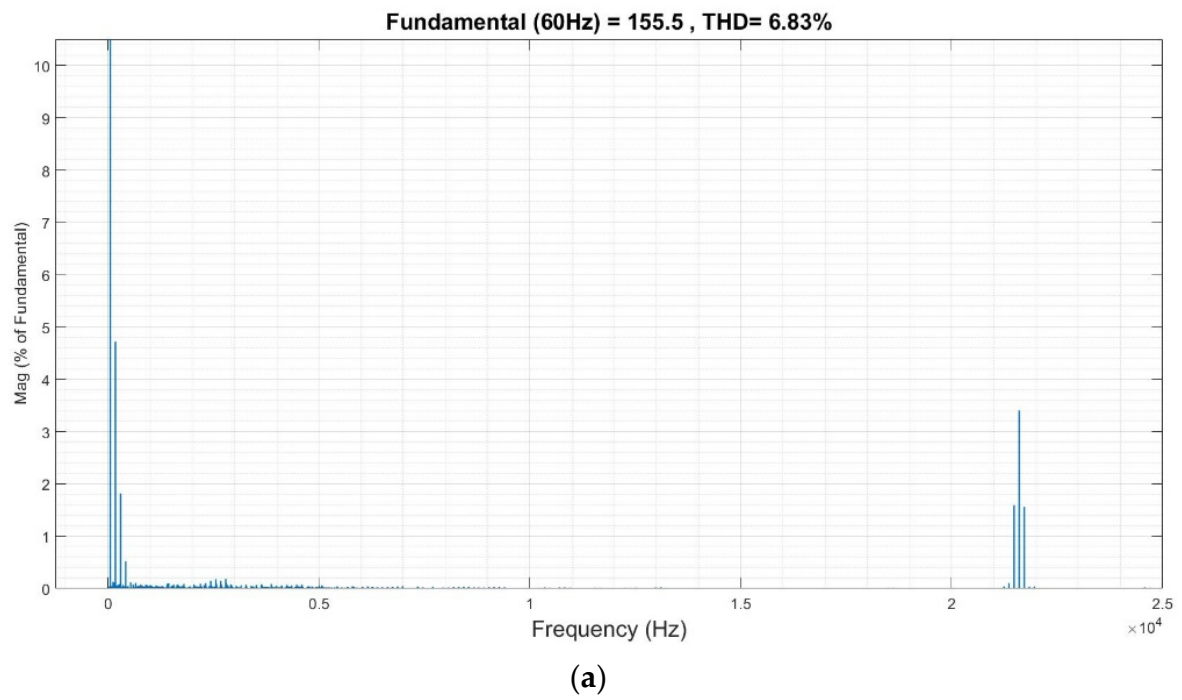
(**a**)

(**b**)
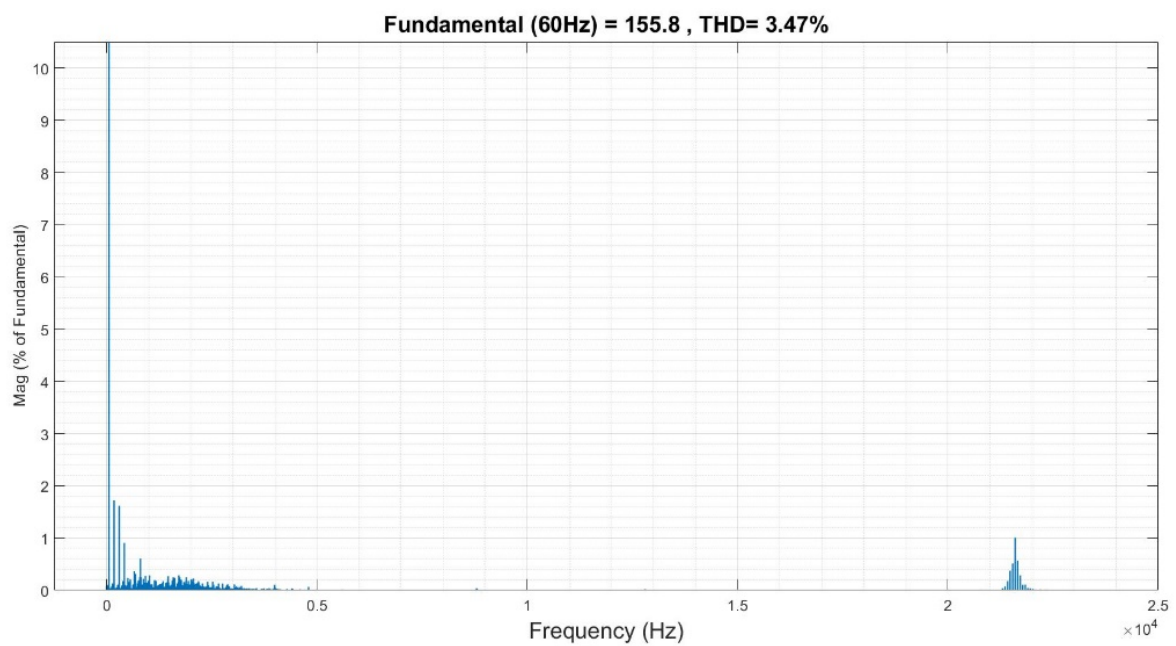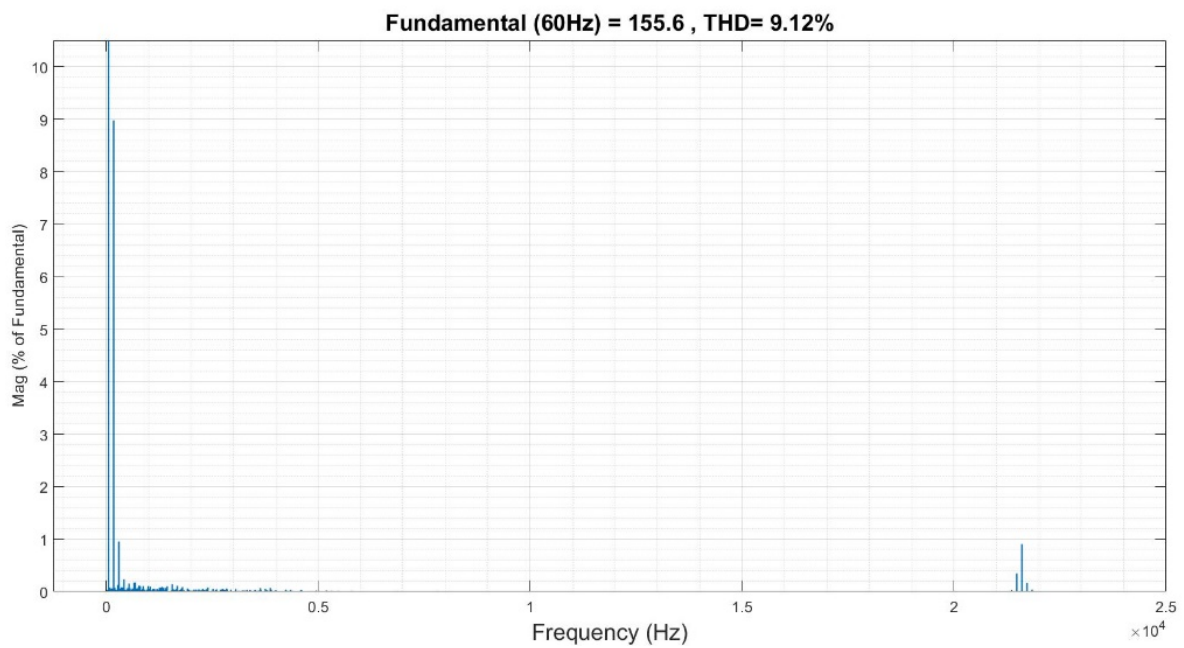
Figure 21. THD analysis of the simulation (250 W) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.
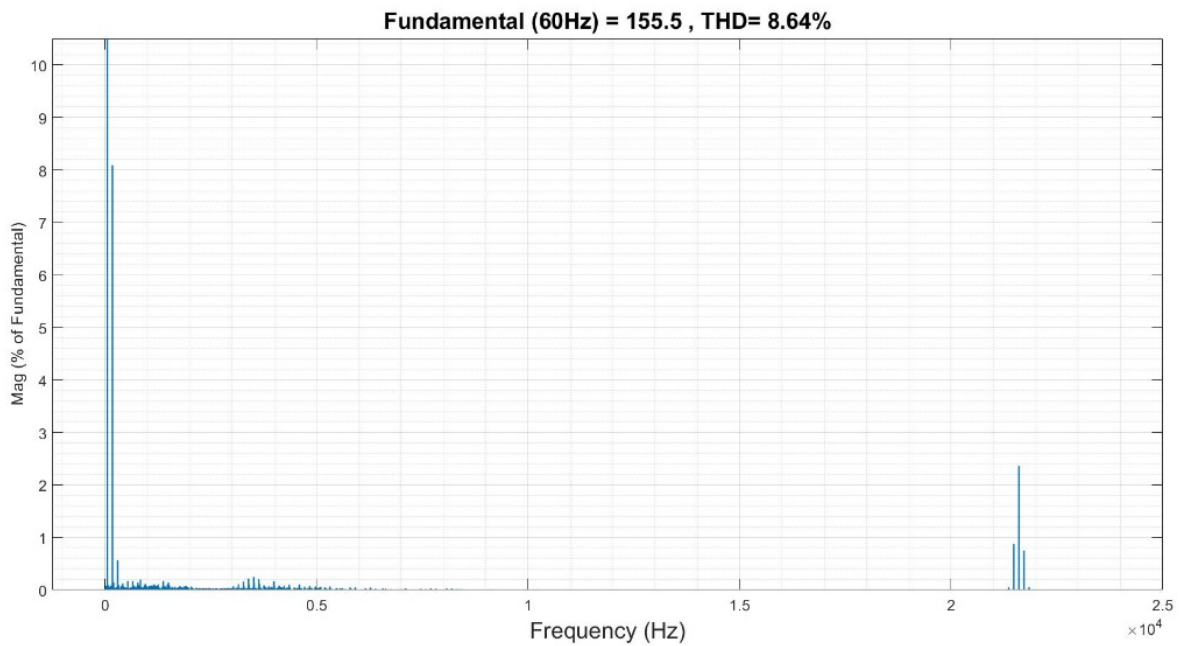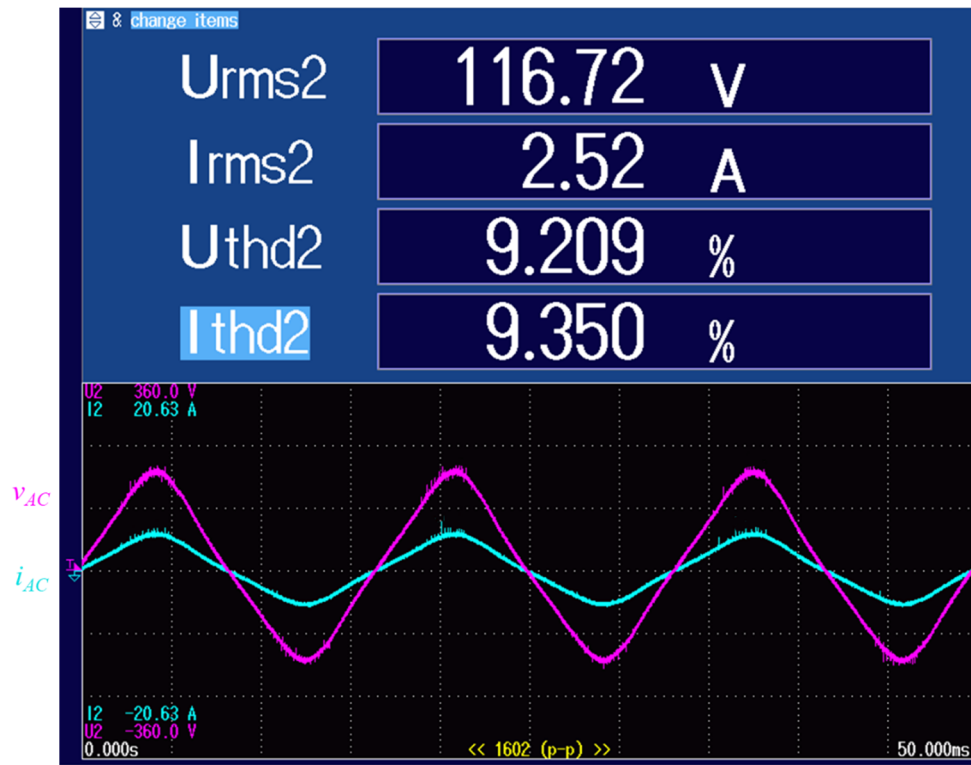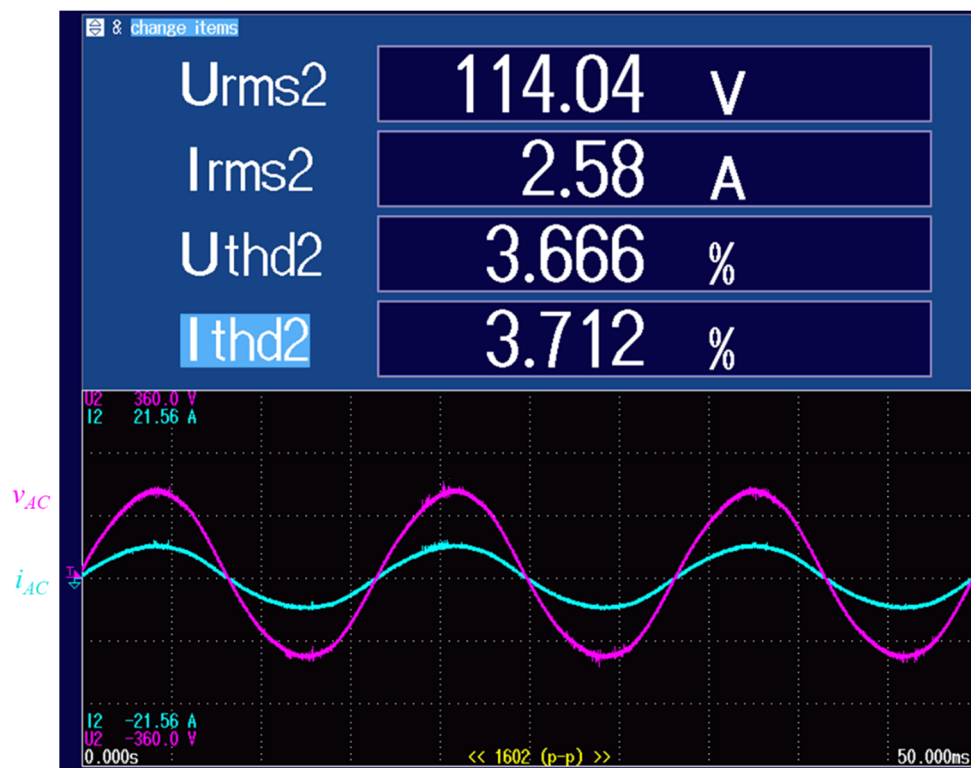
(**a**)
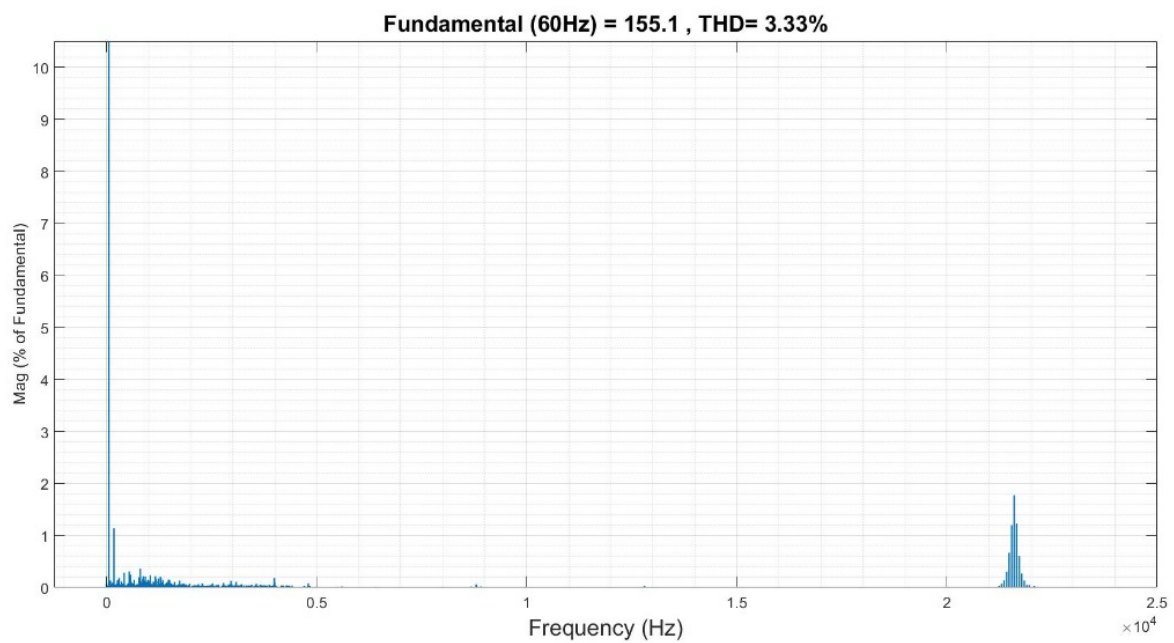
(**b**)

Figure 22. THD analysis of the simulation (500 W) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

(a)

(b)

Figure 23. THD analysis of the simulation (1 kW) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.
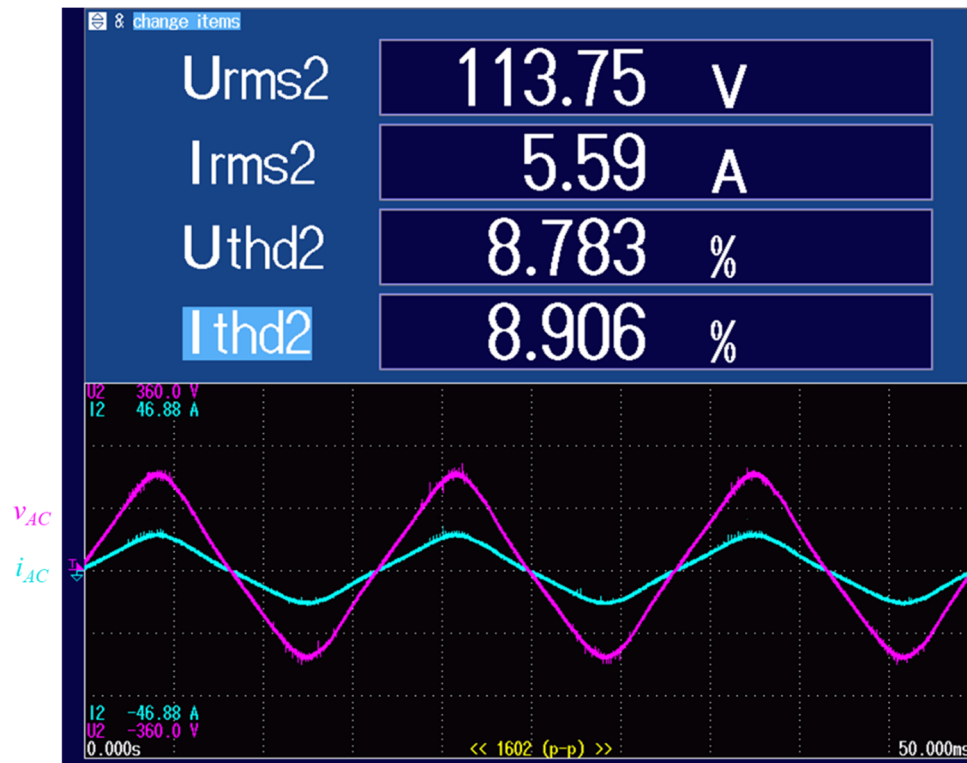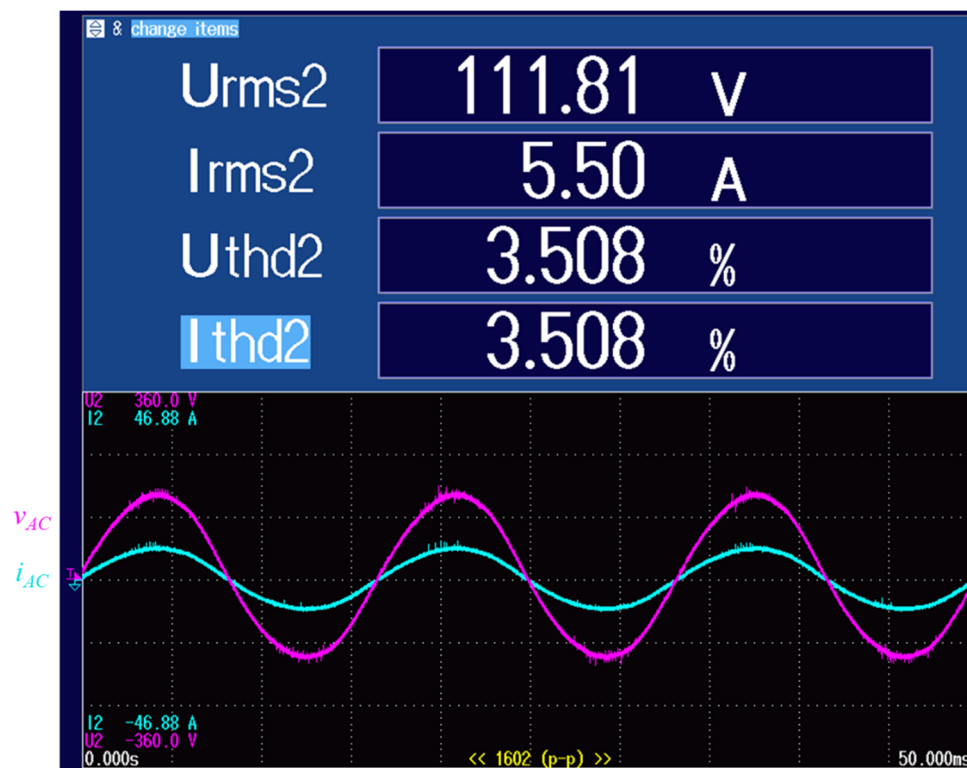
(**a**)

(**b**)

Figure 24. THD analysis in hardware experiments (250 W) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.
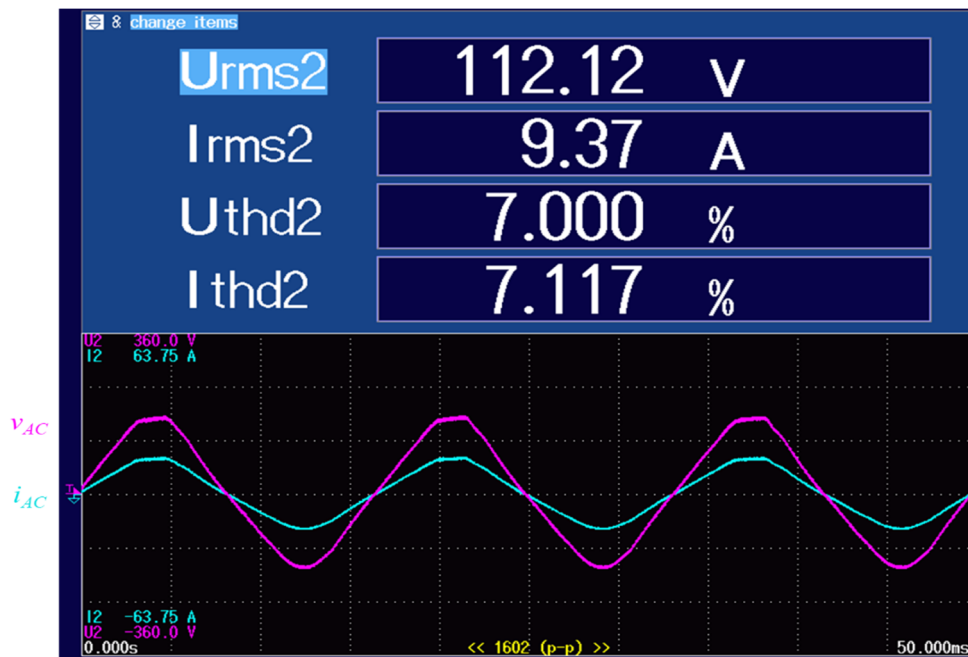
(**a**)

(**b**)

Figure 25. THD analysis in hardware experiments (500 W) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

(**a**)
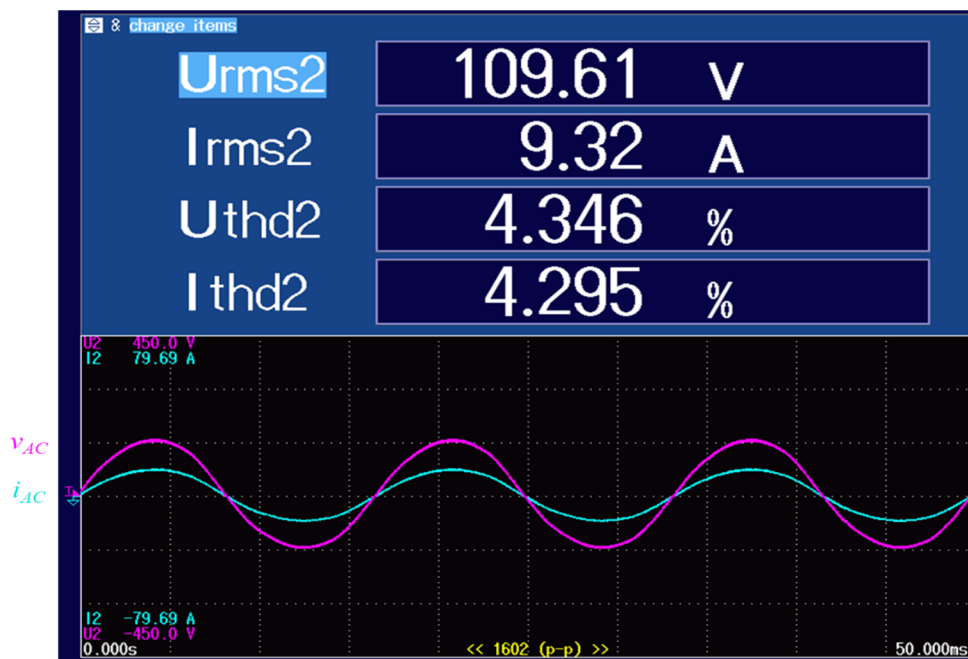

(**b**)

Figure 26. THD analysis in hardware experiments (1 kW) when using (**a**) the traditional SPWM control and (**b**) modified SPWM control.

Table 3. Comparison of the THD in the results of the simulations and hardware experiments.

Results	THD		
	250 W	**500 W**	**1000 W**
Simulation (traditional)	9.12%	8.64%	6.83%
Simulation (modified)	3.47%	3.33%	4.24%
Hardware experiment (traditional)	9.20%	8.78%	7.00%
Hardware experiment (modified)	3.66%	3.50%	4.29%

5. Conclusions

When the traditional SPWM control is directly used in an SSDBI, waveform distortion and a high voltage peak will occur on the AC side. The problems increase the THD and the stress on the components of the inverter. Therefore, this study proposed a modified SPWM control for application to the SSDBI in order to overcome these problems in simulations and a hardware implementation. The results verified the performance of the SSDBI when the modified SPWM was applied; the distortion and the high voltage peak on the AC side were improved, and the modified SPWM control significantly decreased the inverter's THD in both the simulations and the actual measurements. After the proposed modification, the proposed inverter can operate safely and can comply with the IEEE Std 519-1992 and IEEE Std 519-2014 standards.

Institutional Review Board Statement: Not applicable.

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Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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