Mathematical and Computational Applications

MDPI

Article

Single-Objective Optimization of a CMOS VCO Considering PVT and Monte Carlo Simulations

Perla Rubi Castañeda-Aviña [1,†], Esteban Tlelo-Cuautle [1,*,†] and Luis Gerardo de la Fraga [2,†]

[1] Department of Electronics, INAOE, Tonantzintla, Puebla 72840, Mexico; perlacastaneda@inaoep.mx
[2] Computer Science Department, Center for Research and Advanced Studies of the National Polytechnic Institute (CINVESTAV), Ciudad de Mexico 07360, Mexico; fraga@cs.cinvestav.mx
* Correspondence: etlelo@inaoep.mx; Tel.: +52-222-266-3100
† These authors contributed equally to this work.

Received: 23 September 2020; Accepted: 30 November 2020; Published: 3 December 2020

Abstract: The optimization of analog integrated circuits requires to take into account a number of considerations and trade-offs that are specific to each circuit, meaning that each case of design may be subject to different constraints to accomplish target specifications. This paper shows the single-objective optimization of a complementary metal-oxide-semiconductor (CMOS) four-stage voltage-controlled oscillator (VCO) to maximize the oscillation frequency. The stages are designed by using CMOS current-mode logic or differential pairs and are connected in a ring structure. The optimization is performed by applying differential evolution (DE) algorithm, in which the design variables are the control voltage and the transistors' widths and lengths. The objective is maximizing the oscillation frequency under the constraints so that the CMOS VCO be robust to Monte Carlo simulations and to process-voltage-temperature (PVT) variations. The optimization results show that DE provides feasible solutions oscillating at 5 GHz with a wide control voltage range and robust to both Monte Carlo and PVT analyses.

Keywords: VCO; differential evolution; CMOS differential pair; PVT variations; Monte Carlo analysis

1. Introduction

The voltage-controlled oscillator (VCO) is quite useful in applications such as: analog-to-digital converters [1–3], phase-locked loops [4], and so on. The VCO can be implemented by using complementary metal-oxide-semiconductor (CMOS) technology of integrated circuits, as already shown in [5], and also by using LC-tank structures. Several CMOS VCO designs can be classified by using single-ended stages [6,7], differential stages [8,9] and pseudo-differential stages [10]. Among the currently available VCO topologies, the one consisting of a ring structure [11], and using CMOS differential stages has the advantage of providing great immunity to supply disturbances [12]. Other desired features in designing a VCO are associated to accomplish low-power consumption, minimum layout area, high-frequency and wide control voltage range. These target specifications become difficult to achieve due to the continuous down scaling of silicon CMOS technologies. Besides, designing a VCO in a ring topology is frequently a more attractive alternative because it allows accomplishing a wide tuning (control voltage) range, small layout area, high gain, low cost, robustness to variations, simplicity and scalability in nanoscale CMOS processes [13,14]. The three principal causes of alteration on the performace for a circuit are the variations in the fabrication process, power supply and operation temperature, these constitute PVT variations and their impact is increased with the devices' downscaling [15]. Process variations include wafer defects or may be produced by certain chemical procedures causing some circuit's paremeters to change, voltage fluctuations in the circuit take place for a variety of reasons such as supply noise and can be compensated with a voltage

regulator to prevent the transistor's operating point from being affected, last but not least temperature variations can be caused by external sources or by the circuit's own power dissipation. These PVT variations can be minimized by a proper design and layout placement and routing. Among the currently available designs, the authors in [5] introduced a wide-band VCO implemented by CMOS differential stages connected in a ring topology. Other design guidelines to improve the VCO's performance can be found in [16–19].

The oscillation frequency f_{osc} of a VCO can be evaluated by (1), where N indicates the number of stages and τ is a time constant that depends on the associated resistance of the active load and the value of the capacitor load. f_{osc} varies in a range determined by a control voltage V_{ctrl} [14], and depends on the number of CMOS differential stages N, but decreasing N yields a reduction in gain, which may result in the oscillation mitigation. This trade-off can be improved by applying metaheuristics to maximize f_{osc} under a wide range of V_{ctrl}, and low silicon area or number of CMOS differential stages N. Different metaheuristics have been applied to the optimization of CMOS integrated circuits in previous works due to the complexity involved in the design processes [7,20–22]. In this manner, the differential evolution (DE) algorithm is applied herein to vary the sizes of the transistors in the CMOS differential stages to maximize the oscillation frequency of a CMOS VCO f_{osc}. The electrical characteristics of the VCO are evaluated by linking the simulation program with integrated circuit emphasis (SPICE).

$$f_{osc} = \frac{1}{2N \cdot \tau} \tag{1}$$

The rest of the paper is organized as follows: Section 2 describes the considerations taken for the design of both the CMOS differential pair stage and the VCO in a ring topology. The DE algorithm is detailed in Section 4. The single-objective optimization is described in Section 5. Section 6 describes a brief disscussion about this work. Finally, Section 7 summarizes the conclusions.

2. Ring VCO-Based on CMOS Differential Stages

In this paper, the main objective in designing a CMOS differential stage as the one shown in Figure 1, which will be used to implement a ring VCO, is oriented to achieve the highest oscillation frequency f_{osc} given in (1), which is inversely proportional to both the number of CMOS stages N and the propagation delay τ. Supposing N constant, then the delay generated by the differential pair must be minimized [14,23]. Some authors recommend that the delay can be reduced by augmenting the output transconductance g_{ds} of the active MOS transistor and by reducing the equivalent capacitance, where the load capacitance C_L could be the dominant one [13,23,24]. The trade-off here is that augmenting g_{ds} leads to increase the sizes of the MOS transistors and this generates larger parasitic capacitance values. Therefore, this problem is quite suitable for applying metaheuristics, like the DE algorithm.

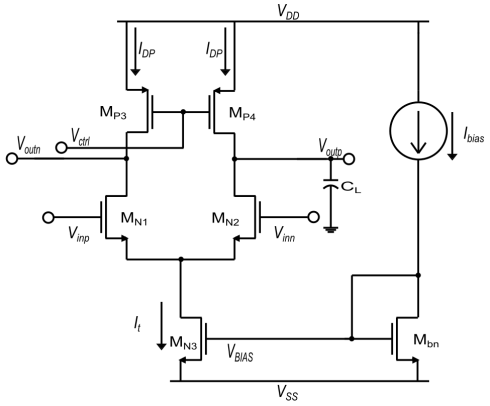


Figure 1. CMOS differential stage with active load and control voltage V_{ctrl}.

If the MOS transistors M_{N1} and M_{N2} operate in their saturation region, then they must accomplish $|V_{DS}| > (|V_{GS}| - |V_{TH}|)$ and $|V_{GS}| > |V_{TH}|$, where the voltages are associated to the drain (D), gate (G) and source (S) terminals of the MOS transistors, and its associated threshold voltage V_{TH}. The width (W) and length (L) sizes of the MOS transistors can be evaluated by (2), where I_D is the drain current, and $\mu_n C_{ox}$ are parameters provided by the CMOS technology foundry. In this work the sizing is performed by using 180 nanometers (nm) from United Microelectronics Corporation (UMC).

$$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox}(|V_{GS}| - |V_{TH}|)^2} \tag{2}$$

As already shown in [5], the active loads are implemented by P-type MOS transistors (M_{P3} and M_{P4}) operating in the triode region, and their sizing accomplish $|V_{DS}| < (|V_{GS}| - |V_{TH}|)$ and (3) [25]. The equivalent resistance is tuned by the control voltage V_{ctrl} at the gates of the PMOS transistors [14,26], and the output conductance of the PMOS transistor can be approached as $1/g_o = 1/g_{ds} = 1/\mu C_{ox}(|V_{ctrl} - V_s| - |V_{th}|)$.

$$I_D = \mu C_{ox} \frac{W}{L} \left[|V_{GS} - V_{TH}| \ |V_{DS}| - \frac{1}{2} |V_{DS}|^2 \right] \tag{3}$$

The propagation delay τ is directly related to the dominant pole, and it has been approximated as in (4), which depends on C_L, the transconductance g_m of the CMOS differential pair, and g_{ds} of the active load [27], so that the reduction of the transistors' sizes leads to an increase of the dominant pole ω_p.

$$\omega_p = \frac{3.29{\cdot}10^{54}(C_D+C_{db2}+C_{db4}+C_L)+2.43{\cdot}10^{44}(gds_2+gds_4)+1.46{\cdot}10^{56}gm_2(C_D+C_L)+3.86{\cdot}10^{45}(gds_4gm_2)+2.51{\cdot}10^{58}(C_Lgds_4gm_2)}{3.29{\cdot}10^{54}(gds_2+gds_4)+1.46{\cdot}10^{56}(gds_4gm_2+gds_2gds_4+gds_4gmb_2)} \tag{4}$$

The delay cell shown in Figure 1 can therefore be characterized by measuring the open-loop gain A_{OL} and the dominant pole ω_p. For instance, the gain-bandwidth product (GBW) of the delay cell, is the frequency at which A_{OL} becomes 0 dB [28]. Its design including process, voltage and temperature (PVT) variations is given in [5], and in this paper the delay cell is optimized to provide the smallest propagation delay τ to increase f_{osc}. The CMOS differential stage with active load is used to design the four-stages ($N = 4$) VCO shown in Figure 2.

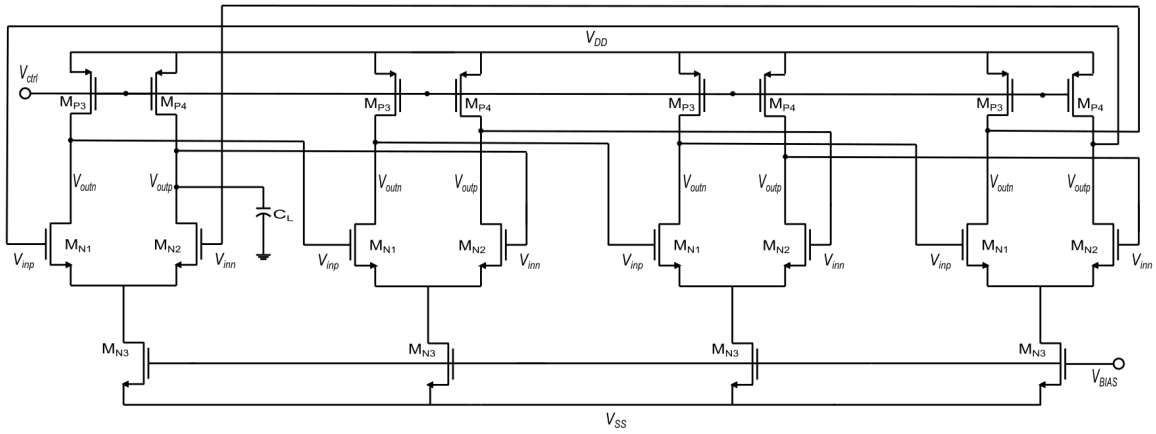


Figure 2. VCO consisting of four CMOS differential stages with active loads, in a ring topology.

3. VCO Optimization Methods

The VCO optimization has been carried out through different approaches, such as metaheuristics [7,22]. In [7], a ring VCO's operation improvement is performed through particle

swam optimization (PSO) and non-dominated sorting genetic algorithm (NSGA-II), to minimize both the phase noise and the power consumption. This is carried out through the use of symbolic modeling techniques to obtain the total output noise density and VCO's phase noise expressions by doing this the run time is reduced and the noise expression is simplified. Achieving also an improvement in tuning range without being an objective and also performing both Monte Carlo and process corners analyses to the final design. Similarly, in [22] the optimal sizing of a differential ring VCO is carried out through multi-objective particle swam optimization (MOPSO) and infeasibility-driven evolutionary algorithm (IDEA) to improve its performances by minimizing both the phase noise and the power consumption while maintaining a given oscillation frequency. Noise modeling is also carried out, to obtain the simplified noise expressions and solve the equations' system the determinate decision diagram (DDD) symbolic technique is used. Furthermore, Monte Carlo and PVT variations analyses were performed to guarantee the design robustness.

In [29], an algorithm that performs RF circuits sizing by using evolutionary strategies and simulating annealing in the search and selection parts, respectively, is implemented in Matlab. The optimization is carried out taking into account the parasitics caused by the passive elements' layout through physical based equivalent parasitic models, by doing this the number of iterations between circuit sizing and layout generation is reduced (reducing the synthesis time) since the difference between synthesis and post-layout results is decreased. The use of simplified models through RF circuit synthesis to approximate layout-induced parasitics lead to unrealistic outcomes. An LC cross-coupled oscillator was optimized using this approach, where the restrictions are: oscillation frequency, phase noise, power consumption, and oscillation amplitude.

In [30], the circuit optimization tool AIDA-C is used to carry out a multi-objective optimization and perform the sizing of an LC-tank VCO with the aim to minimize two compromised objectives, which are phase noise and power consumption. This optimization process achieves a good balance between the two objectives, since there is a trade-off between them, the optimization execution takes several hours to run. In [31], two design tools AIDA and SIDe-O to design a robust LC-tank VCO are introduced. SIDe-O is employed to face the problems relative to the passive elements and through AIDA a robust design is assured due to its corner-aware approach and NSGA-II is employed for the phase noise, power consumption and area minimization, as in the previous case the algorithm takes several hours to run, in both algorithms none of the objectives are focused on achieving a higher oscillation frequency.

4. Problem Formulation for the Optimization of the VCO by Applying DE

The single-objective function $g(x)$ is formulated by (5), where μ is a constant established to one and $r(x)$ stands for the constraints. One can see that when all the constraints are fulfilled then the second term of the function is equal to 0 and the objective function is the oscillating-period of the ring VCO $g(x) = f(x)$. Therefore, the sizing optimization problem can be defined by (6).

$$g(x) = f(x) + \mu \sum r^2(x) \tag{5}$$

$$\begin{aligned} &\text{Search} : x = [W_1, W_3, L_1, L_3, V_{ctrl}] \\ &Minimize : g(x) \\ &\text{Subject to} : 5 > A_{OL} > 1, \\ &V_{DS} \leq V_{GS} - V_{TH} \quad \text{for} \quad M_{P3} \quad \text{and} \quad M_{P4}, \\ &V_{DS} \geq V_{GS} - V_{TH} \quad \text{otherwise}, \\ &W_{min} < W < W_{max}, \\ &L_{min} < L < L_{max}, \\ &V_{SS} < V_{ctrl} < V_{DD} \end{aligned} \tag{6}$$

By applying the DE algorithm, which is described below, the sizing optimization process requires a population of I_n individuals, a maximum number of generations $maxGen$, and the objective function

$g(x)$. Two of the main factors guaranteeing that global optimality is achievable by a metaheuristic like DE are the selection of the best solutions and randomization, where the former ensures that the solution converges to an optimum value while the later keeps the solution from getting halted at local optima [32]. To maximize f_{osc}, this paper minimizes the oscillating period of the ring VCO, which is subject to the constraints of maintaining the load MOS transistors M_{P3} and M_{P4} operating in the triode region and the rest N-type MOS transistors operating in the saturation region. The SPICE simulator is linked within the optimization loop to evaluate the delay cell's gain A_{OL} to be maintained within 1 and 5 dB.

The DE algorithm is a metaheuristic that performs an iterative optimization based on the evolution of a population of individuals under the concept of competition. The initial population is randomly generated where each individual represents a tentative solution that is associated to a fitness value through an objective function to point out the individual's suitability to a particular problem. The individuals with better fitness are more likely to be selected as parents, the chosen ones are reproduced using genetic operators (crossover, mutation) to produce new offsprings, which will also be evaluated to determine its survival. This represents a generation and this process is repeated until a stop criteria is met [33–36]. The DE algorithm is suitable for continuous optimization problems, like sizing analog CMOS integrated circuits as the VCO. In the DE algorithm, a vector population is altered through a vector of differences, which translates to a two operators: the first one being a recombination operator of two or more solutions and the second one coming as a self-referential mutation operator that conducts the algorithm unto finding acceptable solutions. Each individual is encoded as a vector of real numbers that are within the limits defined for each design variable (as the widths (W) and lengths (L) of the MOS transistors). The crossover operator defines the offspring-associated variable to be a a linear combination of three randomly selected individuals or an inheritance of its parents value while guaranteeing that at least one of the offspring's variable will be different from its parent. A scaling factor is employed to prevent stagnation of the search process [33,37].

In the DE algorithm, if a variable's magnitude is out of range, the recombination and mutation operators can be employed to reset the value. For instance the value can be established to the limit it exceeds, however this diminish the population's diversity. Other approaches reset it to a random value or initializing this value to a mid point between its previous value and the violated bound. In the latter the limits are approached asymptotically leading to diminish the amount of disruption [33]. In our current DE implementation, the individual is reset randomly within the search bounds. Other guidelines to design a DE algorithm may include to set the population number to ten times the amount of decision variables and initialize the weighting factor, P_f to 0.8 and the crossover constant, P_c to 0.9. If no convergence is achieved an increase in population may be necessary, however frequently the weighting factor is the one that has to be modified to be a little lower or higher than 0.8. The relation between convergence speed and robustness features is a trade-off, if the amount of population increments and the weighting factor decrements then convergence is more likely to occur but within a longer period of time. The performance of DE is more sensitive to the value of the weighting factor than the value of the crossover constant, and the range of both is generally in [0.5, 1]. A faster convergence may occur with higher values of the crossover constant [33].

The usefulness of the DE algorithm in sizing CMOS integrated circuits has been proved in [38–40]. Algorithm 1 describes its adaptation to maximize the oscillation frequency of the ring VCO shown in Figure 2. As mentioned above, herein the objective function is associated to minimize the propagation delay τ that is accomplished by measuring the oscillating period by using SPICE.

Algorithm 1 DE pseudocode.

```
procedure DE(I_n, maxGen, g(x))
    Generate the SPICE netlist of the ring VCO
    for i = 1 : I_n do
        Initialize the population randomly and replace the initial individuals (Ws, Ls, V_ctrl) into the netlist
        Evaluate the VCO's delay cell and check the constraints
        if constraints = 0 then
            Simulate the VCO and evaluate the objective function
        end if
    end for
    while j < maxGen do
        for i = 1 : I_n do
            Create a trial solution from three randomly selected parents using (7)
            Apply crossover using (8)
            Replace the new individual into the netlist
            Simulate the VCO's delay cell and count the constraints
            if constraints = 0 then
                Simulate the VCO and evaluate the objective function
            end if
            if the individual's objective function is lower than that of the parent then
                The new individual replaces the parent using (9)
            end if
        end for
    end while
end procedure
```

In the optimization process the individuals I_n of the population generated by the DE algorithm are replaced into the netlist file of the VCO's delay cell and each individual is simulated in SPICE. The electrical characteristics are obtained from the (.lis) output SPICE-file to verify that all the MOS transistors are working in the appropriate region of operation and that the gain is within the range of $5 > A_{OL} > 1$. A flag assigns 0 to a fulfilled constraint and 1 to a not fulfilled one. The period of the sinusoidal wave is associated to the function $f(x)$. If the VCO is not oscillating then a high value is assigned to $f(x)$. In the DE algorithm each individual is mutated to generate an adaptive solution v_{ij} from three randomly selected parents, as given in (7). Afterwards, the crossover takes place creating a trial solution, through the recombination of a mutated solution v_{ij} with an individual x_{ij}, given by (8). Finally, the replacement is carried out employing an elitist selection, where the new individual will replace its parent if its objective function value is better than the parent, as given in (9) [33].

$$v_{ij} = x_{r3j} + P_f(x_{r1j} - x_{r2j}) \tag{7}$$

$$u_{ij} = \begin{cases} v_{ij} & \text{if} \quad rand_j[0,1] < P_c \quad \text{or} \quad j = j_{rand} \\ x_{ij} & \text{otherwise} \end{cases} \tag{8}$$

$$x_i(t+1) = \begin{cases} u_i(t+1) & \text{if} \quad f(u_i(t+1)) < f(x_i(t)) \\ x_i(t) & \text{otherwise} \end{cases} \tag{9}$$

5. Optimizing the CMOS VCO by Applying DE Algorithm

The sizing optimization problem defined by (6), requires the sizes of the design variables (widths W and lengths L) of the MOS transistors, but one must determine the search space ranges. For instance, the limits of the sizes are set to: $2\lambda \leq W \leq 1000\lambda$ and $2\lambda \leq L \leq 10\lambda$, respectively, where λ = 90 nm for the UMC CMOS technology of 180 nm. Another design variable is the control voltage, which bounds are set to $V_{SS} \leq V_{ctrl} \leq V_{DD}$, and where $V_{SS} = -0.9$ V is the lower supply voltage and $V_{DD} = 0.9$ V the higher supply voltage.

The DE algorithm was calibrated by adjusting P_c, P_f and I_n to 0.7, 0.6 and 50, respectively. The maximum number of generations is set to 50. In total, 30 runs of DE were performed. The best feasible solution provided an oscillation frequency of 5 GHz, as shown in Figure 3. In such a case the obtained parameter values are: $I_{bias} = I_{MN3} = 4$ mA, $W_{MN1} = W_{MN2} = 40$ µm, $W_{MN3} = 500$ µm, $W_{MP3} = W_{MP4} = 17$ µm, $L_{MN1} = L_{MN2} = L_{MN3} = L_{MP3} = L_{MP4} = 0.18$ µm, $V_{ctrl} = -0.8$ V and $C_L = 31.39$ fF. The V_{BIAS} is created from Figure 1, in which the CMOS differential stage with active load is biased with $I_{bias} = 2$ mA, and the sizes of M_{bn} are $W = 200$ µm and $L = 180$ µm.

The SPICE simulation result of the best solution of the DE algorithm is shown in Figure 3.

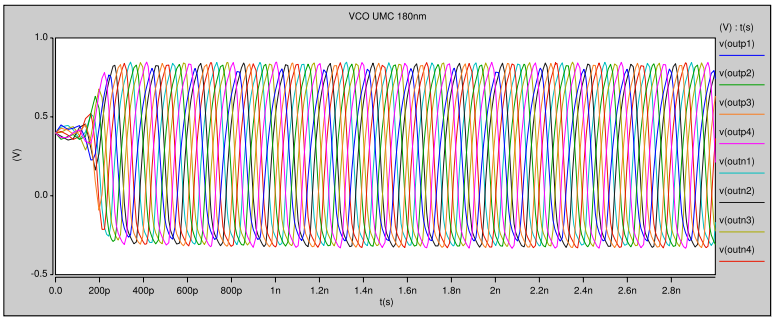


Figure 3. VCO's oscillation frequency provided by the best solution of the DE algorithm.

Monte Carlo is an integrated circuits' statistical analysis in which a circuit devices' parameters and mismatch are varied randomly. Monte Carlo simulation allows the designer to consider the possible effects of a random variation of certain circuit's parameter over its performance. Monte Carlo analysis is carried out through the variation of W and L for each one of the 30 feasible solutions over 1000 runs, and considering a Gaussian distribution with 10% deviation. The outcome of the Monte Carlo simulations is employed to compute the mean and the standard deviation of the objetive function value, those results are sketched in Figure 4.

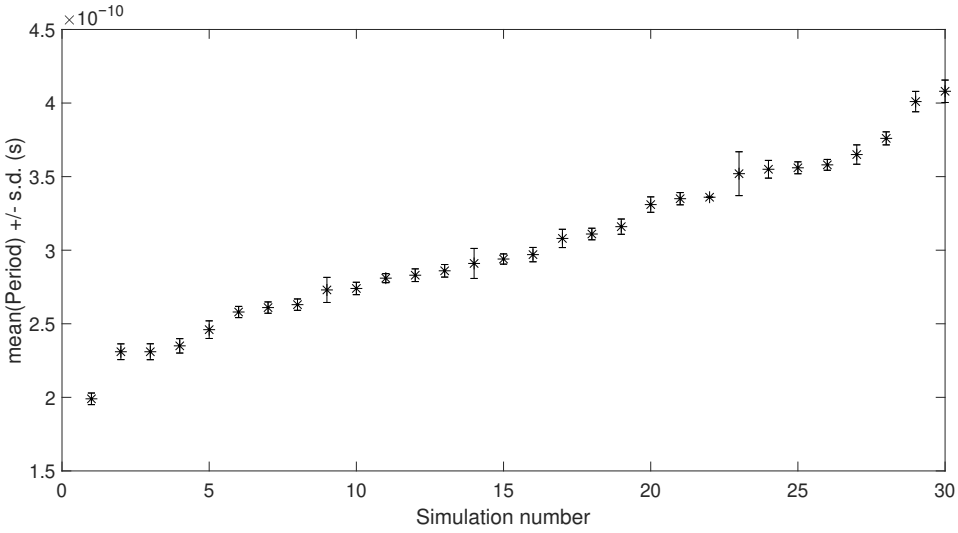


Figure 4. Mean and standard deviation of the Monte Carlo analysis for 30 feasible sized solutions of the DE algorithm. The best solution is the one with the lowest period (corresponding to a greater oscillation frequency).

The feasible sized solutions that accomplished the lower time delay τ of the CMOS differential stages are analyzed and their statistics related to the mean and standard deviation of the period of the sinusoidal wave are summarized in Table 1. From this table, the Monte Carlo simulation of the best solution of the DE algorithm is shown in Figure 5.

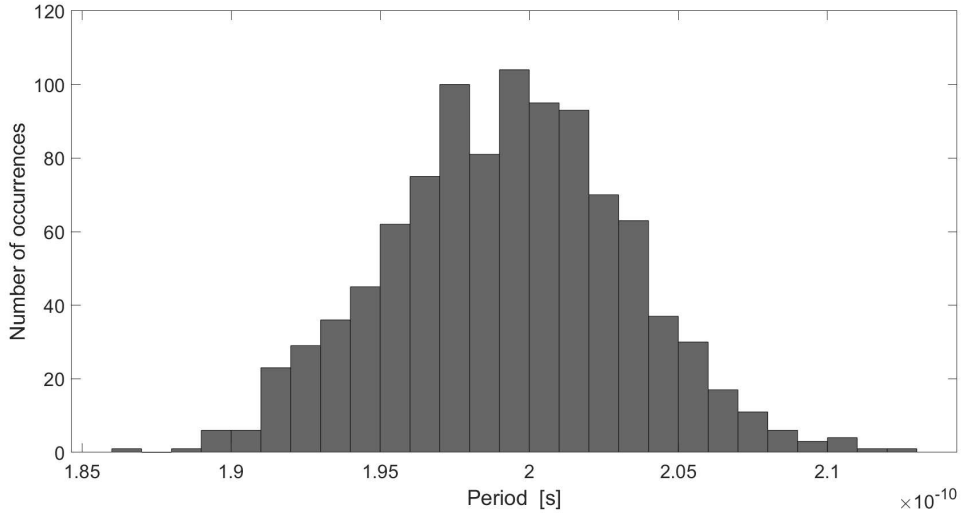


Figure 5. Monte Carlo simulation of the best feasible sized solution of the DE algorithm.

Table 1. Statistics of the Monte Carlo analysis of the best 5 feasible sized solutions provided by the DE algorithm.

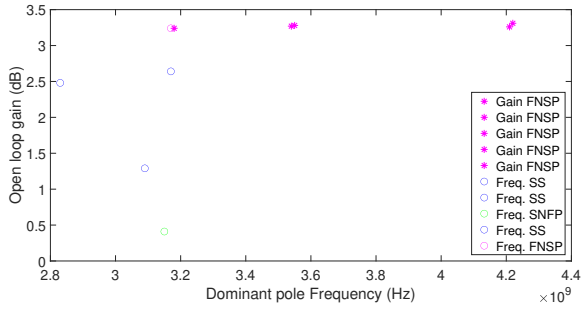
Solution	Minimum (ns)	Maximum (ns)	Mean (ns)	Variance	Standard Deviation
1	0.187	0.213	0.199	1.55×10^{-23}	3.94×10^{-12}
2	0.214	0.248	0.231	2.86×10^{-23}	5.35×10^{-12}
3	0.214	0.249	0.231	2.93×10^{-23}	5.41×10^{-12}
4	0.219	0.251	0.235	2.39×10^{-23}	4.89×10^{-12}
5	0.226	0.265	0.246	3.59×10^{-23}	5.99×10^{-12}

The parameters of each one of the five best feasible sized solutions and the simulated period, frequency and gain of the VCO and the CMOS delay cell, respectively, are summarized in Table 2.

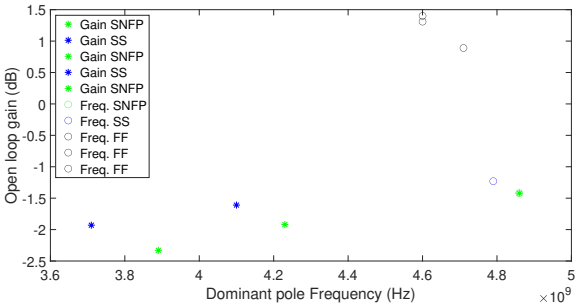
Table 2. Best 5 feasible sized solution design parameters provided by the DE algorithm.

Solution	W_{MN1} (µm)	W_{MP3} (µm)	L_{MN1} (µm)	L_{MP3} (µm)	V_{ctrl} (V)	C_L (fF)	Period (ns)	Frequency (GHz)	A_{OL} (dB)
1	40	17	0.18	0.18	−0.80	31.39	0.199	5.02	1.89
2	45	20	0.18	0.18	−0.56	35.22	0.232	4.32	3.39
3	61	26	0.18	0.18	−0.56	54.69	0.232	4.30	1.78
4	69	22	0.18	0.18	−0.79	96.17	0.235	4.25	2.26
5	46	20	0.18	0.18	−0.51	36.19	0.246	4.07	4.41

A PVT simulation of the ten best feasible sized solutions was also performed to assure that the CMOS VCO is robust to variations. The PVT variations are simulated by setting $V_{ctrl} = -0.8$ V. Considering five process corners (typical-typical (TT), slow-slow (SS), slow N-type MOS transistor and fast P-type MOS transistor (SNFP), fast N-type MOS transistor and slow P-type MOS transistor (FNSP), and fast-fast (FF)), three voltage variations ($\pm$10% of $\pm V_{supply} = 0.9$ V), and three temperature variations ($T- = -20$ °C, $T = 60$ °C and $T+ = 120$ °C) [41], Figure 6 shows the higher and lower gain and oscillation frequency values provided by the DE algorithm. Table 3 summarizes PVT simulation results, where the five corners (TT, SS, SNFP, FNSP and FF) correspond to the MOS transistor models provided by the UMC foundry.



(**a**)



(**b**)

Figure 6. (**a**) Higher and (**b**) lower gains and dominant pole frequencies, for the solution 1 CMOS delay cell designed with United Microelectronics Corporation (UMC) technology of 180 nm by applying DE algorithm.

Table 3. Open-loop gain and dominant pole frequency over PVT variations with $V_{ctrl} = -0.8$ V.

Solution	Corners	Temperature	T−			T			T+		
		Voltage	V−	V	V+	V−	V	V+	V−	V	V+
1	TT	A_{OL} (dB)	0.82	1.88	2.06	0.55	1.74	1.89	0.24	1.61	1.78
		ω_p (GHz)	4.54	4.24	4.21	3.90	3.58	3.56	3.58	3.22	3.19
	SS	A_{OL} (dB)	−1.23	2.17	2.81	−1.61	1.76	2.64	−1.93	1.29	2.48
		ω_p (GHz)	4.79	3.92	3.77	4.10	3.37	3.17	3.71	3.09	2.83
	SNFP	A_{OL} (dB)	−1.42	0.51	0.88	−1.92	0.20	0.60	−2.33	−0.085	0.41
		ω_p (GHz)	4.86	4.25	4.16	4.23	3.61	3.52	3.89	3.28	3.15
	FNSP	A_{OL} (dB)	2.66	3.26	3.31	2.64	3.27	3.28	2.49	3.24	3.24
		ω_p (GHz)	4.35	4.21	4.22	3.68	3.54	3.55	3.34	3.17	3.18
	FF	A_{OL} (dB)	0.89	1.31	1.40	0.77	1.15	1.20	0.64	1.05	1.08
		ω_p (GHz)	4.71	4.60	4.60	4.00	3.91	3.91	3.63	3.52	3.53
2	TT	A_{OL} (dB)	2.75	3.22	3.02	2.77	3.31	3.06	2.61	3.3	3.07
		ω_p (GHz)	4.21	4.1	4.17	3.51	3.43	3.49	3.23	3.06	3.12
	SS	A_{OL} (dB)	1.62	4.23	4.25	1.49	4.24	4.38	1.21	4.01	4.4
		ω_p (GHz)	4.16	3.62	3.63	3.53	3.04	3.01	3.21	2.75	2.67
	SNFP	A_{OL} (dB)	0.42	1.67	1.68	0.16	1.57	1.57	−0.16	1.43	1.49
		ω_p (GHz)	4.51	4.16	4.17	3.86	3.5	3.5	3.53	3.15	3.13
	FNSP	A_{OL} (dB)	4.93	4.91	4.51	5.27	5.21	4.74	5.29	5.34	4.86
		ω_p (GHz)	3.97	3.99	4.11	3.3	3.31	3.42	2.96	2.94	3.04
	FF	A_{OL} (dB)	2.23	2.27	2.08	2.29	2.28	2.05	2.26	2.28	2.03
		ω_p (GHz)	4.55	4.56	4.64	3.84	3.85	3.92	3.45	3.45	3.52

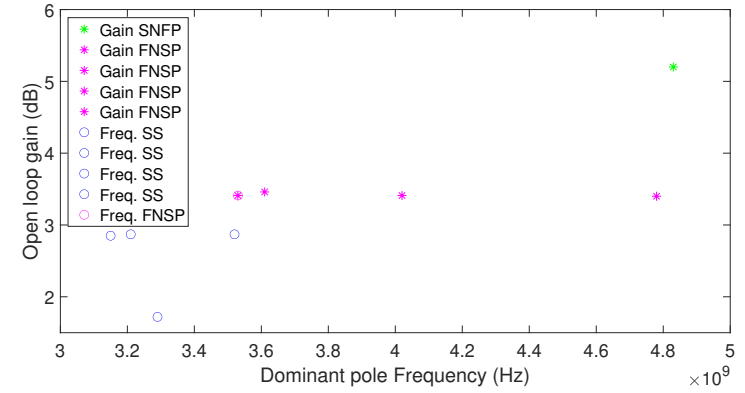
Table 3. *Cont.*

Solution	Corners	Temperature	T−			T			T+		
		Voltage	V−	V	V+	V−	V	V+	V−	V	V+
3	TT	A_{OL} (dB)	1.57	1.7	1.52	1.63	1.69	1.45	1.64	1.7	1.43
		ω_p (GHz)	4.6	4.66	4.8	3.85	3.91	4.04	3.47	3.51	3.62
	SS	A_{OL} (dB)	1.52	2.65	2.5	1.5	2.65	2.47	1.36	2.62	2.45
		ω_p (GHz)	4.22	4.06	4.17	3.54	3.38	3.47	3.2	3.02	3.09
	SNFP	A_{OL} (dB)	−0.1	0.42	0.35	−0.18	0.3	0.18	−0.28	0.24	0.1
		ω_p (GHz)	4.73	4.68	4.78	3.99	3.93	4.02	3.61	3.52	3.61
	FNSP	A_{OL} (dB)	3.19	3.07	2.77	3.39	3.18	2.82	3.49	3.26	2.87
		ω_p (GHz)	4.45	4.58	4.76	3.72	3.84	3.99	3.33	3.44	3.58
	FF	A_{OL} (dB)	0.89	0.87	0.72	0.91	0.81	0.61	0.93	0.82	0.59
		ω_p (GHz)	5.11	5.22	5.37	4.32	4.43	4.55	3.9	3.99	4.11
4	TT	A_{OL} (dB)	1.9	2.25	2.3	1.91	2.16	2.13	1.94	2.15	2.08
		ω_p (GHz)	4.77	4.81	4.93	4	4.05	4.16	3.6	3.64	3.74
	SS	A_{OL} (dB)	1.82	2.94	3.06	1.79	2.87	2.92	1.72	2.85	2.87
		ω_p (GHz)	4.37	4.23	4.31	3.66	3.52	3.6	3.29	3.15	3.21
	SNFP	A_{OL} (dB)	5.2	1.15	1.27	0.43	0.97	1.02	0.39	0.91	0.91
		ω_p (GHz)	4.83	4.79	4.88	4.07	4.04	4.12	3.67	3.62	3.7
	FNSP	A_{OL} (dB)	3.21	3.4	3.4	3.32	3.41	3.32	3.41	3.46	3.33
		ω_p (GHz)	4.69	4.78	4.91	3.93	4.02	4.14	3.53	3.61	3.73
	FF	A_{OL} (dB)	1.42	1.62	1.68	1.37	1.48	1.47	1.4	1.47	1.41
		ω_p (GHz)	5.28	5.36	5.49	4.47	4.56	4.67	4.04	4.12	4.23
5	TT	A_{OL} (dB)	3.89	4.17	3.82	4	4.34	3.94	3.86	4.38	3.98
		ω_p (GHz)	4.02	3.96	4.07	3.38	3.3	3.39	3.06	2.94	3.02
	SS	A_{OL} (dB)	3.05	5.53	5.3	3.04	5.71	5.57	2.77	5.55	5.67
		ω_p (GHz)	3.89	3.44	3.49	3.29	2.85	2.87	3	2.57	2.53
	SNFP	A_{OL} (dB)	1.39	2.5	2.38	1.19	2.45	2.33	0.88	2.34	2.28
		ω_p (GHz)	4.34	4.05	4.09	3.7	3.4	3.43	3.38	3.05	3.06
	FNSP	A_{OL} (dB)	6.37	6.07	5.45	6.9	6.53	5.8	6.94	6.72	5.98
		ω_p (GHz)	3.73	3.81	3.97	3.06	3.13	3.28	2.73	2.76	2.9
	FF	A_{OL} (dB)	3.14	3.04	2.74	3.25	3.11	2.76	3.24	3.12	2.77
		ω_p (GHz)	4.41	4.45	4.56	3.7	3.74	3.84	3.33	3.35	3.44

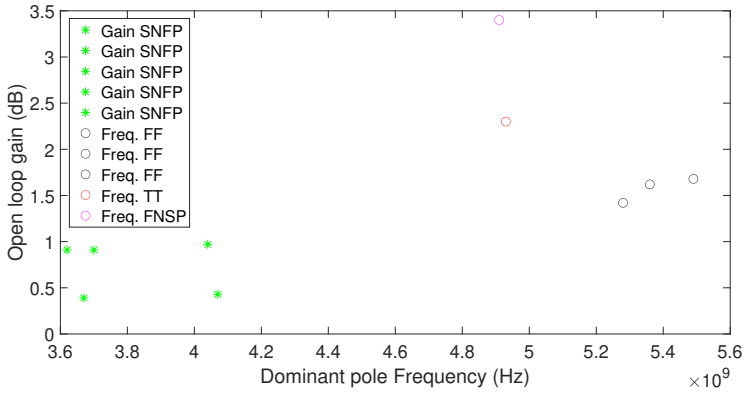
As one can see from Table 3 solution number 4 is the most robust to PVT. This solution has the greater frequency with all the gains been positive. Figure 6 depicts the higher and lower gains and dominant pole frequencies for solution number 1 since this is the one that provides the higher oscillation frequency, as one can see the greater gains occur at the FNSP process-corner (in Figure 6a) while the lower gains for the most part occur at SNFP process-corner (see Figure 6b. Furthermore, the greater ω_p takes place mostly at FF process-corner, while the lower ω_p mostly takes place at SS process-corner.

Figure 7 depicts the higher and lower gains and dominant pole frequencies for solution number 4 since is the most robust one. As one can see in Figure 7a the greater gains occur mostly at the FNSP process-corner, while the lower gains, in Figure 7b, for the most part occur at SNFP process-corner. The greater ω_p takes place mostly at the FF process-corner (in Figure 7b), while the lower ω_p mostly takes place at the SS process-corner (in Figure 7a).

Table 4 shows the oscillation frequency and power dissipation corresponding to each control voltage V_{ctrl} value for the best 5 feasible sized solutions.



(**a**)



(**b**)

Figure 7. (**a**) Higher and (**b**) lower gains and dominant pole frequencies, for the solution 4 CMOS delay cell designed with UMC technology of 180 nm by applying DE algorithm.

Table 4. Oscillation frequency and power dissipation to the corresponding V_{ctrl}.

Solution	Parameter	Measured Oscillation Frequency and Power Dissipation								
1	V_{ctrl} (V)	−0.53	−0.55	−0.6	−0.65	−0.7	−0.75	−0.8	−0.85	−0.9
	f_{osc} (GHz)	4.03	4.08	4.27	4.48	4.69	4.83	5	5.15	5.32
	P_{cons} (mW)	30.6	31	32.1	33.1	33.9	34.6	35.3	35.8	36.3
2	V_{ctrl} (V)	−0.41	−0.5	−0.6	−0.65	−0.7	−0.75	−0.8	−0.85	−0.9
	f_{osc} (GHz)	3.56	4.02	4.46	4.65	4.83	5	5.18	5.29	5.35
	P_{cons} (mW)	30.8	33.1	35.1	35.9	36.6	37.2	37.7	38.1	38.4
3	V_{ctrl} (V)	−0.27	−0.3	−0.4	−0.5	−0.56	−0.6	−0.7	−0.8	−0.9
	f_{osc} (GHz)	2.91	3.07	3.61	4.05	4.3	4.37	4.78	5.1	5.38
	P_{cons} (mW)	31.9	33	35.9	38	38.9	39.4	40.3	40.9	41.2
4	V_{ctrl} (V)	−0.36	−0.4	−0.5	−0.6	−0.7	−0.75	−0.8	−0.85	−0.9
	f_{osc} (GHz)	2.72	2.88	3.25	3.6	3.98	4.08	4.26	4.33	4.44
	P_{cons} (mW)	32	33.2	35.7	37.5	38.9	39.4	39.8	40.2	40.5
5	V_{ctrl} (V)	−0.41	−0.5	−0.6	−0.65	−0.7	−0.75	−0.8	−0.85	−0.9
	f_{osc} (GHz)	3.56	3.97	4.39	4.57	4.74	4.93	5.1	5.21	5.38
	P_{cons} (mW)	30.8	33.1	35.2	36	36.7	37.2	37.7	38.1	38.5

6. Discussion

The proposed methodology to circuit design here is: (1) apply DE at least 30 times. This give us 30 solutions to our design problem, considering only the best solutions according to the objective function. (2) From the best 10 solutions, apply the Monte Carlo (MT) analysis. (3) From the best 10 solutions of the MC analysis apply the PVT analysis. Finally, (4) select the best solution according to the showed variations in the PVT analysis.

We apply the MC analysis to vary the dimension for all the circuit's transistors up to 10% of their value. As shown in Figure 5, these variations are not too high to move the operating point of the MOS transistors, and still the order of the obtained solution according to the objective function is kept after the MC analysis.

Then we apply the PVT analysis: The five process corners employed for this simulation are the ones provided by the foundry which are typical-typical (TT), slow NMOS transistor and fast PMOS transistor (SNFP), fast NMOS transistor and slow PMOS transistor (FNSP), slow-slow (SS) and fast-fast (FF), these account for the variation of fabrication parameters. A circuit can also be subject to temperature (considering three temperatures -20°, 60° and 120°) and voltage variations (considering a variation of $\pm 10\%$) in its operation environment therefore each corner is simulated with each temperature and voltage variation.

The chosen solution is the one with lower time period (or higher operation frequency) while all the gains are positive, within the gain constraint of $1 < A_{OL} < 5$.

In Table 3 are shown only the first five solutions, although 10 analyses were performed.

We use a DE version programmed in C language. One single run (50 individuals, and 50 generations) took around 32 min.

The MC and PVT analyses could be incorporated within the optimization loop, as another set of constraints. This idea also will increase the simulation time to several hours. We are going to analyse this idea as a future work.

7. Conclusions

The application of the DE algorithm has proven to be effective in the minimization of the time period of a CMOS VCO designed with CMOS differential delay cells in a ring topology. We use the Monte Carlo analysis over the sized transistor dimensions to rank the obtained DE solutions. Then we apply the PVT analyses to the 10 best solutions according to the Monte Carlo analysis. The most robust solution to PVT, provides an oscillation frequency up to 4.25 GHz (corresponding to a time period of 0.235 ns), and it has a wider tunning range, of 2.72–4.44 GHz, corresponding to V_{ctrl} of -0.36 to -0.9V.

Author Contributions: Investigation, P.R.C.-A., E.T.-C., and L.G.d.l.F.; and Writing—review and editing, P.R.C.-A., E.T.-C., and L.G.d.l.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Al-Tamimi, K.M.; El-Sankary, K.; Fouzar, Y. VCO-Based ADC With Built-In Supply Noise Immunity Using Injection-Locked Ring Oscillators. *IEEE Trans. Circuits Syst. Express Briefs* **2019**, *66*, 1089–1093. [CrossRef]
2. Ding, Z.; Zhou, X.; Li, Q. A 0.5-1.1-V Adaptive Bypassing SAR ADC Utilizing the Oscillation-Cycle Information of a VCO-Based Comparator. *IEEE J. Solid State Circuits* **2019**, *54*, 968–977. [CrossRef]
3. Danesh, M.; Sanyal, A. 0.13 pW/Hz Ring VCO-Based Continuous-Time Read-Out ADC for Bio-Impedance Measurement. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**. [CrossRef]
4. Sharma, J.; Krishnaswamy, H. A 2.4-GHz Reference-Sampling Phase-Locked Loop That Simultaneously Achieves Low-Noise and Low-Spur Performance. *IEEE J. Solid State Circuits* **2019**, *54*, 1407–1424. [CrossRef]

5. Tlelo-Cuautle, E.; Castañeda-Aviña, P.R.; Trejo-Guerra, R.; Carbajal-Gómez, V.H. Design of a Wide-Band Voltage-Controlled Ring Oscillator Implemented in 180 nm CMOS Technology. *Electronics* **2019**, *8*, 1156. [CrossRef]
6. Lee, I.Y.; Im, D. Low phase noise ring VCO employing input-coupled dynamic current source. *Electron. Lett.* **2019**, *56*, 76–78. [CrossRef]
7. Panda, M.; Patnaik, S.K.; Mal, A.K. Performance enhancement of a VCO using symbolic modelling and optimisation. *IET Circuits Devices Syst.* **2017**, *12*, 196–202. [CrossRef]
8. Gui, X.; Tang, R.; Zhang, Y.; Li, D.; Geng, L. A Voltage-Controlled Ring Oscillator With VCO-Gain Variation Compensation. *IEEE Microw. Wirel. Components Lett.* **2020**, *30*, 288–291. [CrossRef]
9. Jung, O.Y.; Seok, H.G.; Dissanayake, A.; Lee, S.G. A 45-μ W, 162.1-dBc/Hz FoM, 490-MHz Two-Stage Differential Ring VCO Without a Cross-Coupled Latch. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *65*, 1579–1583. [CrossRef]
10. Jiang, T.; Yin, J.; Mak, P.I.; Martins, R.P. A 0.5-V 0.4-to-1.6-GHz 8-phase bootstrap ring-VCO using inherent non-overlapping clocks achieving a 162.2-dBc/Hz FoM. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *66*, 157–161. [CrossRef]
11. Sun, I.F.; Yin, J.; Mak, P.I.; Martins, R.P. A Comparative Study of 8-Phase Feedforward-Coupling Ring VCOs. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 527–531. [CrossRef]
12. Abidi, A.A. Phase noise and jitter in CMOS ring oscillators. *IEEE J. Solid State Circuits* **2006**, *41*, 1803–1816. [CrossRef]
13. Gui, X.; Green, M.M. Design of CML ring oscillators with low supply sensitivity. *IEEE Trans. Circuits Syst. Regul. Pap.* **2013**, *60*, 1753–1763. [CrossRef]
14. Zhang, Z.; Chen, L.; Djahanshahi, H. A SEE Insensitive CML Voltage Controlled Oscillator in 65 nm CMOS. In Proceedings of the 2018 IEEE Canadian Conference on Electrical & Computer Engineering (CCECE), Quebec City, QC, Canada, 13–16 May 2018; pp. 1–4. [CrossRef]
15. Amaya, A.; Villota, F.; Espinosa, G. A robust to PVT fully-differential amplifier in 45 nm SOI-CMOS technology. In Proceedings of the 2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS), Cusco, Peru, 27 February–1 March 2013; pp. 1–4.
16. Hsieh, J.Y.; Lin, K.Y. A 0.7-mW LC Voltage-Controlled Oscillator Leveraging Switched Biasing Technique for Low Phase Noise. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1307–1310. [CrossRef]
17. Basaligheh, A.; Saffari, P.; Winkler, W.; Moez, K. A Wide Tuning Range, Low Phase Noise, and Area Efficient Dual-Band Millimeter-Wave CMOS VCO Based on Switching Cores. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 2888–2897. [CrossRef]
18. Poor, M.A.; Esmaeeli, O.; Sheikhaei, S. A low phase noise quadrature VCO using superharmonic injection, current reuse, and negative resistance techniques in CMOS technology. *Analog. Integr. Circuits Signal Process.* **2019**, *99*, 633–644. [CrossRef]
19. Ghorbel, I.; Haddad, F.; Rahajandraibe, W.; Loulou, M. Design Methodology of Ultra-Low-Power LC-VCOs for IoT Applications. *J. Circuits Syst. Comput.* **2019**, *28*. [CrossRef]
20. de Melo, J.L.; Pereira, N.; Leitão, P.V.; Paulino, N.; Goes, J. A Systematic Design Methodology for Optimization of Sigma-Delta Modulators Based on an Evolutionary Algorithm. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3544–3556. [CrossRef]
21. Vural, R.A.; Yildirim, T.; Kadioglu, T.; Basargan, A. Performance evaluation of evolutionary algorithms for optimal filter design. *IEEE Trans. Evol. Comput.* **2011**, *16*, 135–147. [CrossRef]
22. Panda, M.; Patnaik, S.K.; Mal, A.K.; Ghosh, S. Fast and optimised design of a differential VCO using symbolic technique and multi objective algorithms. *IET Circuits Devices Syst.* **2019**, *13*, 1187–1195. [CrossRef]
23. Heydari, P.; Mohanavelu, R. Design of ultrahigh-speed low-voltage CMOS CML buffers and latches. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2004**, *12*, 1081–1093. [CrossRef]
24. Kumar, M. Design of Linear Low-Power Voltage-Controlled Oscillator with I-MOS Varactor and Back-Gate Tuning. *Circuits Syst. Signal Process.* **2018**, 1–17. [CrossRef]
25. Sedra, A.S.; Smith, K.C. *Microelectronic Circuits*; Holt, Rinehart and Winston: New York, NY, USA, 1982.
26. Jyotsna, K.; Kumar, P.S.; Madhavi, B. Implementation of 8 Bit Microprocessor Using Current Mode Logic (CML) Approach. In Proceedings of the 2018 3rd International Conference for Convergence in Technology (I2CT), Pune, India, 6–8 April 2018; pp. 1–6. [CrossRef]
27. Palumbo, G.; Pennisi, S. *Feedback Amplifiers: Theory and Design*; Springer: Berlin/Heisenberg, Germany, 2002.

28. Maloberti, F. *Analog Design for CMOS VLSI Systems*; Springer: Berlin/Heisenberg, Germany, 2006; Volume 646. [CrossRef]
29. Afacan, E.; Dündar, G. A mixed domain sizing approach for RF circuit synthesis. In Proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Kosice, Slovakia, 20–22 April 2016; pp. 1–4.
30. Póvoa, R.; Lourenço, R.; Lourenço, N.; Canelas, A.; Martins, R.; Horta, N. LC-VCO automatic synthesis using multi-objective evolutionary techniques. In Proceedings of the 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Victoria, Australia, 1–5 June 2014; pp. 293–296.
31. Passos, F.; Martins, R.; Lourenço, N.; Roca, E.; Povoa, R.; Canelas, A.; Castro-López, R.; Horta, N.; Fernández, F.V. Enhanced systematic design of a voltage controlled oscillator using a two-step optimization methodology. *Integration* **2018**, *63*, 351–361. [CrossRef]
32. Yang, X.S. *Engineering Optimization: An Introduction with Metaheuristic Applications*; John Wiley & Sons: Hoboken, NJ, USA, 2010. [CrossRef]
33. Talbi, E.G. *Metaheuristics: From Design to Implementation*; John Wiley & Sons: Hoboken, NJ, USA, 2009; Volume 74. [CrossRef]
34. Dasgupta, D.; Michalewicz, Z. Evolutionary algorithms—An overview. In *Evolutionary Algorithms in Engineering Applications*; Springer: Berlin/Heisenberg, Germany, 1997; pp. 3–28. [CrossRef]
35. Coello, C.A.C. An introduction to evolutionary algorithms and their applications. In *International Symposium and School on Advancex Distributed Systems*; Springer: Berlin/Heisenberg, Germany, 2005; pp. 425–442. [CrossRef]
36. Woldesenbet, Y.G.; Yen, G.G.; Tessema, B.G. Constraint handling in multiobjective evolutionary optimization. *IEEE Trans. Evol. Comput.* **2009**, *13*, 514–525. [CrossRef]
37. Yu, X.; Gen, M. *Introduction to Evolutionary Algorithms*; Springer: Berlin/Heisenberg, Germany, 2010. [CrossRef]
38. Elhajjami, I.; Benhala, B.; Bouyghf, H. Optimal Design of RF Integrated Inductors via Differential Evolution Algorithm. In Proceedings of the 2020 1st International Conference on Innovative Research in Applied Science, Engineering and Technology (IRASET), Meknes, Morocco, 16–19 April 2020; pp. 1–6. [CrossRef]
39. Li, J.; Zeng, Y.; Wu, H.; Li, R.; Zhang, J.; Tan, H.Z. Performance optimization for LDO regulator based on the differential evolution. In Proceedings of the 2019 IEEE 13th International Conference on ASIC (ASICON), Chongqing, China, 29 October–1 November 2019; pp. 1–4. [CrossRef]
40. Barik, C.K.; Baksi, R.; Shekhar, H.; Kuanr, B.R.; Lata, M. Effect of parameter tuning of differential evolution on PID controller for automatic generation control of a hybrid power system in deregulated environment. In Proceedings of the 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, India, 18–19 March 2016; pp. 1–6. [CrossRef]
41. Chen, P.; Cheng, H.C.; Widodo, A.; Tsai, W.X. A PVT insensitive field programmable gate array time-to-digital converter. In Proceedings of the 2013 IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC), Perugia, Italy, 3 October 2013; pp. 1–4. [CrossRef]