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A Current-Mode Optoelectronic Receiver IC for Short-Range LiDAR Sensors in 180 nm CMOS

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Abstract: This paper presents three different types of on-chip avalanche photodiodes (APDs) realized in a TSMC 180 nm 1P6M RF CMOS process, i.e., a P^+/N-well (NW) APD for its high responsivity and large bandwidth by excluding slow diffusion currents; a P^+/Deep N-well (DNW) APD for its improved near-infrared (NIR) sensitivity; and a P^+/NW/DNW APD for its capability to prevent premature edge breakdown and improve NIR sensitivity. Thereafter, a conventional voltage-mode optoelectronic receiver (V-OER) was realized to confirm the feasibility of the three on-chip APDs. However, the measured results of the V-OER demonstrate a very narrow dynamic range. Therefore, we propose a current-mode optoelectronic receiver (C-OER) realized in the same CMOS process for the applications of short-range LiDAR sensors, where current-conveyor input buffers are exploited to deliver the photocurrents with no significant signal loss to the following inverter cascode transimpedance amplifier, hence resulting in an extended dynamic range. The optically measured results of the C-OER with an 850 nm laser source demonstrate large output pulses. The C-OER chip consumes 47.8 mW from a 1.8 V supply and the core occupies 0.087 mm^2.

Keywords: avalanche photodiode; CMOS; current-mode; LiDAR; mirrored-cascode; optoelectronic; transimpedance amplifier

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1. Introduction

Recently, light detection and ranging (LiDAR) sensors have been popular in various areas such as advanced driver assistance systems for unmanned vehicles, remote sensing detection and navigation systems for robots, and monitoring systems for dementia patients in long-term care facilities [1,2]. Most LiDAR sensors exploit the well-known pulsed time-of-flight mechanism that ensures the successful scan operations ranging up to several hundred meters. Figure 1 shows the block diagram of a typical LiDAR sensor, in which the transmitter includes a laser-diode driver to emit narrow light pulses to targets. The reflected pulses are detected by a receiver that comprises an optical detector, a transimpedance amplifier (TIA), a single-to-differential (S2D) converter, a post-amplifier (PA), and a time-to-digital converter (TDC).

Optical detectors are realized as either a p-i-n photodiode or an avalanche photodiode (APD), depending upon the applications. In this work, APDs are preferred even with the characteristics of noise amplification because targets are usually located within a few-meter distance, hence providing large photocurrents. Nevertheless, the bond-wire interconnection between the APD chip and the receiver circuit inevitably causes severe signal distortions. Additionally, the length of bond wires cannot be precisely controlled, thus degrading the

sensor performance in terms of factors such as gain, bandwidth, and noise. In addition, on-chip electro-static discharge (ESD) protection diodes are mostly necessary to avoid the chip damage from the ESD, which may yet shrink the receiver bandwidth considerably.

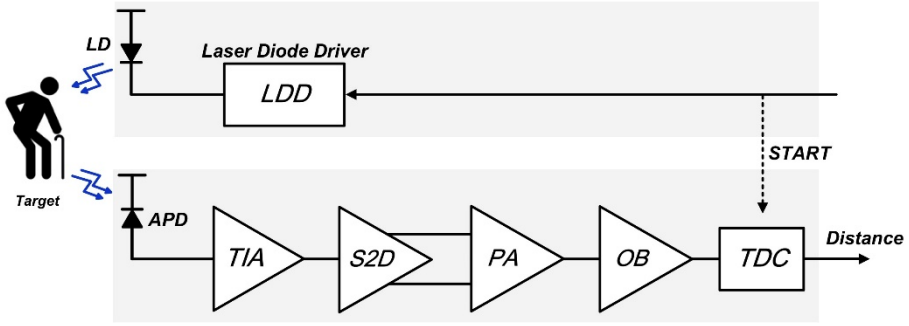


Figure 1. Block diagram of a typical LiDAR sensor.

Several research works have been conducted to develop on-chip optical detectors implemented in bulk CMOS processes [2–8]. Although they inherently suffer from low responsivity and narrow bandwidth [2], the on-chip CMOS APDs can be an effective solution to overcome the aforementioned shortcomings, particularly for the applications of short-range LiDAR sensors [3–5].

Section 2 describes three on-chip CMOS APDs with their measured results. Section 3 presents a conventional voltage-mode optoelectronic receiver with the on-chip CMOS APDs. Section 4 introduces the proposed current-mode optoelectronic receiver, of which measured results are demonstrated in Section 5. Then, a conclusion follows.

2. On-Chip CMOS APDs

This section describes three different types of CMOS APDs in detail, which include a P^+/N-well (NW) APD, a P^+/Deep N-well (DNW) APD, and a P^+/NW/DNW APD. These three structures are suggested to compare their performance in terms of responsivity, bandwidth, and breakdown voltage [4–6].

2.1. P^+/N-Well APD

Figure 2 illustrates the cross-sectional view of the on-chip CMOS P^+/NW APD formed by a P^+/NW junction and an NW/P-substrate junction. Here, the avalanche multiplication is initiated by a hole in the P^+/NW junction [4,5]. The P^+ contacts shown in the mid-region are connected to the front-end TIA, thereby excluding the slow diffusion currents contributed from the P-substrate, and thus providing the characteristics of high responsivity and large bandwidth. Additionally, shallow trench isolation (STI) is located between two active areas as guard rings and penetrates deeper than the P^+/NW junction. Then, the electric field can be distributed uniformly at the edge of the junction. Therefore, the STI can prevent premature edge breakdown, although it may decrease the responsivity of the P^+/NW APD [6]. The P^+ source and drain regions should be covered by the salicide blocking layer to form an optical window. Yet, the P^+ contacts should be open because the salicidation process reduces the contact's resistivity [7]. In addition, the area occupied by the P^+ contacts should be small enough not to degrade the responsivity.

2.2. P^+/Deep N-Well APD

Figure 3 shows the cross-sectional view of the on-chip CMOS APD based on the P^+/DNW junction, where the slow diffusion currents from the P-substrate are eliminated by using a DNW. Hence, the near-infrared (NIR) sensitivity can be greatly improved because the depletion region is formed deeper and wider than other structures. However, it should be noted that the premature edge breakdown might occur, provided that the

depletion region is formed way below STI. Furthermore, the responsivity is considerably lower than in other structures, which is confirmed by the measured results.

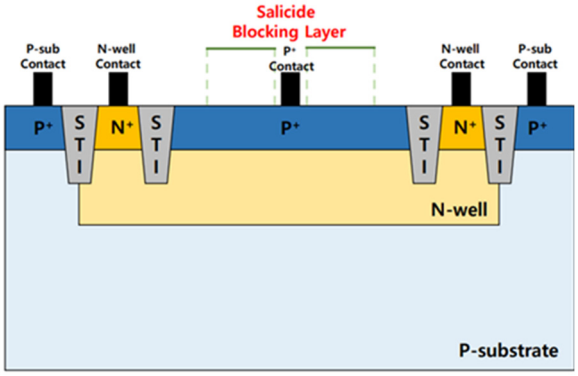


Figure 2. Cross-sectional view of a P^+/NW APD [4,5].

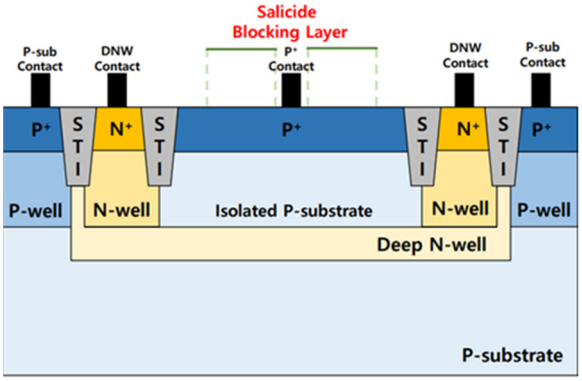


Figure 3. Cross-sectional view of a P^+/DNW APD.

2.3. P^+/N-Well/Deep N-Well APD

Figure 4 illustrates the cross-sectional view of the on-chip CMOS P^+/NW/DNW APD, where the avalanche multiplication is also initiated by a hole at the P^+/NW junction. The premature edge breakdown can be prevented by the STIs. Additionally, the addition of a DNW improves the NIR sensitivity because it decreases the number of holes spreading into the P-substrate. Moreover, the photocurrents generated in the P-substrate can be excluded, owing to the built-in potential barrier between the DNW and the P-substrate.

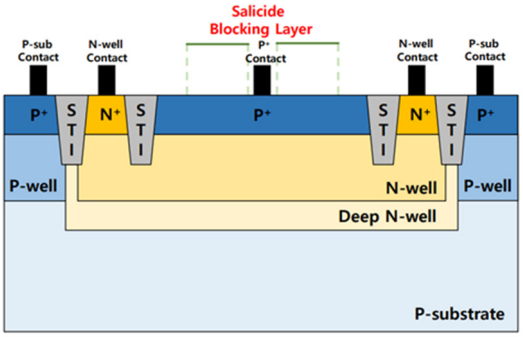


Figure 4. Cross-sectional view of a P^+/NW/DNW APD.

Figure 5 depicts the layout of an on-chip CMOS APD, where the P^+ source and drain regions should be covered by the salicide blocking layer to form an optical window. However, the P^+ contacts in the middle of the optical window should not be blocked because the salicidation process reduces the contact's resistivity [6]. The diagonal length of

the optical window is 40 µm, such that the APD provides a total depletion capacitance (C_{PD}) of 490 fF and a photodetection bandwidth of 1.7 GHz at the reverse bias of 10.25 V. The octagonal shape is preferred to minimize the feasible damage from the edge breakdown. For HSPICE simulation purposes, the equivalent modeling of the on-chip APD comprises an ideal current source with a parasitic capacitance of 490 fF.

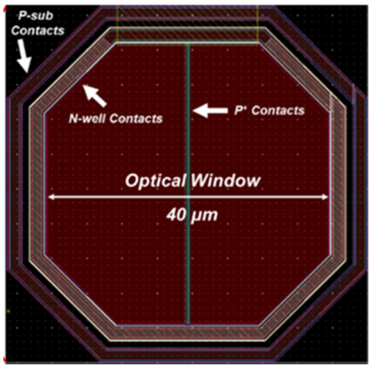


Figure 5. Layout of an on-chip APD.

2.4. Measured Results

These three types of on-chip APDs were implemented by using a TSMC 0.18 µm 1P6M RF CMOS process. Figure 6 shows an example of chip photographs for three on-chip APDs, where each area occupies 375 × 450 µm^2, including I/O pads.

Figures 7 and 8 demonstrate the measured current-voltage (I–V) characteristics of each APD and the measured responsivity versus the reverse bias voltages under the conditions of both dark and optical illuminations. It is clearly seen that both the dark current and the illumination current increase dramatically at the breakdown voltage due to the avalanche multiplication process.

The breakdown voltages are measured to be 10.9 V for P$^+$/NW APD, 15.05 V for P$^+$/DNW APD, and 10.55 V for P$^+$/NW/DNW APD, respectively. Here, the inserted optical power (P_{opt}) was set to −30 dBm. Then, the responsivity (R) of each APD is estimated by,

$$R = \frac{I_{illumination} - I_{dark}}{P_{opt}}, \quad (1)$$

where P_{opt} is the incident optical power, and $I_{illumination}$ and I_{dark} represent the measured currents under the illumination and the dark conditions.

Additionally, it is clearly seen that the measured responsivity is 2.77 A/W at 10.85 V for P$^+$/NW APD, 1.38 A/W at 15 V for P$^+$/DNW APD, and 4.16 A/W at 10.5 V for P$^+$/NW/DNW APD, respectively.

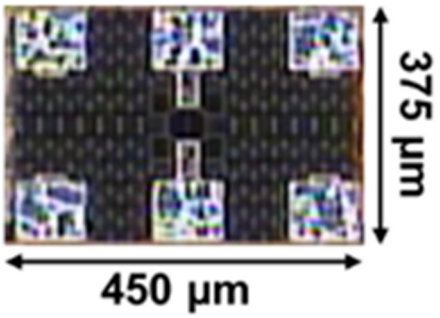


Figure 6. An example of on-chip APDs' photograph.

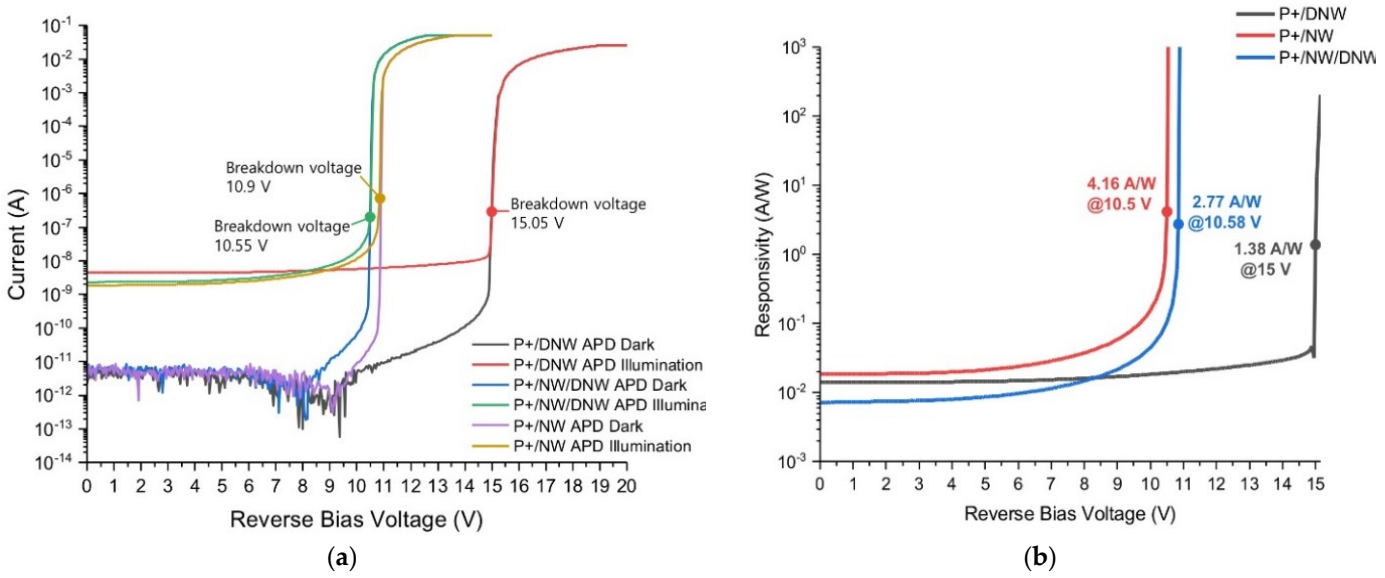


Figure 7. (**a**) Measured I-V curves and (**b**) Measured responsivities of the three on-chip APDs.

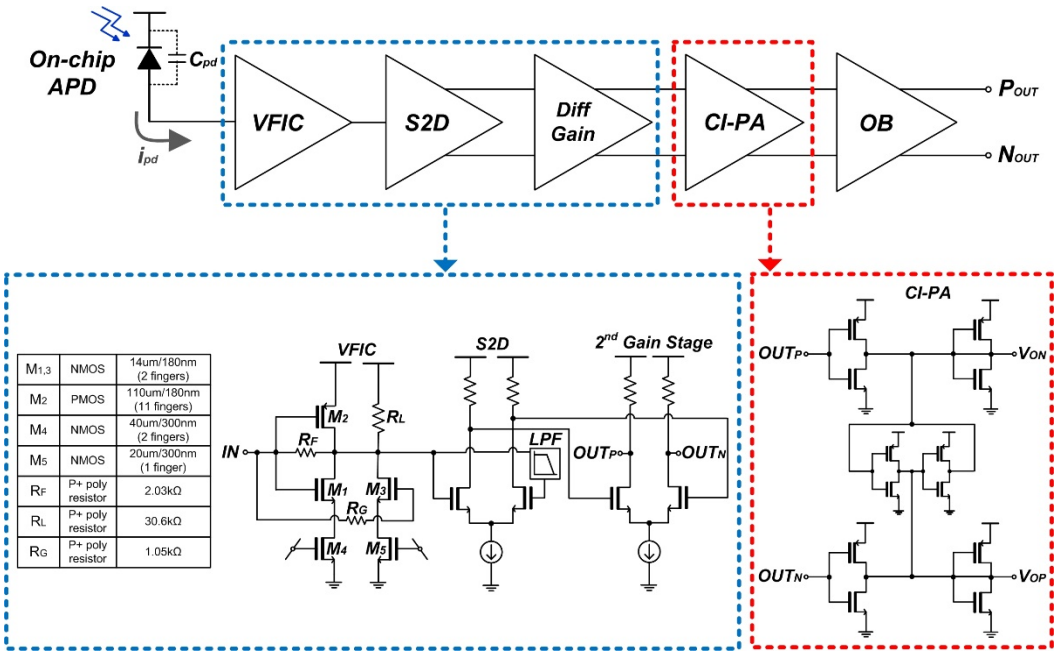


Figure 8. Block diagram of the voltage-mode optoelectronic receiver (V-OER) with an on-chip APD.

3. Voltage-Mode Optoelectronic Receiver (V-OER)

3.1. Experimental Methods

An optoelectronic optical receiver IC with the suggested on-chip APDs was realized in a TSMC 180 nm CMOS process to verify the feasibilities for the applications of short-range LiDAR sensors. As a front-end transimpedance amplifier (TIA), a conventional voltage-mode feedforward input circuit (VFIC) is exploited in this work since it can provide low-noise high-gain performance [5]. Figure 8 shows the block diagram of the voltage-mode optoelectronic receiver (V-OER) which consists of an APD as an optical detector, a VFIC as a TIA to convert the generated photocurrents to electrical voltages, a single-to-differential (S2D) converter for differential signaling, a differential gain stage for gain boosting, and a cross-coupled inverter post-amplifier (CI-PA) for offset cancellation. An output buffer (OB) is inserted not only for 50 Ω impedance matching, but also for the effective isolation of the V-OER circuit from the following time-to-digital converter (TDC) that is typically

employed to estimate the time interval between the transmitted pulses and the received echo pulses [9,10].

In the VFIC, a voltage-mode inverter (INV) input stage with a feedback resistor (R_F) is merged with a feedforward common-source amplifier of which the gate node is connected to the gates of the INV input stage [4,5]. The CI-PA consists of four inverters and two diode-connected output buffers, where the output voltages (V_{ON} and V_{OP}) can be enhanced by merging the input signals (OUT_N and OUT_P) with other small portions of another path. However, circuit designs should be carefully conducted to match $\partial g_{mn}/\partial v_{gs}$ with $\partial g_{mp}/\partial v_{gs}$ because the amplitude mismatches between two outputs might occur in the cases of short-distance detection, where g_{mn} and g_{mp} represent the transconductance of NMOS and PMOS transistors, respectively.

3.2. Measured Results

Firstly, the implemented V-OER IC demonstrated the electrically measured eye-diagrams, where the eyes of the V-OER IC were wide and clean at a data rate up to 500 Mb/s with the input currents of 20 μA_{pp} and 50 μA_{pp}, respectively. The single-ended output amplitude of each eye-diagram was measured with a 50 Ω termination, where amplitudes acquired were similar to those demonstrated in [5].

Secondly, the electrically measured output noise of the V-OER IC revealed that the equivalent noise current spectral density was 4.54 pA/$\sqrt{\text{Hz}}$, which corresponds to the optical sensitivity of −35.5 dBm for the BER of 10^{-12} with the APD responsivity of 2.77 A/W. Here, it is noted that the inherent noise voltage of the utilized oscilloscope (i.e., Agilent DCA 86100D) was measured to be 0.75 mV_{RMS}.

Figure 9 depicts a PC-board module for optical testing, in which on-chip APDs were integrated on the same die of the V-OER IC. The four-channel V-OER array IC occupies the total area of 2.0 × 1.1 mm^2, including I/O pads. For optical testing, an 850 nm laser source driver (Seed LDD, Notice Korea Ltd., Anyang, Republic of Korea) with a laser diode (Qphotonics, Ann Arbor, MI, USA) was utilized to generate light pulses.

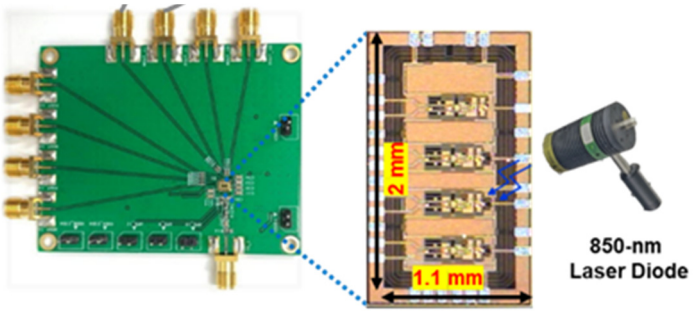
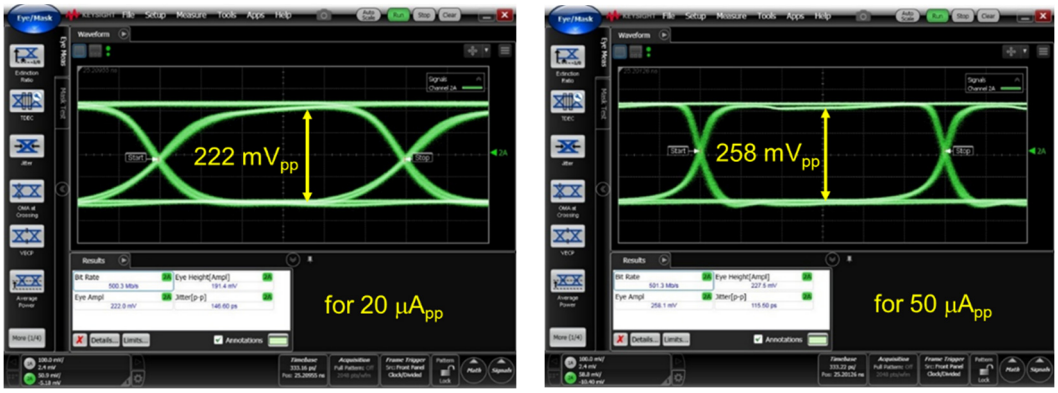


Figure 9. Chip photo of the V-OER IC in a test module with three CMOS APDs.

Figure 10 demonstrates the electrically measured eye-diagrams of the V-OER at 500 Mb/s with different input currents of 20 μA_{pp} and 50 μA_{pp}, in which a singled-ended output was measured with a 50 Ω termination. Hence, each output corresponds to the transimpedance gain of 91.6 dBΩ and 85.2 dBΩ, respectively.

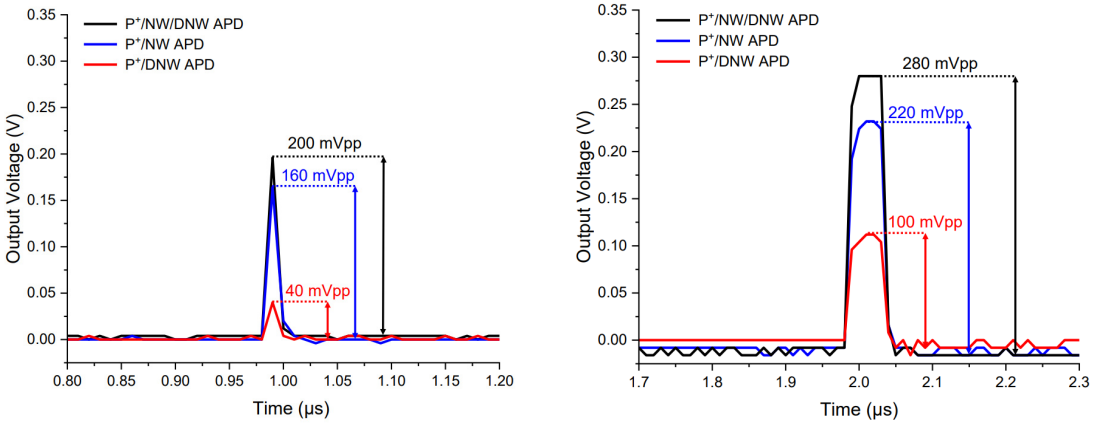
Additionally, the output noise voltage of the V-OER IC was measured with the inherent background noise of the oscilloscope (Agilent DCA 86100D). Thereby, the input-referred average noise current spectral density is estimated to 4.54 pA/$\sqrt{\text{Hz}}$, which corresponds to the optical sensitivity of −29.5 dBm for bit-error-rate (BER) of 10^{-12} to satisfy the maximum signal-to-noise ratio (SNR) of 14.

Figure 11 demonstrates the optically measured pulse responses, where the light pulses were generated by utilizing an 850 nm laser source driver. It is clearly seen that the V-OER IC with the P^+/NW/DNW APD yields the largest output pulses.



(**a**) (**b**)

Figure 10. Electrically measured eye-diagrams of the V-OER for 2^{23}-1 PRBS input currents at 500-Mb/s data rates: (**a**) 20 μA_{pp} and (**b**) 50 μA_{pp}, respectively.



(**a**) (**b**)

Figure 11. Optically measured pulse responses of the V-OER with three different APDs for (**a**) 5 ns and (**b**) 50 ns input pulses, respectively.

Table 1 compares the performance of the realized V-OER IC with the prior parts for the applications of short-range LiDAR sensors. Ref. [4] demonstrated an optoelectronic receiver IC for home-monitoring purposes, which consisted of an on-chip P^+/NW APD, a feedforward TIA, and a limiting amplifier. However, the measured results showed poorly recovered optical pulses, i.e., 8 mV_{pp} amplitude with a 25 ms pulse width. Ref. [11] suggested a differential shunt-feedback (SF) TIA employing an off-chip APD (with 40-A/W responsivity). Even though it achieved very high transimpedance gain and a very large maximum detectable input current, AC coupling capacitors and bias resistors were mandatory for the interconnection between the off-chip APD and the receiver. Additionally, it required a separate TDC IC so that the maximum input dynamic range could be achieved. Ref. [12] presented a frequency-compensated inverter TIA that could demonstrate very-low-noise current spectral density. However, it revealed high power dissipation and mandated a large reverse voltage of 200 V for the off-chip APD to achieve 50 A/W responsivity characteristics. Ref. [13] realized a shunt-feedback (SF) TIA with an off-chip APD, providing a very low-power solution. Furthermore, it could recover a narrow pulse width of 2 ns. Yet, the chip area was quite large.

The V-OER IC exploits an on-chip APD to realize a small chip area and provide a low minimum detectable current and a large signal-to-noise ratio (~10 in this work). However, it is clearly seen that the input dynamic range is very limited—to 26.4 dB (i.e., the max. input current of 50 μA_{pp}).

Table 1. Performance comparison with previously reported voltage-mode CMOS TIAS.

PARAMETERS	[4]	[11]	[12]	[13]	V-OER
CMOS technology (nm)	180	350	180	180	180
APD	On-chip	Off-chip	Off-chip	Off-chip	On-chip
Input configuration	VCF	SF	SF with FC	SF	VCF
Bandwidth (MHz)	790	230	281	450	608
TZ gain (dBΩ)	93.4	100	86	100	95.1
Noise current spectral density (pA/sqrt(Hz))	12	6.32	4.68	2.59	4.54
Min. detectable current (mA_{pp})	6.74 (SNR = 10)	1.0 (SNR = 5)	2.0 (SNR = 25)	2.5 (SNR = 5)	2.38 (SNR = 10)
Single-pulse width	25 ms	3 ns	3 ns	2 ns	5 ns
Optically measured pulse (mV_{pp})	8	200	110	300	200
Power dissipation (mW)	56.5 (w/OB)	180 (w/TDC)	200 (w/PA)	6.6 (w/o OB)	39.3 (w/OB)
Core area (mm^2)	0.09	14	2.20	4.08	0.068

VCF: voltage-mode CMOS feedforward, SF: shunt feedback, FC: frequency compensation, SNR: signal-to-noise ratio.

4. Proposed Current-Mode Optoelectronic Receiver (C-OER)

Voltage-mode TIAs can be preferred for long-range LiDAR sensors because of their low-noise characteristics. In particular, inverter TIAs (INV-TIAs) have been frequently exploited because of their inherent advantages such as easy design, no additional bias circuitry, high gain, low noise, etc. However, they may suffer from considerable degradation of bandwidth and noise performance because the photodiode capacitance (C_{pd}) may vary significantly depending upon the amplitudes of the incoming input currents [10]. Hence, we employ a current-mode TIA in this work as a front-end circuit to facilitate the aforementioned issues of the photodiode capacitance.

Basically, a current-mode TIA functions as a current-buffer, provides a small input resistance, and thus helps to isolate the photodiode capacitance from the determination of the circuit bandwidth. Common-gate architecture is a conventional example of a current-mode TIA, which however suffers from the significant loss of currents because the input resistance (~$1/g_m$) cannot be indefinitely reduced [10]. To the contrary, the symmetric current-conveyor input buffer (CCIB) architecture is another example of a current-mode TIA, which can prevent the loss of input currents effectively since the modified cascode input configuration yields a large output resistance.

Figure 12 illustrates the block diagram of the proposed current-mode optoelectronic receiver (C-OER), which consists of an on-chip APD to generate photocurrents, a parallel arrangement of five current conveyor input buffers (CCIBs) that can separate the parasitic photodiode capacitance from the cascode inverter stage (CIS) effectively, a single-to-different (S2D) converter for differential signaling to improve common-mode rejection ratio characteristics, a second-stage differential amplifier (DIFF) for further gain-boosting and improved output symmetry, a cross-coupled inverter-based post-amplifier (CI-PA) to boost the output swing and reduce the mismatches between differential pulses, and an output buffer (OB) for 50 Ω impedance matching.

Figure 13a depicts the schematic diagram of a single CCIB stage with a modified NMOS cascode circuit (M_1~M_4) incorporated into its PMOS counterpart (M_5~M_8). Consequently, half (i.e., $i_{PD,n}$) of the input current flows through the NMOS cascode circuit (M_1 and M_2), while the other half (i.e., $i_{PD,p}$) flows into the PMOS cascode circuit (M_5 and M_6). Therefore, the total input photocurrent (i_{PD}) from the photodiode can be almost symmetrically split into two paths. Furthermore, the two currents ($i_{PD,n}$ and $i_{PD,p}$) are mirrored to the circuit, comprising M_3, M_4, M_7, and M_8. The mirrored currents can be summed and flow out of

the feedback resistor (R_F) in the following CIS. Consequently, a positive transimpedance gain can be provided, which is the opposite to the case of the previous V-OER.

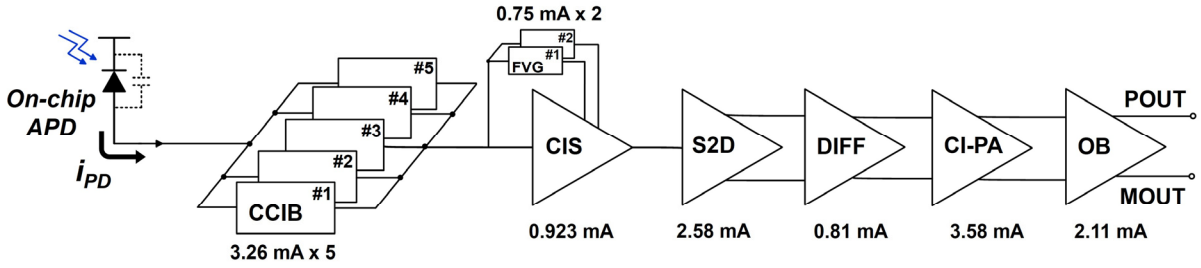


Figure 12. Block diagram of the proposed C-OER.

According to small signal analysis, the input resistance of the CCIBs varies with respect to the number of the switched-on blocks. When only CCIB#3 is turned on, the input resistance ($R_{in,3}$) is given by,

$$R_{in,3} = \frac{1}{g_{m2}} || \frac{1}{g_{m5}} \cong \frac{1}{2g_m}, \tag{2}$$

where g_{m2} and g_{m5} represent the transconductance of M_2 and M_5, respectively. Provided that $g_{m2} = g_{m5} = g_m$, the input resistance becomes equal to $1/2g_m$.

When other two CCIB blocks (#2 and #4) are added to CCIB#3 with the switch turned on, the new input resistance ($R_{in,2}$) is given by,

$$R_{in,2} = R_{in,3} || R_{in,parallel} \cong \frac{1}{2g_m} || \left(\frac{1}{2g_m} || \frac{1}{2g_m} \right) = \frac{1}{6g_m} \tag{3}$$

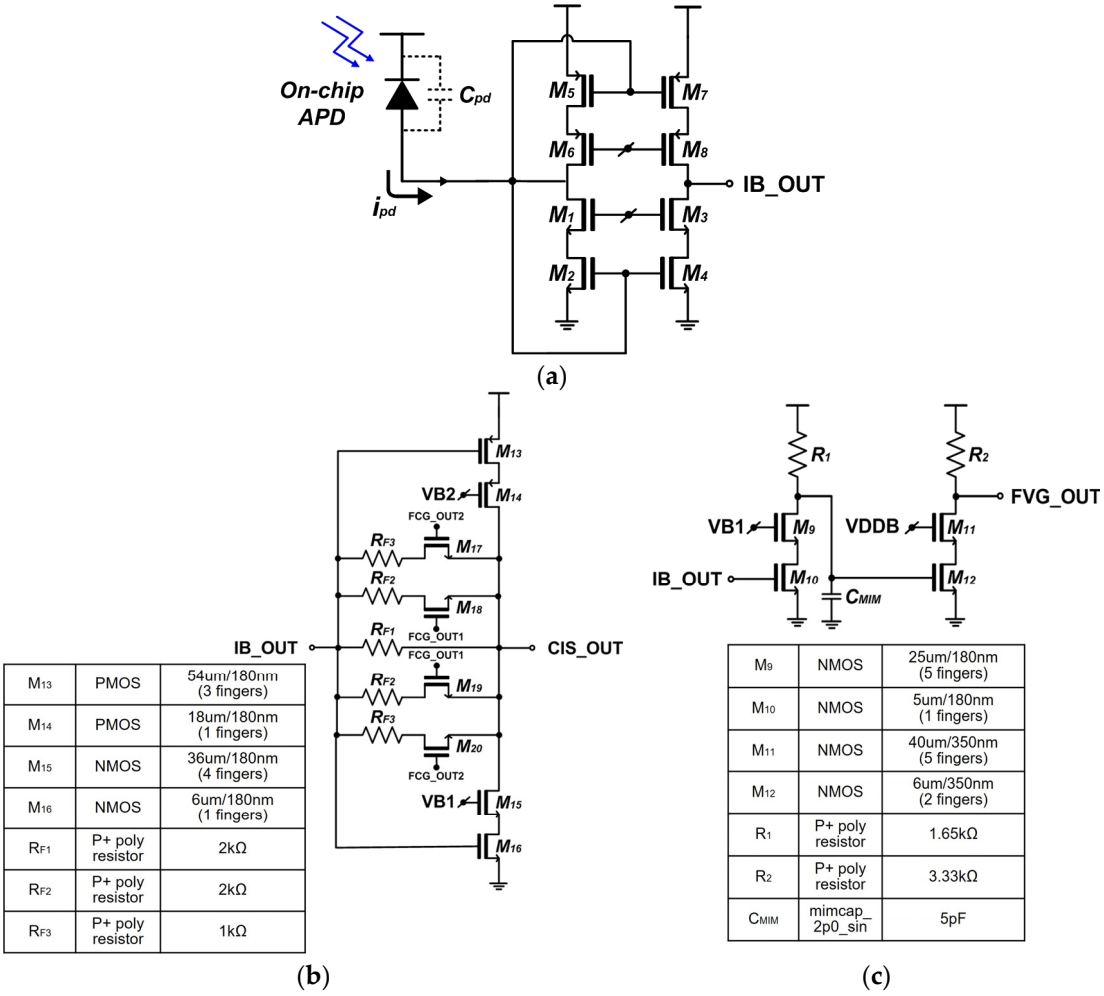
All the CCIB blocks are turned on simultaneously, the input resistance (R_{in}) is given by,

$$R_{in} = R_{in,2} || R_{in,parallel} \cong \frac{1}{6g_m} || \left(\frac{1}{2g_m} || \frac{1}{2g_m} \right) = \frac{1}{10g_m} \tag{4}$$

Therefore, it is clearly seen that the CCIB stage provides a very low input resistance of $1/10g_m$, hence helping to isolate the photodiode capacitance from the bandwidth determination more effectively than the V-OER. Additionally, it yields a large output resistance of $\sim(1/2){g_{mro}}^2$, thereby preventing the loss of the input current signals more efficiently.

Figure 13b shows the schematic diagram of the cascode inverter stage (CIS) with a feedback resistor array (FRA) that comprises five resistors (R_{F1}~R_{F3}) and four switches (M_{17}~M_{20}). The FRA conducts the function of automatic gain control (AGC). Among the five resistors in the FRA, R_{F1} should always be connected, while the other four resistors (R_{F2} and R_{F3}) are turned on via thick-gate NMOS switches (M_{17}~M_{20}). These thick-gate NMOS switches are designed to operate in pairs and are controlled by a feedforward voltage generator (FVG) that consists of two-stage cascaded amplifiers and an on-chip MIM capacitor (C_{MIM}) for low-pass filtering, as shown in Figure 13c. Thereby, the transimpedance gain can be tuned automatically within the duration of a narrow single pulse at the different input voltages of VB1 and VB2, respectively.

Based on the output voltage (IB_OUT) of the CCIB stage, the FVG generates 3.3 V DC voltages (FVG_OUT) to turn the NMOS switches on in the FRA. When the FVG turns all the NMOS switches on, the CIS produces the lowest transimpedance gain. When the FVG is turned off, only the feedback resistor R_{F1} is activated and thus the CIS amplifies the input currents with the highest transimpedance gain.



M_{13}	PMOS	54um/180nm (3 fingers)
M_{14}	PMOS	18um/180nm (1 fingers)
M_{15}	NMOS	36um/180nm (4 fingers)
M_{16}	NMOS	6um/180nm (1 fingers)
R_{F1}	P+ poly resistor	2kΩ
R_{F2}	P+ poly resistor	2kΩ
R_{F3}	P+ poly resistor	1kΩ

M_9	NMOS	25um/180nm (5 fingers)
M_{10}	NMOS	5um/180nm (1 fingers)
M_{11}	NMOS	40um/350nm (5 fingers)
M_{12}	NMOS	6um/350nm (2 fingers)
R_1	P+ poly resistor	1.65kΩ
R_2	P+ poly resistor	3.33kΩ
C_{MIM}	mimcap_ 2p0_sin	5pF

Figure 13. Schematic diagrams and the specific parameters of (**a**) CCIB, (**b**) CIS, and (**c**) FVG blocks.

Small signal analysis indicates that the transimpedance gain of the CIS is given by,

$$Z_{T,inv} \approx \left(\frac{A_{inv}}{1+A_{inv}}\right) R_{F,EQ} \cong R_{F,EQ}, \tag{5}$$

where A_{inv} is the voltage gain of the CIS, and $R_{F,EQ}$ represents the equivalent feedback resistance of the FRA [10].

The input resistance of the CIS is given by,

$$R_{in,ITS} = \frac{R_F}{A_{inv}+1} \cong \frac{R_{F,tot}}{{g_m}^2 {r_o}^2}, \tag{6}$$

where the non-dominant pole occurs at the input node of the CIS. The output pole also becomes non-dominant because of its small capacitance [10]. Therefore, the bandwidth ($f_{\text{-3dB}}$) is nearly determined at the input node of the CCIB stage, i.e.,

$$f_{-3\text{dB}} \cong \frac{1}{10\pi R_{in}(C_{pd} + 2C_{gs,n} + 2C_{gs,p})}, \tag{7}$$

where R_{in} is the input resistance of the CCIB stage as defined in (3), C_{pd} is the photodiode capacitance, $C_{gs,n}$ is the gate-source capacitance of NMOS transistors (M_2 and M_4), and $C_{gs,p}$ is the gate-source capacitance of PMOS transistors (M_5 and M_7), respectively [10].

The input-referred equivalent noise current spectral density of the five CCIB blocks is roughly given by,

$$\overline{i^2_{eq}} \cong 5\left[\overline{i^2_{d2}} + \overline{i^2_{d5}} + \frac{(\overline{i^2_{d4}} + \overline{i^2_{d7}})}{{g_{m4}}^2}\cdot\omega^2{C_{tot}}^2\right] + \frac{\omega^2{C_{tot}}^2}{5{g_{m4}}^2}\cdot\left[\overline{i^2_{R_{F,EQ}}} + (\frac{\overline{i^2_{d16}} + \overline{i^2_{d13}}}{{g_{m16}}^2})\cdot(\frac{1}{{R_{F,EQ}}^2} + \omega^2{C_1}^2)\right], \quad (8)$$

where $\overline{i^2_{di\,(i=2,4,5,7)}}$ represents the thermal noise current spectral density of $M_{i\,(i=2,4,5,7)}$, $\overline{i^2_{R_{F,tot}}}$ is the thermal noise current of $R_{F,EQ}$, $C_1\left(= C_{gs13} + C_{gs16}\right)$ is the input capacitance of the CIS, and $C_{tot}\left(= 5C_{in} + C_{pd}\right)$ represents the total capacitance at the input node of the CCIB that comprises the input capacitance $\left(C_{in} = C_{gs2} + C_{gs4} + C_{gs5} + C_{gs7}\right)$ of the CCIB and the photodiode capacitance (C_{pd}).

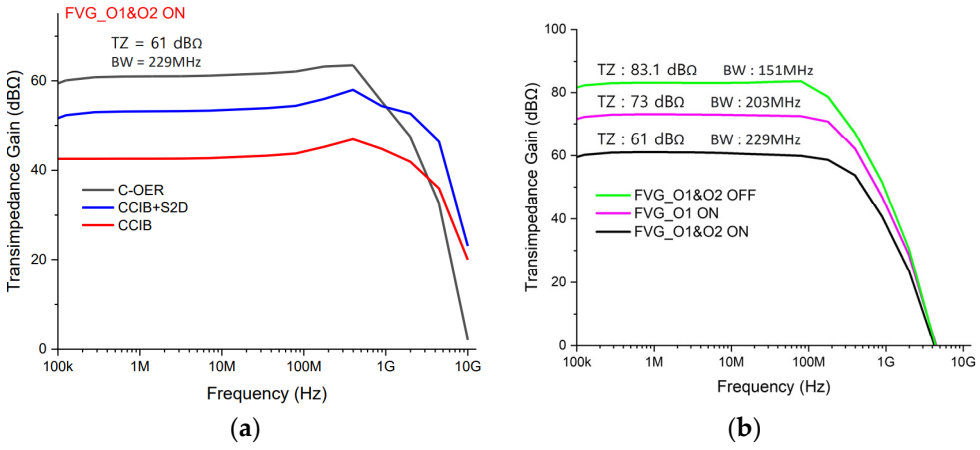
Here, it is assumed that $g_{m2} = g_{m5}$, $g_{m4} = g_{m7}$, $g_{m13} = g_{m16}$, $\overline{i^2_{d2}} = \overline{i^2_{d5}}$, $\overline{i^2_{d4}} = \overline{i^2_{d7}}$, and $\overline{i^2_{d13}} = \overline{i^2_{d16}}$. Therefore, Equation (7) is simply approximated by,

$$\begin{aligned}\overline{i^2_{eq}} &\cong 10\overline{i^2_{d2}} + \left(\frac{\omega C_{tot}}{g_{m4}}\right)^2\left[10\overline{i^2_{d4}} + \frac{\overline{i^2_{R_{F,EQ}}}}{5} + \frac{2\overline{i^2_{d16}}}{5}\cdot\left(\frac{\omega C_1}{g_{m16}}\right)^2\right] \\ &= 40KT\Gamma g_{m2} + 8KT\Gamma\left(\frac{\omega C_{tot}}{g_{m4}}\right)^2\left[5g_{m4} + \frac{1}{10\Gamma R_{F,EQ}} + \frac{g_{m16}}{5}\left(\frac{2\omega}{\omega_T}\right)^2\right] \cong 40KT\Gamma\left[g_{m2} + \frac{\omega^2{C_{tot}}^2}{g_{m4}}\right]\end{aligned} \quad (9)$$

where K is the Boltzmann constant, T is the absolute temperature, Γ is the noise factor of MOSFET. Under the assumption that $g_{m2} = g_{m4}$, the input capacitance (C_{in}) should be roughly equal to $(\frac{C_{pd}}{5})$ to minimize the noise current spectral density.

Post-layout simulations were performed for the proposed C-OER by using the model parameters of a TSMC 180 nm CMOS technology. Figure 14a shows the frequency response with the FVG modules turned on, achieving the transimpedance gain of 61 dBΩ and the bandwidth of 229 MHz. Figure 14b illustrates that the C-OER obtains the transimpedance gain of 73 dBΩ and a bandwidth of 203 MHz when only the FVG_O1 module is turned on. The largest transimpedance gain of 83.1 dBΩ and a bandwidth of 151 MHz are obtained when the FVGs are turned off.

Figure 15 depicts the simulated pulse responses of the C-OER at different input current levels of 5 μA_{pp}~1.0 mA_{pp}, which corresponds to the input dynamic range of 46 dB. Moreover, it is clearly seen that the output voltages can be saturated with the input currents of 300 μA_{pp} and above.



(**a**) (**b**)

Figure 14. Simulated gain variations (**a**) with both FVGs turned on, (**b**) with FVG turn on and off, respectively.

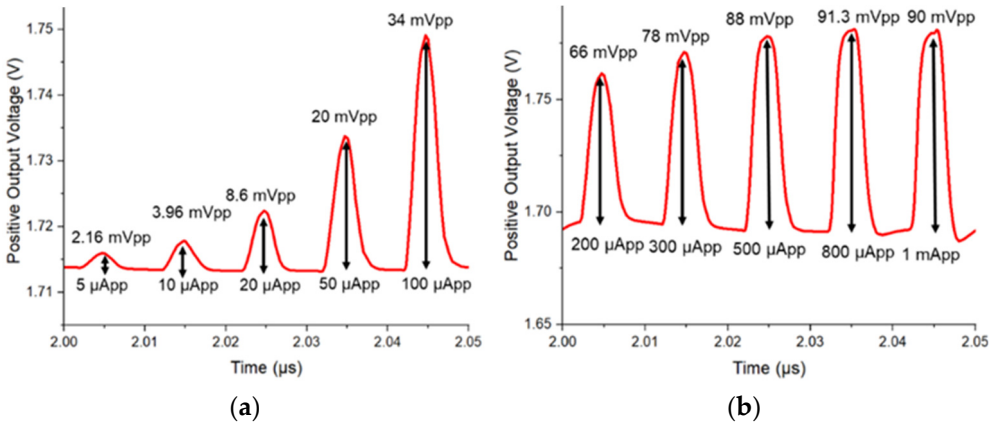


Figure 15. Simulated pulse responses of the proposed C-OER IC: (**a**) with small (5~100 μA_{pp}), (**b**) with large (0.2~1 mA_{pp}) input currents, respectively.

5. Measured Results of the Proposed C-OER

5.1. Experimental Methods

Test chips of the proposed C-OER IC were implemented in the same CMOS process. Figure 16 depicts the chip photograph of the C-OER IC and a PC-board module for optical testing, where an 850 nm laser source driver (Seed LDD, Notice Korea Ltd., Anyang-si, Republic of Korea) with a laser diode (Qphotonics, Ann Arbor, MI, USA) was utilized to generate light pulses. The chip core occupies the area of 0.087 mm^2, and the DC measurements reveal the power dissipation of 47.8 mW from a 1.8 V supply.

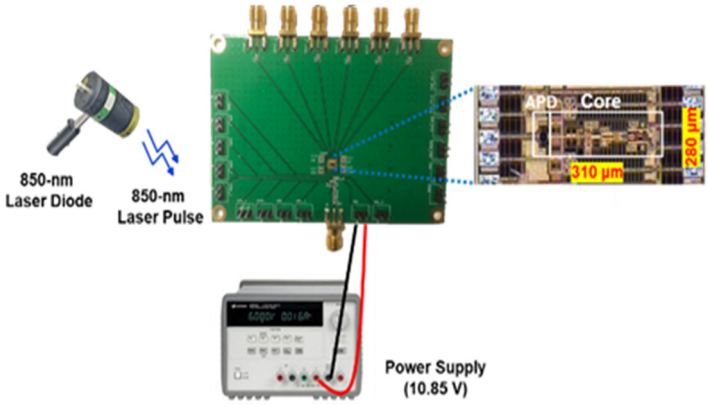


Figure 16. Chip photo of the C-OER IC and its test module.

5.2. Measured Results

Figure 17 demonstrates the optically measured pulse responses of the proposed C-OER IC for two different on-chip APDs with two different input pulses, where it is clearly seen that the C-OER integrated with the P^+/NW APD exhibits relatively much larger output voltages than the case with the P^+/DNW APD. Here, it is noted that the P^+/NW/DNW APD was not integrated in this C-OER IC even with its highest responsivity because this might saturate the output voltages even at a much smaller input current than 1 mA_{pp}, i.e., the limited input dynamic range.

Therefore, the P^+/NW APD would be the most appropriate detector, not only to extend the input dynamic range further, but also to recover the weak input currents of 5 μA_{pp} well enough.

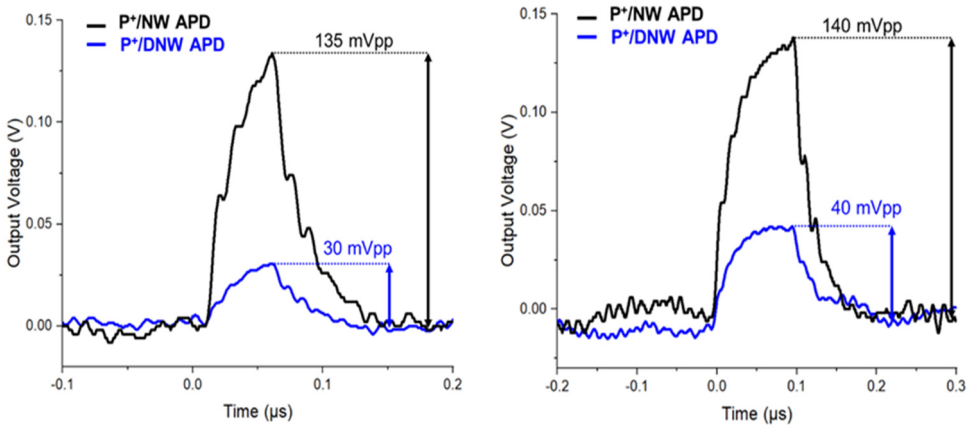


Figure 17. Optically measured pulse responses of the proposed C-OER IC with two different APDs for (**a**) 50 ns and (**b**) 100 ns input pulses.

Table 2 compares the performance of the C-OER IC with the previously reported CMOS receivers for short-range LiDAR sensors. Ref. [14] suggested a current-mirror (CM) input configuration with a shunt-feedback (SF) topology, which could successfully attain high transimpedance gain and wide dynamic range. However, the AGC function was carried out by an external field programmable gate array (FPGA). Ref. [15] merged a voltage-mode feedforward input configuration with a negative feedback AGC circuit comprising four switches so as to extend the dynamic range. However, it exploited off-chip APDs and the AGC circuit could not recover the input pulses within a single-pulse width. Ref. [16] proposed a capacitive feedback (CF) topology to obtain nanoampere low-noise currents. However, the manual gain control was required for low-gain and high-gain modes, and the maximum current detectable in the loop was limited to 250 μA_{pp}. Ref. [17] achieved a wide bandwidth with a current-amplifier-based feedback configuration (CAF) by a pole-zero cancellation technique. Nevertheless, the AGC function was conducted by using an external control. Yet, the detectable current range was limited from 23 μA_{pp} to 83 μA_{pp}.

Table 2. Performance Comparison with Previously Reported CMOS Receivers for LiDAR Sensors.

PARAMETERS	[14]	[15]	[16]	[17]	V-OER	C-OER
CMOS technology (nm)	180	180	350	180	180	180
Supply (V)	3.3	1.8	3.3	1.8/3.3	1.8	1.8/3.3
APD	On-chip	Off-chip	On-chip	Off-chip	On-chip	On-chip
Input configuration	CM + SF	VCF	CF	CAF	VCF	CCIB
Output signaling	single-ended	differential	single-ended	differential	differential	differential
Bandwidth (MHz)	153	720	160	1000	608	151~229
TZ gain (dBΩ)	106	76.3	78~110	56.8~69.3	95.1	61~83.1
Gain control	External	Auto	External	External	No	Auto
Max. detectable current (mA_{pp})	5.0	1.1	0.022	0.083	0.05	1.0
Min. detectable current (mA_{pp})	0.5 (SNR = 5)	1.14 (SNR = 12)	0.053 (SNR = 3.3)	23 (SNR = 14)	2.38 (SNR = 10)	5.0 (SNR = 14)
Power dissipation (mW)	16.5(w/o OB)	29.8	79	6.6(w/o OB)	39.3(w/OB)	47.8
Core area (mm^2)	1.2 × 1.13	5.0 × 1.1	1.0 × 1.2	0.1 × 0.075	0.068	0.28 × 0.31

CM: current-mirror, CF: capacitive feedback.

In this proposed C-OER IC, we have realized the variable AGC mechanism within a narrow single-pulse width by employing FRA feedforward gain control. Consequently, the input dynamic range is extended much further than the V-OER, i.e., the maximum and minimum detectable currents of 1 mA_{pp}, and 5 μA_{pp}, respectively.

6. Conclusions

We have demonstrated the realization of a conventional voltage-mode optoelectronic receiver (V-OER) with three different on-chip APDs by utilizing a TSMC 180 nm RF CMOS process in order to confirm the feasibility of the CMOS on-chip APDs. However, the V-OER IC showed the inherent characteristics of the limited dynamic range. Then, we have presented the C-OER IC, in which a current-conveyor input buffer was employed to deliver the input photocurrents with no loss and to acquire a positive transimpedance gain with automatic gain control within a narrow single-pulse width. Implemented in the same TSMC 180 nm CMOS process, the optically measured results demonstrate the vividly large output pulses and conclusively confirm that the proposed C-OER provides a highly efficient solution for short-range LiDAR sensors.

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