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Advancements in CMOS-Compatible Silicon Nitride Optical Modulators via Thin-Film Crystalline or Amorphous Silicon p–n Junctions

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Abstract: This paper proposes two types of electro-refractive optical modulator structures as a fully CMOS-compatible alternative solution. These modulators leverage the properties of amorphous (top) and crystalline (bottom) silicon films surrounding silicon nitride waveguides operating in the C-band communications range at a wavelength of 1550 nm. Various structures have been demonstrated and explored to compete with or surpass the current state-of-the-art performance of thermal tuners, the most widely used tuning mechanism in silicon nitride integrated photonics. Designs utilizing vertical and lateral p–n junctions with amorphous or crystalline films have been simulated and proposed. For the lateral p–n junctions, modulator lengths to achieve a π phase shift smaller than 287 µm have been demonstrated for the TE mode and that smaller than 1937 µm for the TM mode, reaching 168 µm in the case of a lateral p–n junction that is completely a p-doped region over or under the waveguide for TE, and 1107 µm for TM. Power consumption is higher for the TM modes than for the TE, being in the order of 100 mW for the former and lower than 23 mW for the latter. The modulators exhibit higher losses for amorphous material compared to crystalline, with losses smaller than 10.21 dB and 3.2 dB, respectively. The vertical p–n junctions present a larger footprint than the lateral ones, 5.03 mm for TE and 38.75 mm for TM, with losses lower than 3.16 dB and 3.95 dB, respectively, for the crystalline silicon. Also, their power consumption is on the order of 21 mW for TE and 164 mW for TM.

Keywords: silicon photonics; silicon nitride; optical modulators; CMOS technology; integrated photonics; p–n junction; crystalline silicon; amorphous silicon

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1. Introduction

In the quest for high-speed, energy-efficient optical communication systems, silicon nitride (SiN) photonics modulators have emerged as an alternative technology, offering high performance and versatility [1–5]. Combining the passive SiN components with active functional materials enables the precise manipulation of optical signals (phase and amplitude) with remarkable speed, bandwidth, and integration density [6,7]. As the demand for ever-increasing data rates and bandwidths continues to escalate [8–10], SiN photonics modulators present a different approach compared with other active materials platforms such as silicon-on-insulator (SOI) [11,12] or indium phosphide (InP) [13,14]. SiN, with its wide transparency window ranging from visible to near-infrared (NIR) [15,16], low optical losses [17,18], refractive index tuning [19,20], multilayer stacking [21], low temperature sensitivity [22], non-two-photon absorption (TPA) at telecom wavelengths [23,24], and high tolerance to fabrication errors [25] stands out as a distinct platform for realizing modulators capable of meeting several requirements of modern optical communication systems [26]. Moreover, the compatibility of SiN with complementary metal-oxide-semiconductor (CMOS) processes and wafer-scale fabrication techniques enables the cost-effective production of large-scale photonic integrated circuits (PICs), paving

the way for highly integrated and scalable optical communication platforms, allowing multilayer stacking (3D integration) fabrication processes, increasing the density of components [20,21].

State-of-the-art SOI modulators rely on phase modulation through free carrier plasma dispersion in p–n [27] or p–i–n [28] structures [29,30]. SiN is an insulator material and does not have free carriers that can be modulated by an electric field; therefore, the plasma dispersion effect cannot occur. The inherent nature of deposited SiN material prevents solutions using epitaxial integration, and its centrosymmetric property impedes the exploitation of the Pockels effect for modulation in the waveguide (WG) core itself [31,32].

A perspective of material science, device physics, and system engineering is required for designing and fabricating modulators in SiN WG structures. Different types of these devices have been proposed and demonstrated through the precise engineering of WG geometries, taking advantage of the electro-optic effect of active materials such as lead zirconate titanate (PZT) thin films [31], liquid crystals [33], electro-optic polymers [34], hybrid integration with materials such as III–V semiconductors [35,36], and 2D materials [37–39], including graphene capacitors [40–42]. Other approaches are stress-optic modulation [43], piezoelectric effects [44] or all-optical non-volatile phase-change [45–48]. Making use of these technologies, researchers have achieved remarkable breakthroughs in integrated optical modulation performance, including high-speed modulation, low power consumption, and broad operation bandwidth.

Despite impressive advancements, modulators for SiN WG structures face challenges such as fabrication-induced losses, nonlinear optical effects, power consumption, thermal tuning issues (liquid crystals, electro-optic polymers, PZTs, and piezoelectrics), complex fabrication or integration (III/V materials, 2D materials, PZT, and liquid crystals), limited speed (stress-optic, piezoelectric, and liquid crystals), scalability (2D materials), and degradation (PCMs, PZT, and polymers). These challenges hinder further performance enhancements and integration scalability (wafer-scale integration). Additionally, integrating these devices with other photonic and electronic components requires innovative solutions to address compatibility issues (monolithic CMOS) and optimize system-level performance.

In this work, an electro-optical modulator is proposed to address some of these challenges. This modulator leverages the properties of crystalline silicon (c-Si) and amorphous silicon (a-Si), following two different approaches: c-Si positioned at the bottom of the SiN WG and a-Si on top of the SiN WG, both operating at a wavelength of 1550 nm. Various designs utilizing lateral and vertical p–n junctions are explored. Electrical and optical simulations demonstrate the potential performance and phase-shifting capabilities of these modulators. The proposed devices can be fabricated on the existing SiN photonic platform using CMOS-compatible processes, and a comprehensive comparison of both technologies, using c-Si and a-Si, is presented.

2. Device Description

2.1. Silicon Nitride Platform

Although the proposed devices have only been simulated, an already mature technology could serve as the basis for their fabrication. The SiN photonics platform developed at IMB-CNM [49] starts on 100/150 mm p-type (100) silicon (Si) wafers and is followed by CMOS-compatible fabrication processes. The WGs, acting as passive components, would be built on a 300 nm thick stoichiometric SiN film deposited by Low Pressure Chemical Vapor Deposition (LPCVD) onto 2.5 µm thermally grown silicon dioxide (SiO_2). Using photolithography and etching steps, the different components would be patterned in the SiN. Figure 1a,c show a transversal cut of the SiN WG, designed to operate in single-mode condition for the 1550 nm wavelength band [19].

The dielectric nature of SiN inhibits the direct modulation of its refractive index. Therefore, external indirect methods are necessary to achieve a change in this property. To address this limitation and ensure CMOS compatibility with the existing SiN photonic platform, two different approaches are proposed: a c-Si thin film positioned underneath

the SiN WG, and an a-Si thin film placed on top of the SiN structure. These configurations aim to create an active device capable of altering the phase or intensity of the propagated wave. The concepts are illustrated in Figure 1b,d for each approach.

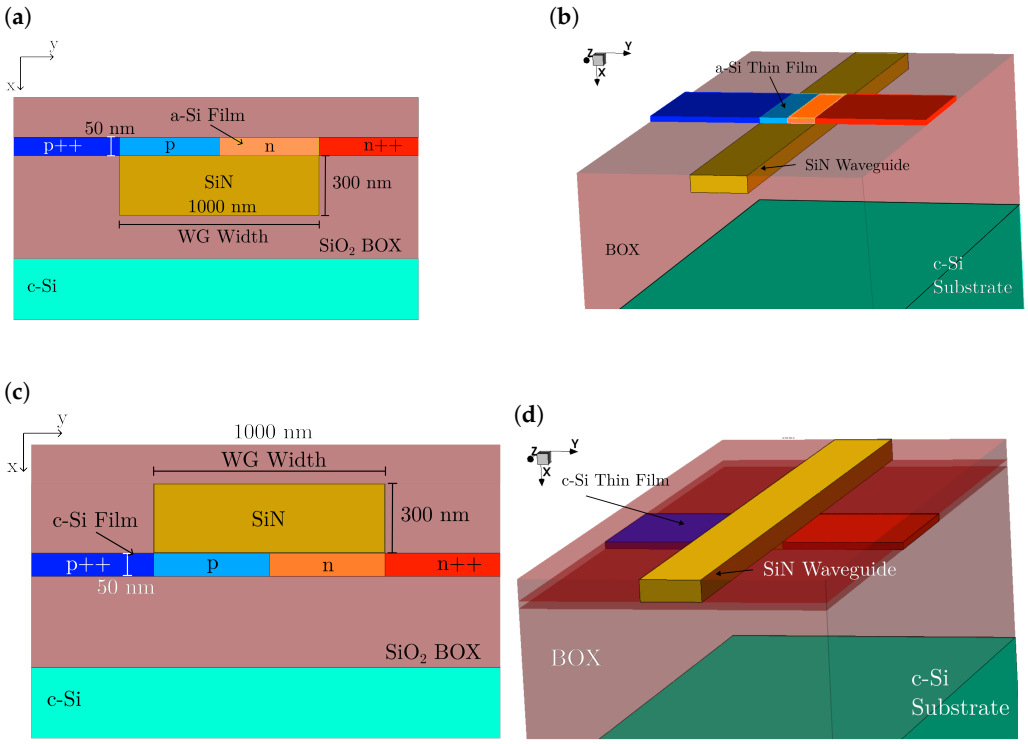

Figure 1. Schematic of the transverse section (not to scale) and 3D view of the conceptual modulators based on a SiN waveguide with (**a**,**b**) a-Si on top of it and (**c**,**d**) c-Si underneath.

The fabrication of SOI modulators using silicon as the core material is less complex than that of the proposed device and can operate in reverse bias, resulting in low power consumption (pW) with footprints around 2 mm. However, our design allows for the exploitation of all the advantageous properties of SiN as a guiding material, such as low optical losses, multilayer stacking, absence of TPA at 1550 nm, and a lower thermal coefficient than silicon. Another approach involves 3D integration, where Si and SiN coexist, enabling light to transition between waveguides and leveraging the benefits of each platform [50]. In this scenario, the fabrication complexity is similar to our proposed device, but in our design, light does not need to travel between waveguides, which requires long coupling lengths, making the total footprint higher, and also implies coupling losses.

The structure depicted in Figure 1 was obtained using Synopsys-Sentaurus TCAD [51], obeying the design rules and materials previously described. The main proposal for active tuning of the optical signal is to accumulate or deplete charge carriers in the Si film in order to modify the refractive index, taking advantage of the carrier plasma dispersion effect [52,53]. At the same time, the effective refractive index (n_{eff}) of the Si/SiN WG system is altered, which means that the mode of the propagated wave sees different n_{eff} as a function of the charge carrier excess due to the applied bias voltage. By building an active Si-based device using CMOS techniques, an electro-refractive based optical modulator will be developed. This modulator will leverage the properties of Si to achieve the desired modulation of the light wave. In the next section, the principles of carrier plasma dispersion in silicon p–n junctions will be reviewed, explored, and studied.

2.2. Carrier Plasma Dispersion in Crystalline and Amorphous Silicon

The refractive index change in silicon due to the injection or depletion of free carriers at a wavelength (λ) equal to 1550 nm can be derived to a first-order approximation from

the classical Drude model, applicable also for a-Si semiconductor [52,54,55]. The refractive index and the absorption coefficient change (Δn and $\Delta\alpha$), caused by accumulated electrons and holes, are given by:

$$\Delta n = -\left(\frac{q^2\lambda^2}{8\pi^2c^2\varepsilon_0 n}\right)\left(\frac{\Delta N}{m^*_{ce}} + \frac{\Delta P}{m^*_{ch}}\right) \quad (1)$$

$$\Delta\alpha = \left(\frac{q^3\lambda^2}{4\pi^2c^3\varepsilon_0 n}\right)\left(\frac{\Delta N}{{m^*_{ce}}^2\mu_e} + \frac{\Delta P}{{m^*_{ch}}^2\mu_h}\right) \quad (2)$$

where q is the electron charge, λ is the wavelength, ε_0 is the permittivity of free space, n is the refractive index of the material, m^*_{ce} and m^*_{ch} are the effective masses for conductivity of electrons and holes respectively, μ_e and μ_h are the mobility of the carriers, and ΔN and ΔP are the concentrations of free electrons and holes in the semiconductor. The applicability of the Drude model to an amorphous material has been shown to give good agreement with experimental results [54,55]. According to Equation (2), higher absorption is to be expected in the case of a-Si. This is because the electron and hole mobilities are smaller in magnitude than in c-Si. For $\lambda = 1550$ nm, the empirical equations to compute Δn and $\Delta\alpha$, obtained from experimental absorption spectra through Kramers–Kronig analysis, are [29,52,54,56,57]:

$$\Delta n = -5.4 \times 10^{-22}\Delta N^{1.011} - 1.53 \times 10^{-18}\Delta P^{0.838} \quad (3)$$

$$\Delta\alpha = 8.88 \times 10^{-21}\Delta N^{1.167} + 5.84 \times 10^{-20}\Delta P^{1.109} \quad (4)$$

where electron and holes carrier densities (ΔN and ΔP) are in units of cm^{-3}, and $\Delta\alpha$ is in cm^{-1} units. Figure 2 shows the curve of Δn and $\Delta\alpha$ variation as a function of the free carrier concentration for c-Si and a-Si. The blue lines represent the case of free holes, while the red solid lines represent the case of free electrons. Dashed lines represent the case for a-Si, while c-Si curves correspond to the fit of the experimental data of Equations (3) and (4). $\Delta\alpha$ for a-Si is obtained using the Drude model presented in Equation (2) using $m^*_{ce} = 0.2m_0$, $m^*_{ch} = 0.5m_0$, $\mu_e = 25\,\mathrm{cm}^2/(\mathrm{V\,s})$ and $\mu_h = 6\,\mathrm{cm}^2/(\mathrm{V\,s})$ where m_0 is the electron mass [58,59].

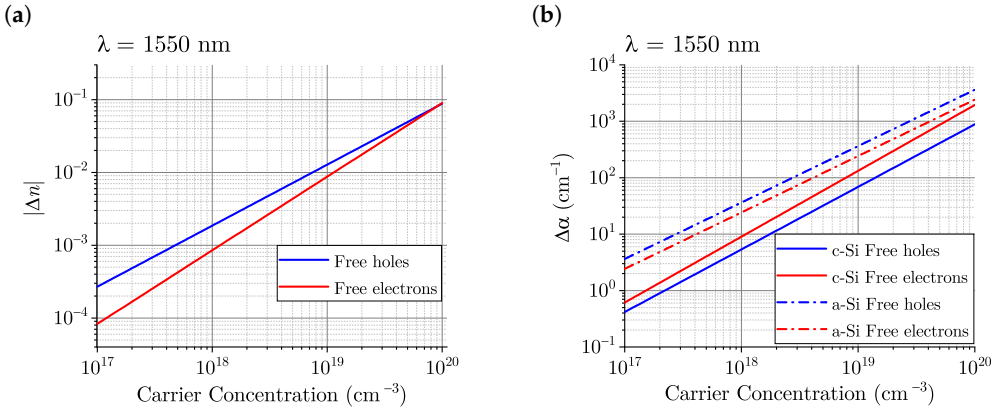

Figure 2. (**a**) Δn for silicon (amorphous and crystalline) and (**b**) the $\Delta\alpha$ for a-Si and c-Si. The blue lines represent the case of free holes, while the red lines represent the case of free electrons. Dashed lines correspond to the theoretical model of a-Si, while the c-Si curves correspond to the fit of the experimental data to Equations (3) and (4).

The main characteristic is the increase in the magnitude of Δn with the carrier concentration, along with the growth in the absorption coefficient $\Delta\alpha$ as the carrier concentration rises. This results in a trade-off between achieving a high refractive index contrast and managing the insertion losses (IL) of the material. Free holes produce more variation than free electrons in the phase (Δn). However, a high concentration (above $10^{18}\,\mathrm{cm}^{-3}$) is required to obtain a significant change in the refractive index (10^{-3} to 10^{-4}) to achieve substantial modulation. The Δn reached for a certain amount of carrier concentration produces a

change in the n_{eff} of the WG mode, which implies a change in the phase velocity of the propagated optical signal. To evaluate the phase shift in the optical signal, the change in n_{eff} due to the applied voltage is determined by Equation (5):

$$\Delta n_{eff}(V) = n_{eff2}(V_2) - n_{eff1}(V_1) \tag{5}$$

where Δn_{eff} is the difference between two states (state 1 or state 2) of the junctions, with each state associated with a specific voltage (V_1 and V_2). The change in n_{eff} results in a phase shift $\Delta\phi$ in the optical mode given by:

$$\Delta\phi = \frac{2\pi\Delta n_{eff} L}{\lambda} \tag{6}$$

where L is the active length of the phase shifter, λ is the wavelength of light in free space, and Δn_{eff} is the effective index change in the WG, which is the difference between the n_{eff} of the WG phase shifter before and after charge accumulation. For a given Δn_{eff} and in order to obtain $\Delta\phi$ equal to π rad, the required modulator length (L_π) is:

$$L_\pi = \frac{\lambda}{2\Delta n_{eff}} \tag{7}$$

Equation (7) predicts that with a high Δn_{eff}, the required length to obtain a phase shift of π rad is reduced. p–n junction modulators have been successfully demonstrated in c-Si WGs [60–63], where, by applying a reverse bias voltage, carriers are depleted in the region of interest. The next step is to study the behavior of c-Si and a-Si p–n junctions for modulating the refractive index, thereby inducing a n_{eff} change in the Si/SiN device, which can be observed through the phase shift of the guided mode.

2.3. p–n Junction Theory and Design

The depletion width (W_D) in a p–n junction is a function of the doping concentration: acceptor concentration (N_A) in the p-region and donor concentration (N_D) in the n-region. In an ideal step abrupt uniform junction, the W_D can be computed with Equation (8):

$$W_D = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0(N_A + N_D)(V_{bi} - V)}{qN_A N_D}} \tag{8}$$

where ε_{Si} is the silicon dielectric constant, ε_0 is the vacuum permittivity, and V is the bias voltage applied in the terminals. V_{bi} is the built-in voltage and can be obtained with (9):

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{{n_i}^2} \tag{9}$$

where k is the Boltzmann constant, T is the absolute temperature, and n_i is the intrinsic concentration of the semiconductor. The existence of V_{bi} is due to the electric field in the junction as a result of the carrier depletion. Applying a negative voltage (reverse bias), the electric field is increased, and more charge quantity is depleted; consequently, the W_D is increased. Figure 3 shows a p–n junction schematic and W_D as a function of the reverse voltage for different doping concentrations, assuming that one side of the p–n junction is heavily doped.

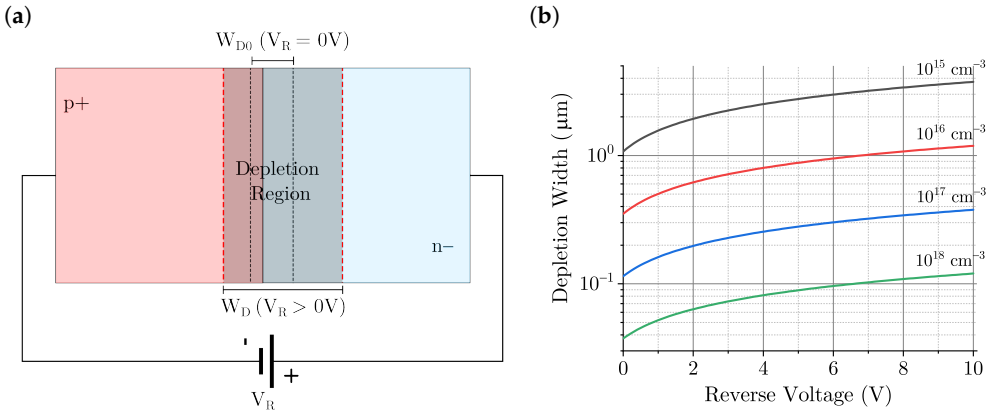

Figure 3. (**a**) p–n junction schematic illustrating the increase in the depletion width with reverse voltage. (**b**) Depletion width of the p–n junction as a function of the reverse voltage. One side is heavily p-doped using a concentration of $>10^{20}$ cm^{-3}, while the doping concentration varies on the other side, n-doped, with $N_D = 10^{15}, 10^{16}, 10^{17}$ and 10^{18} cm^{-3}.

In this case, the p–n junction is assumed to be ideal (abrupt junction), with one side heavily doped to a fixed value ($>10^{20}$ cm^{-3}), while the doping concentration varies on the other side of the junction (one-sided abrupt junction). It is observed that increasing the concentration decreases the total W_D. The depletion region exists on both sides of the junction, where the side with lower concentration has a larger depletion region compared to the side with a higher doping concentration. These quantities have been calculated using the following set of equations:

$$y_p = -\frac{W_D}{1 + \frac{N_A}{N_D}} \tag{10}$$

$$y_n = \frac{W_D}{1 + \frac{N_D}{N_A}} \tag{11}$$

where y_p is the depletion width in the p-region, and y_n is the depletion width in the n-region of the junction. The sum of y_p and y_n results in W_D:

$$y_p + y_n = W_D \tag{12}$$

The ideal current model for a short p–n junction is:

$$J = J_0 \left[e^{\left(\frac{qV}{\eta kT}\right)} - 1 \right] \tag{13}$$

where η is the factor of ideality, and J_0 is the saturation reverse current density, defined as:

$$J_0 = q{n_i}^2 \left(\frac{D_p}{N_A W_n} + \frac{D_n}{N_D W_p} \right) \tag{14}$$

where W_n and W_p are the width of the n-region and p-region in the junction, respectively. D_n and D_p are the diffusion constants, and can be related with the mobility with the Einstein relation:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{q} \tag{15}$$

For the a-Si case, the current follows Equation (13) with some deviations. The ideality factor (η) is greater than 1, suggesting the possible existence of series resistance and defects in the material due to the lack of crystalline periodicity. The built-in voltage (V_{bi}) can be greater than 0.7 V, as the bandgap (E_g) is 1.8 eV according to literature reports [54,58,64]. The saturation reverse current density also varies due to the possible influence of several phenomena, including generation–recombination current, thermal effects on the traps in the semiconductor, and the reduced magnitude of the diffusion constants due to the reduction

in carrier mobilities. Although structural and electronic differences can be found between a-Si and c-Si, the p–n junction theory previously discussed is very similar in both materials, assuming that the dangling bond density in a-Si is controlled during the deposition process through the presence of hydrogen [65,66].

2.4. Lateral and Vertical p–n Junction Structures

The first proposed device consists of a lateral p–n junction with two different scenarios, one using a-Si and the other using c-Si.

a-Si case: For the a-Si scenario, the film is deposited on top of a SiN WG core. Figure 4a shows a 2D transverse cut of the structure, obtained using Synopsys Sentaurus. The initial approach involves using a symmetrical a-Si junction, with the p-region and n-region each having a width of 500 nm. The metallurgical junction is at the WG center. The p-doped side has a boron concentration of 10^{18} cm^{-3}, and the n-doped side has a phosphorus concentration of 10^{17} cm^{-3}. Before the a-Si deposition, an additional SiO_2 layer is deposited on the SiN patterned structures and planarized to the SiN level. On the planar surface, a 50 nm a-Si layer is deposited, and the p–n junction is created. At the extremes of both sides, the heavily doped p-region (p++) and n-region (n++) are built to serve as electrodes. Finally, a 2 µm SiO_2 capping layer is deposited to protect the device. Final SiO_2 cladding etching is required to reach the contacts.

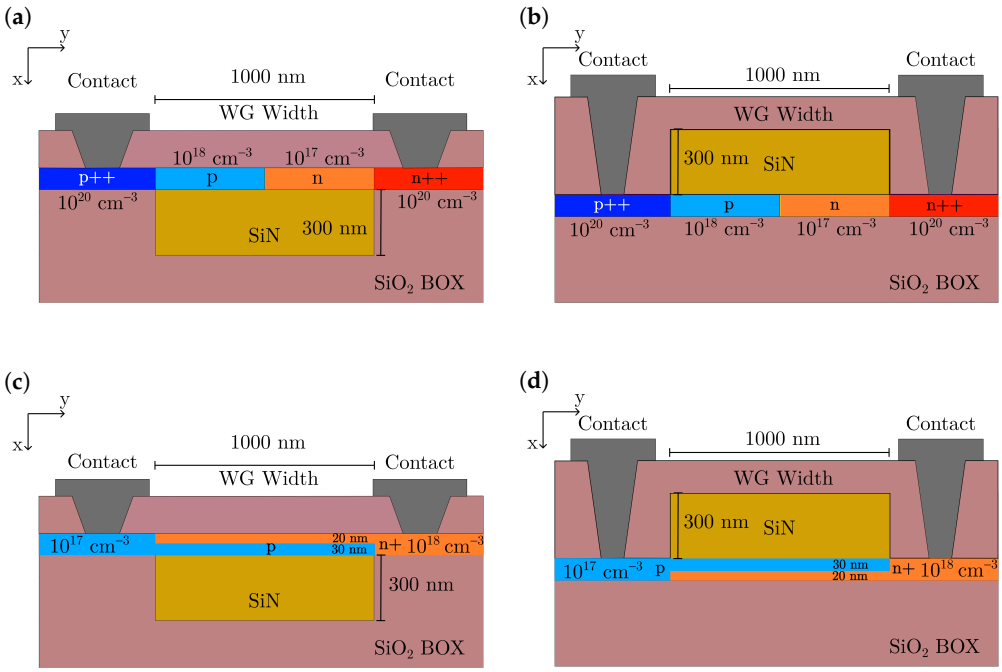

Figure 4. Lateral p–n junction with (**a**) a-Si on top of the SiN WG and (**b**) c-Si on bottom. Both a-Si and c-Si layers have a thickness of 50 nm. (**c**) Vertical p–n junction with a-Si on top of the SiN WG and (**d**) c-Si at the bottom. Not to scale.

c-Si case: For the c-Si scenario, the fabrication starts from a SOI wafer with a 50 nm thick c-Si layer. The process involves etching all the Si except for the area of the modulator. Afterward, the implantation occurs, followed by the deposition of a SiO_2 layer on top, which is then planarized to the level of the c-Si modulator. The concentration of the films and the geometrical position of the p–n junction are the same as for the a-Si case. In the next step, 300 nm of SiN are deposited using LPCVD, and the structures are patterned by etching. The last step is to deposit SiO_2 to protect the structures, followed by etching down the 2 µm SiO_2 cladding to reach the contacts, as illustrated in Figure 4b.

The second proposed device is a vertical p–n junction on top of the SiN WG for the a-Si case, and at the bottom of the SiN WG for the c-Si, as shown in Figure 4c,d, respectively. The

SiN photonics elements are obtained using similar fabrication steps to the lateral design. In this case, the p–n junction is created with a first a-Si layer of 30 nm doped with a boron concentration of 1×10^{17} cm^{-3}. Then, a 20 nm second layer of a-Si is placed on top to form the n-region, with a phosphorus concentration of 1×10^{18} cm^{-3}. For the c-Si vertical p–n junction modulator, it is the other way around: first, the n-region is created and then the p-region. This second proposed device presents a more difficult fabrication process compared to the lateral junction, due to the accurate control required in forming the vertical junction within a 50 nm Si film. The carrier profiles for the lateral and vertical junctions help to understand the change in free carriers and their effect on the optical properties of the Si/SiN modulator.

3. Results and Discussion

The previously obtained structures were transferred to the Synopsys-Sentaurus Device to perform the electrical simulations. Poisson's equation and the carrier continuity equations are coupled and solved in thermal equilibrium and under different biasing conditions. Poisson's and the continuity equations are [67–69]:

$$\nabla^2 \psi = -\frac{q}{\varepsilon}(p - n_e + N_D - N_A) \tag{16}$$

$$\nabla \cdot \vec{J_{n_e}} = q(G_{n_e} - R_{n_e}) + q\frac{\partial n_e}{\partial t} \tag{17}$$

$$\nabla \cdot \vec{J_p} = q(G_p - R_p) - q\frac{\partial p}{\partial t} \tag{18}$$

where ψ is the electrostatic potential, N_A and N_D are the acceptor and donor dopant concentrations, p, n_e, $\vec{J_{n_e}}$, $\vec{J_p}$, G_{n_e}, G_p, R_{n_e} and R_p are the carrier densities, the current densities, the carrier generation rate and recombination rates for electrons and holes, respectively.

Electron and hole distributions were calculated. In addition, the simulation tool incorporates advanced semiconductor physics models to account for carrier statistics, doping and field-dependent carrier mobility, and doping-dependent carrier recombination lifetimes. The applied voltage was swept from 0 V to −10 V in the case of reverse bias (V_R) and, for forward bias (V_F), the sweep was performed from 0 V to 2 V to obtain carrier profiles under high injection conditions. Carrier distributions at each bias point were computed. According to plasma dispersion equations [52,55], free carrier concentrations were transformed into refractive index shifts at each bias point. It is important to highlight the disparity between the physical properties of c-Si and a-Si. While silicon models applicable to c-Si provide valuable insights, several parameters need adjustment for accurate representation of a-Si, including bandgap energy, carrier mobilities, trap defect density, effective masses, and others. Table 1 presents a comprehensive comparison of the physical properties of both c-Si and a-Si to facilitate a meaningful comparison. Some of these parameters depend on the characteristics of the material, obtained through its manufacturing method and process variables [58,59,64,66,67,70–75]. While the carrier transport, current, and built-in voltages in the junction can vary, the charge profile remains similar to that of c-Si.

Table 1. Comparison of the semiconductor parameters between a-Si and c-Si [58,59,64,66,67,70–75].

Physical Parameter	a-Si	c-Si
E_g (eV)	1.80	1.12
μ_n (cm^2/(V s))	1–25	1350
μ_p (cm^2/(V s))	0.01–6	480
ε_{Si}	11.8	11.7
m^*_{ce}/m_0	0.2–0.55	0.26
m^*_{ch}/m_0	0.5–1	0.39
τ_n (s)	10^{-7}	10^{-6}
τ_p (s)	10^{-7}	10^{-6}

3.1. Electrical Results

3.1.1. Lateral p–n Junction Results

Figure 5 shows the transversal free carrier concentration and refractive index shift profiles for the lateral p–n junction on the SiN WG in thermal equilibrium (0 V). The temperature is 300 K. At room temperature, the active dopants in the neutral region can be considered to be in complete ionization condition. This means that the concentration of free holes and electrons equals the corresponding dopant concentration:

$$\Delta P = N_A, \Delta N = N_D \tag{19}$$

where ΔP and ΔN are also called majority carriers. For the p-doped side, the majority carriers are holes, and the minority carriers are electrons (n_{p0}). For the n-doped side, electrons are the majority carriers, and holes are the minority (p_{n0}):

$$n_{p0} = \frac{{n_i}^2}{N_A}, p_{n0} = \frac{{n_i}^2}{N_D} \tag{20}$$

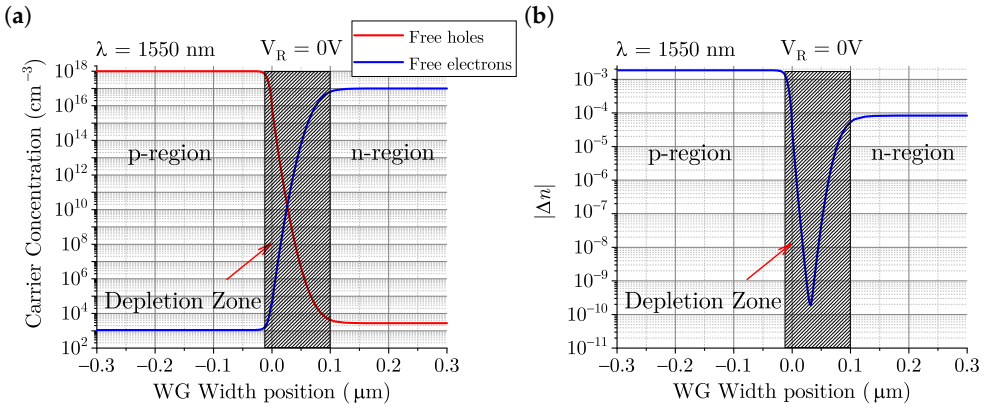

Figure 5. (**a**) Transversal free carrier concentration and (**b**) refractive index shift profiles in the Si lateral p–n junction in equilibrium.

The existence of a built-in electric field produces an initial depletion width (W_{D0}) equal to 110 nm. In this region of the device, available carriers have a very low density, and the refractive index shift has no significant value for modulation and can be considered negligible. Applying more reverse voltage extends the W_D, reducing the available charges, thus producing a larger shift in the refractive index. Figure 6 shows the transversal free carrier concentration and refractive index shift profiles for the lateral p–n junction on the SiN when biased with V_R = 5 V. The decrease in available carriers in the material reduces the effect on the change of the refractive index. The extension of this zone in the n-region is greater than in the p-region. When the reverse voltage is 5 V, the W_D is 290 nm. High voltage is required to obtain a W_D of 1 µm, which is technologically unreachable because the breakdown voltage in the junction is below the target reverse voltage for covering the whole WG width. In order to overcome this issue, forward bias in this kind of structure was explored. Figure 7 shows the profiles for the lateral p–n junction on the SiN when biased with V_F = 1 V.

Forward bias was explored to obtain a high injection rate of carriers in the p–n junction. It can be observed that the concentration of holes in the p-region increases by nearly one order of magnitude (majority carriers) (see Figure 7a) compared to the initial condition with V_R = 0 V displayed in Figure 5a. Notably, the concentration of electrons (minority carriers) increases by several orders of magnitude, from around 10^3 cm^{-3} (see Figure 5a) up to a concentration of 8×10^{18} cm^{-3} (see Figure 7a), close to the value of holes. With this carrier density, Δn is equal to 1.8×10^{-2}. Similarly, in the n-region, electrons and holes have a concentration of 4×10^{18} cm^{-3}, and the resulting Δn is 9×10^{-3}. Figure 8a shows the current density J in the p–n junction under the forward bias voltage, and Figure 8b

shows the power consumption (P_C) for varying voltages at specific modulator lengths. With this voltage (V_F = 1 V), the current density is around 157 kA/cm^2, and for a device with a thickness of 50 nm and a length of 500 µm, the power consumption is around 39 mW.

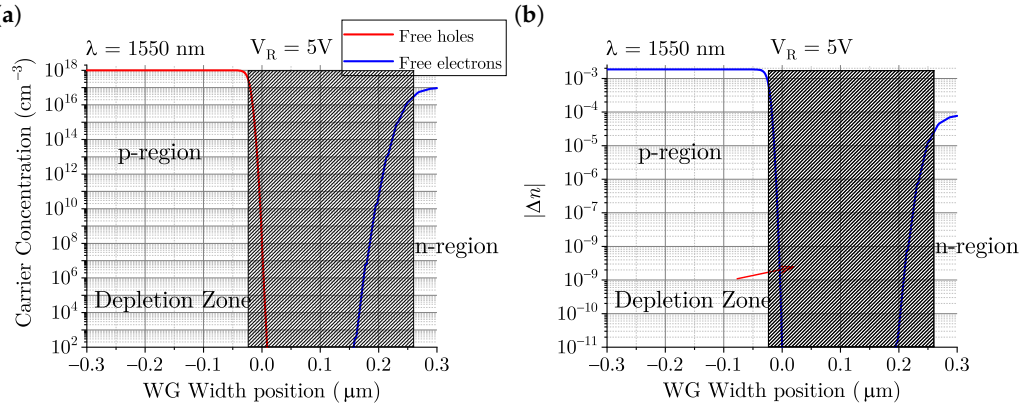

Figure 6. (**a**) Transversal free carrier concentration and (**b**) refractive index shift profiles in the Si lateral p–n junction with V_R = 5 V.

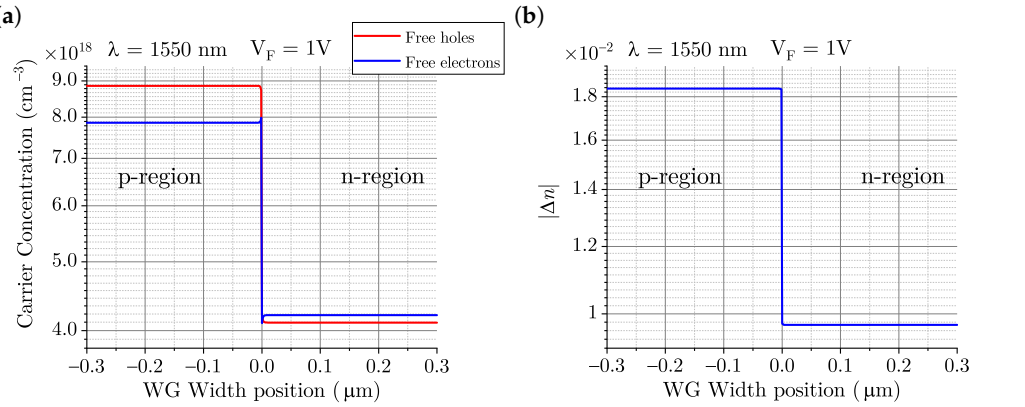

Figure 7. (**a**) Transversal free carrier concentration and (**b**) refractive index shift profiles in the Si lateral p–n junction under forward bias, V_F = 1 V.

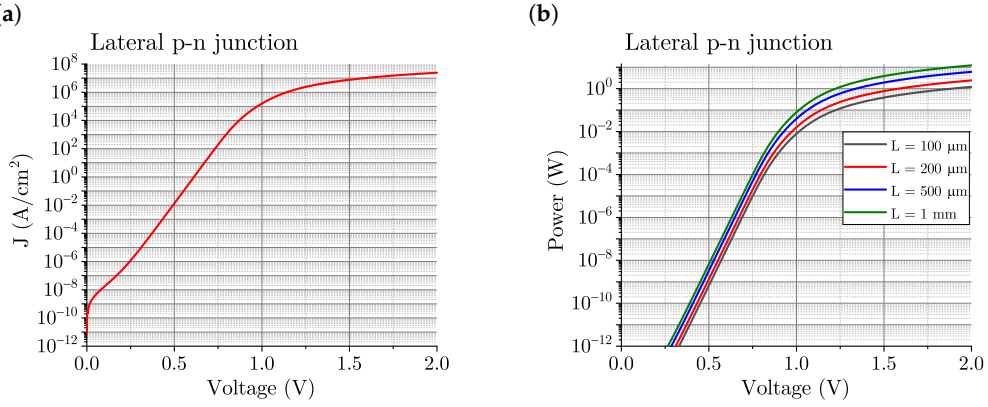

Figure 8. (**a**) Current density and (**b**) power consumption in the lateral p–n junction under forward bias for a Si thickness of 50 nm and for different modulator lengths.

3.1.2. Vertical p–n Junction Results

Figure 9a,b depict the structure and the refractive index profile for the vertical p–n junction. In the n-region, the higher concentration N_D is equal to 10^{18} cm^{-3}, and the

p-region concentration is $N_A = 10^{17}\,\mathrm{cm}^{-3}$. With a uniform N_D, Δn is 8.38×10^{-4} in the n-region. This can be considered constant throughout the film at all reverse bias points because the depletion width inside this region is smaller compared to the depleted width in the p-region. When the junction is biased with $V_R = 0\,\mathrm{V}$, the built-in depletion width (W_{D0}) is around 30 nm and covers the entire p-region; see Figure 9a. In the depletion area, the free carrier concentration decays very rapidly, decreasing the values of Δn below 10^{-5}, this means that Δn in this zone is negligible. To reduce the W_D, it is necessary to bias the device with forward voltage (V_F). Forward bias counteracts the internal barrier potential, reducing the W_D and allowing carrier injection across the junction. Biasing the junction with $V_F = 0.9\,\mathrm{V}$ results in a reduction in the depleted p-region in the direction perpendicular to the surface of the nitride. The W_D is now around 1.2 nm at 0.9 V. Δn in the p-region is 6.50×10^{-4} and the n-region is 1.24×10^{-3} due to the carrier injection contribution. With $V_F = 1\,\mathrm{V}$, the W_D becomes very narrow (below 1 nm) and the current (free carrier injection) increases. At this level, Δn in the p-region is 1.12×10^{-3} and Δn in the n-region is 1.95×10^{-3}. Varying the voltage from $V_R = 0\,\mathrm{V}$ to$V_F = V_{bi}$, W_D is modulated from 30 nm to 0 nm within the p-region. Figure 9c,d display the vertical profile for free carriers and the corresponding Δn under a forward bias of 0.9 V. Vertical modulation with this structure promotes a uniform and constant depletion modulation across the entire width of the WG. By varying the voltage from 0 V to V_{bi} in forward bias, the 30 nm p-region changes from fully depleted to un-depleted, achieving Δn tuning from 0 (zero free carriers) to the value defined by the acceptor concentration in the p-region plus the free carriers injected.

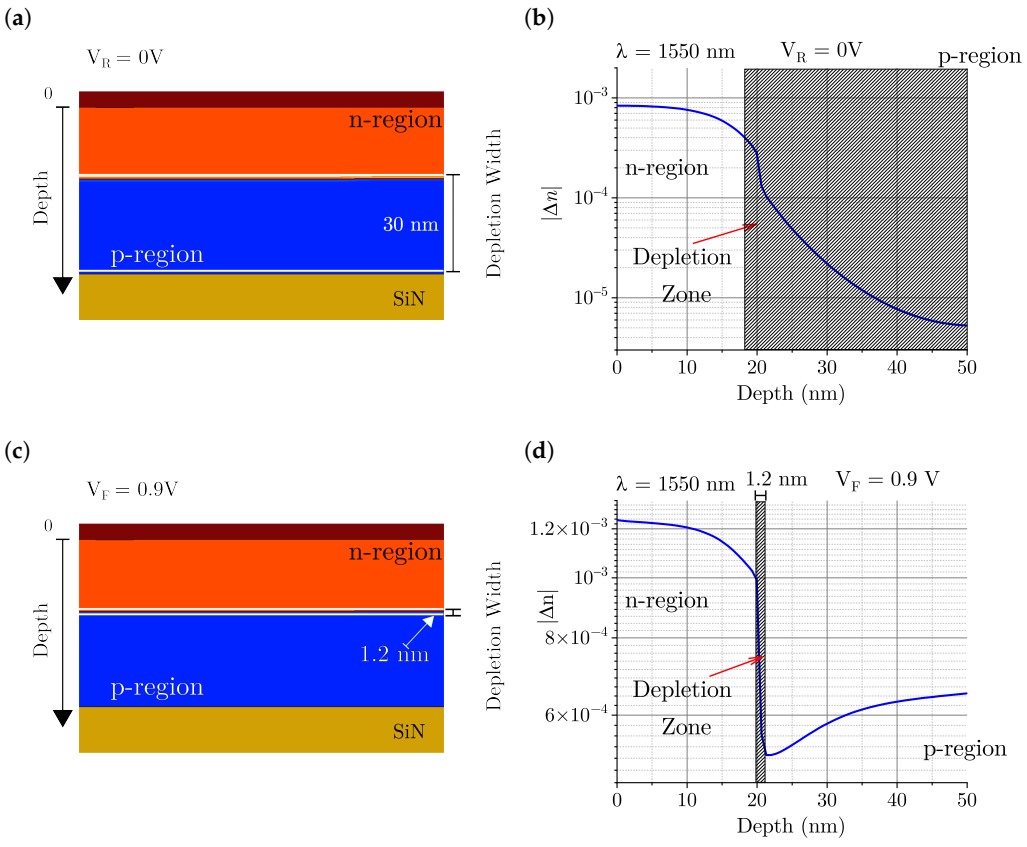

Figure 9. Vertical p–n junction and refractive index shift along the vertical direction. (**a**) Vertical cross-section with $V_R = 0\,\mathrm{V}$. (**b**) Δn with $V_R = 0\,\mathrm{V}$. (**c**) Vertical cut with $V_F = 0.9\,\mathrm{V}$ (**d**) Δn with $V_F = 0.9\,\mathrm{V}$.

Figure 10a shows the current density J in the vertical p–n junction under forward bias voltage, and Figure 10b shows the power consumption for varying voltages at specific modulator lengths. With voltage $V_F = 0.9\,\mathrm{V}$, the current density is around

471 A/cm^2, and for a device with a width of 1 µm and a length of 2 mm, the power consumption is around 8.49 mW.

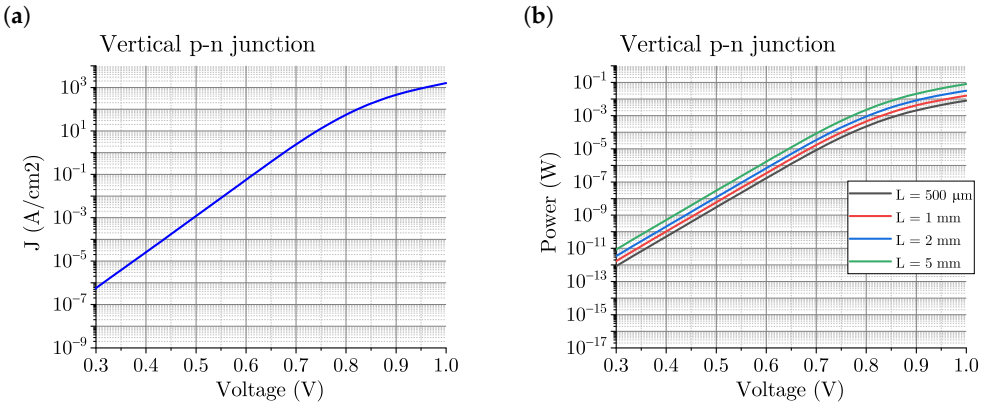

Figure 10. (**a**) Current density and (**b**) power consumption in the vertical p–n junction under forward bias for different modulator lengths using a Si thickness of 50 nm and width of 1 µm.

3.2. Optical Results

The presented modulators have been electrically simulated, but they face optical challenges. To simulate the optical response of the device under study, the free carrier profiles obtained by electrical simulation are translated into Δn and $\Delta \alpha$ variations using the Drude model presented previously in Section 2.2. The refractive indices of the different materials are incorporated into a 2D model in COMSOL Multiphysics, utilizing the mode solver module. The n_{eff} and extinction coefficient for transverse electric (TE) and transverse magnetic (TM) modes are calculated for the different Δn and $\Delta \alpha$ states induced by the bias voltage applied to the p–n junctions. Figure 11 displays the electric fields of the fundamental TE and TM modes at a wavelength of 1550 nm for a bare WG and WGs with the a-Si and c-Si modulators.

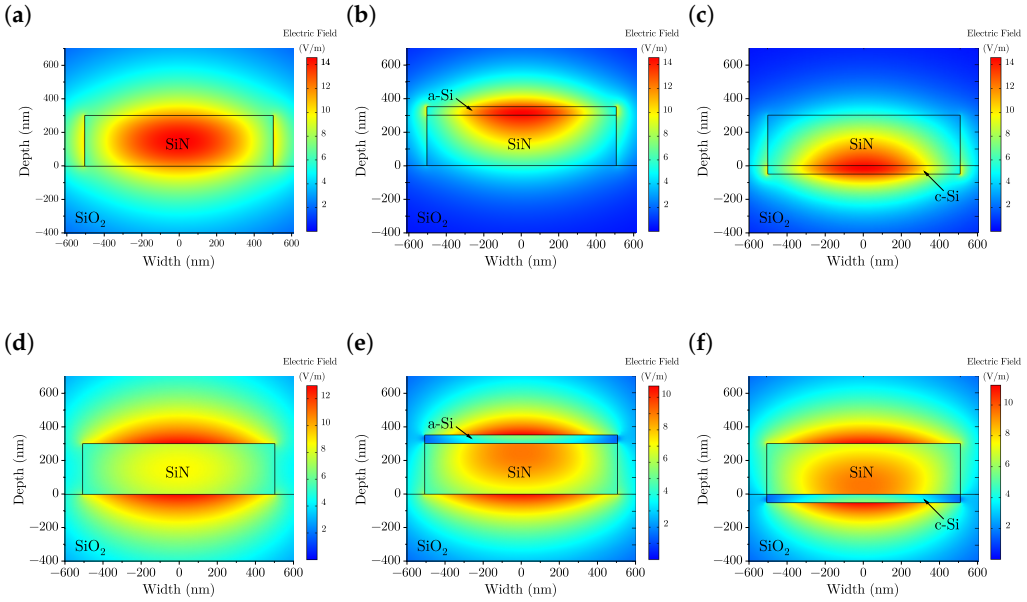

Figure 11. (**a**–**c**) TE and (**d**–**f**) TM mode profiles of the SiN bare WG core, and with a-Si or c-Si, respectively.

The refractive indices used in the optical solver are n_{SiO_2} = 1.44, n_{SiN} = 2.00 and n_{Si} = 3.48. In Figure 11a, corresponding to the TE mode for the SiN WG core only, the electric field is confined within the core as expected, with a value in the n_{eff} of 1.5774 for TE

and 1.5052 for TM; see Figure 11d. With the 50 nm thick a-Si film on top of the WG, serving as the active part of the modulator, the confined wave is modified as shown in Figure 11b. The mode is shifted upwards across the a-Si and SiN area because the refractive index of a-Si is higher than that of SiN. Consequently, the effective refractive index ($n_{eff_{Si}}$) of the mode increases up to 1.8500 for the TE and 1.5934 for the TM. This value shows a significant contrast compared to SiN without a-Si. For the c-Si modulator as shown in Figure 11c, the mode is shifted downwards across the c-Si layer due to the same physical principle as for the a-Si case. This results in the same effective refractive index and optical contrast at the facets of the modulator. To determine the power losses resulting from reflection at the interfaces of the modulator and the bare WG (high optical contrast between n_{eff}), a longitudinal optical simulation was conducted for the TE fundamental mode. Figure 12 shows the longitudinal cut of the WG with Si. Figure 12a illustrates the abrupt case where the propagated mode encounters the step change of $n_{eff}/n_{eff_{Si}}$. The presence of a Si layer, crystalline or amorphous, on top or under the SiN WG creates a significant index contrast, resulting in reflections at the interfaces between the bare WG and the active part, with losses exceeding 3 dB in the optical device. To address these issues, Si tapers are proposed for the input and output facets of the modulator, see Figure 12b. These tapers will provide a gradual change in n_{eff}, reducing the optical contrast and reflections. The optical power through the modulator has been studied for different taper lengths; see Figure 12c. Using tapers with lengths above 50 µm will reduce the optical contrast and reflections, thereby improving the losses of the two facets below 0.5 dB; see Figure 12d.

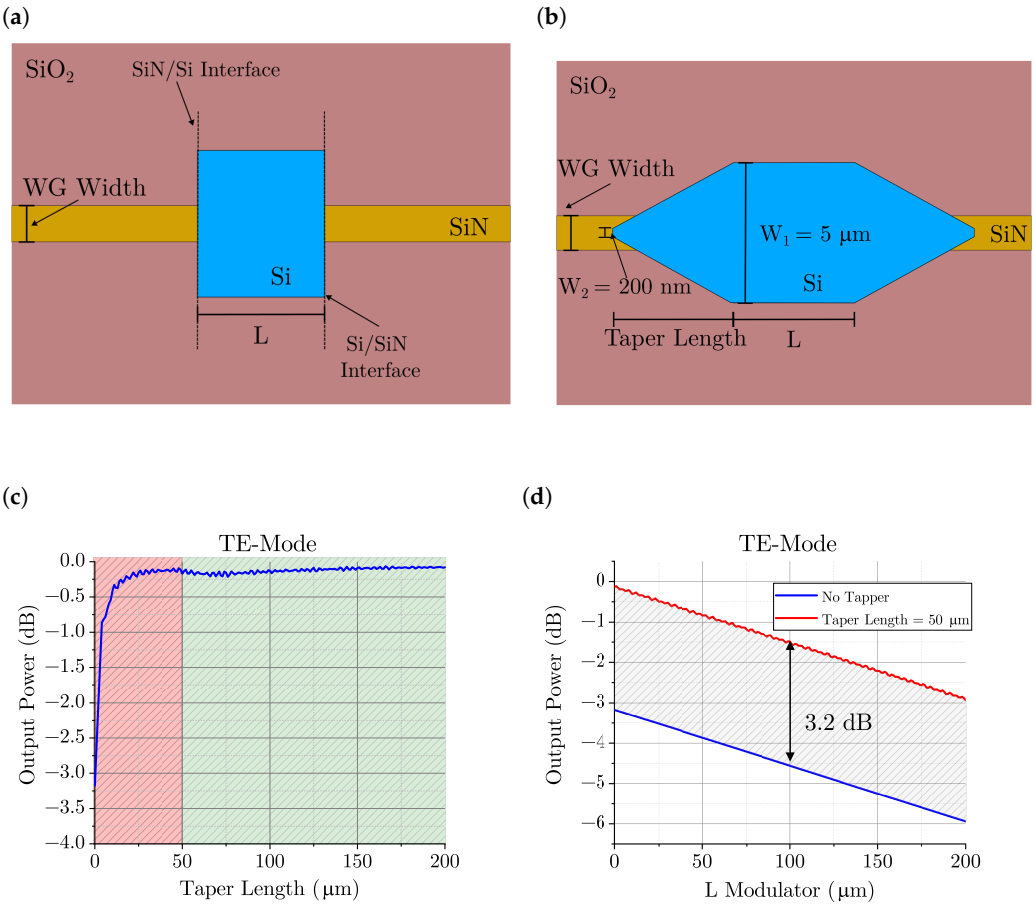

Figure 12. (**a**) Schematic of the abrupt interface between the bare waveguide and the modulator. (**b**) Schematic of the modulator using tapers at the interfaces. (**c**) Optical power through the modulator for different taper lengths for the TE mode. (**d**) Optical power for different modulator lengths with tapers of length 50 µm and without tapers.

3.2.1. Lateral p–n Junction Modulator

According to the electrical results of the lateral p–n junction with acceptor and donor concentrations of 10^{18} cm^{-3} and 10^{17} cm^{-3}, respectively, achieving a W_D of 1 µm, covering the whole WG width, requires a high reverse voltage bias, which can lead to device breakdown. To elevate the Δn and reduce the footprint of the modulator, more free carriers are required as indicated by Equation (7). For the symmetrical p–n junction, a forward bias near the high injection condition is proposed to increase the carrier density in the Si film (both amorphous and crystalline), thereby overcoming the breakdown voltage issue associated with reverse bias. Figure 13 displays the value of n_{eff} for different voltages ranging from 0 V to V_F = 1 V. For 1 V, Δn_{eff} is equal to 0.0036 for the TE and 5 × 10^{-4} for the TM, resulting in L_π = 215 µm and 1550 µm, respectively. An alternative configuration would involve creating a non-symmetrical p–n junction, with the n-region covering the width of the WG and the p-region positioned on one side away from the WG. For this configuration, Δn_{eff} is 0.0027 for TE and 4 × 10^{-4} for TM under an applied forward bias of 1 V. The corresponding L_π is 287 µm in the TE polarization and 1937 µm in the TM. Swapping the positions of the n-region and p-region, with the p-region now covering the width of the WG, Δn_{eff} is 0.0046 for TE and 7 × 10^{-4} for the TM, again, using a forward bias of 1 V. In this case, L_π is 168 µm for TE and 1107 µm for TM. When the p-region covers the complete width of the WG, the length of the modulators is smaller. This is because free holes produce a bigger change in the refractive index compared to free electrons at 1550 nm as predicted by Figure 3a. From Figure 3b, it can also be seen that the doped Si films exhibit a variation in the extinction coefficient when a change in the refractive index occurs. Therefore, doping the layers increases the material losses. The IL of the modulator have also been calculated, being below 3.2 dB for the c-Si modulators and below 10.2 dB for the a-Si modulators. Since the photonic structure is the same for all three cases, the only difference being the position of the metallurgical junction, the current–voltage curves are very similar to Figure 8a. The current (and the power consumption) is a function of the modulator footprint, being proportional to L_π. A summary of Δn_{eff} and L_π for all the studied p–n lateral junction cases in both TE and TM modes is presented in Figure 13.

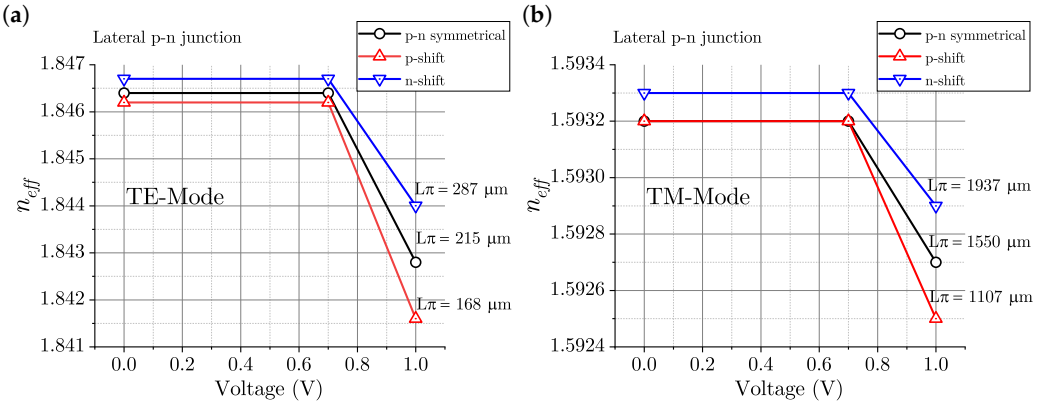

Figure 13. n_{eff} variation as a function of voltage and L_π for the different lateral p–n junction approaches for the (**a**) TE mode and (**b**) TM mode.

A thin film of SiO_2 between the SiN waveguide and the Si layer may exist due to the planarization process precision control. Depending on the thickness, the performance of the device will vary, according to Figure 14. In all cases, the length to obtain a π phase shift is longer when the SiO_2 film is thicker, but the IL remain almost constant. The same explanation applies for vertical modulators which will be covered in the following section.

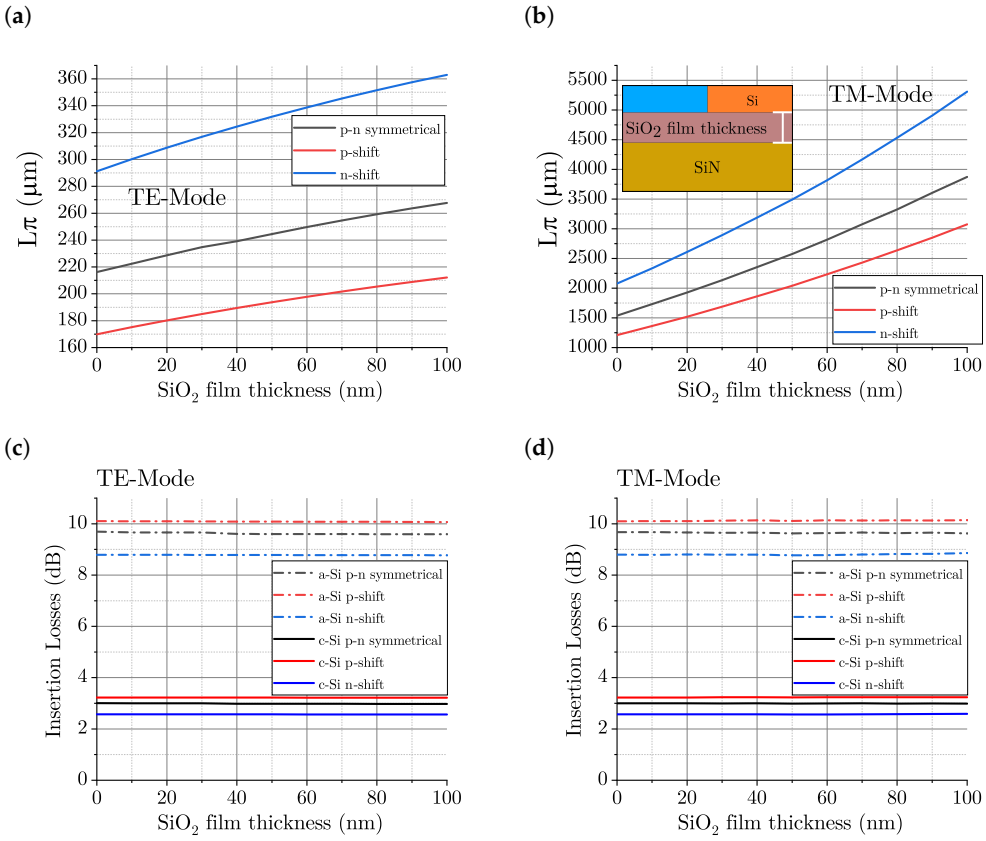

Figure 14. Variation in L_π for (**a**) TE and (**b**) TM modes, with an inset of the schematic of the structure (not to scale), and insertion losses for (**c**) TE and (**d**) TM modes depending on the SiO_2 film thickness for the different lateral p–n junction approaches.

3.2.2. Vertical p–n Junction Modulator

The voltage applied to the vertical p–n junction device induces a change in the n_{eff}, similar to the effect observed in the previously explained lateral p–n junction. In this case, two different forward biases are utilized, 0.9 V and 1 V. For the first forward bias, L_π is 5.03 mm for TE mode and 38.75 mm for the TM mode, with associated losses of 3.16 dB and 3.95 dB, respectively, for the c-Si modulator. For the a-Si modulator, the losses are 13.78 dB for the TE mode and 16.85 dB for the TM mode. When applying a bias of 1 V, L_π decreases to 2.5 mm for the TE mode and to 18.02 mm for the TM mode, with losses of less than 2.8 dB for the c-Si modulator and less than 11.7 dB for the a-Si modulator. Figure 15 shows the value of n_{eff} for different voltages ranging from 0 V to $V_F = 1$ V with the corresponding L_π for the TE and TM modes.

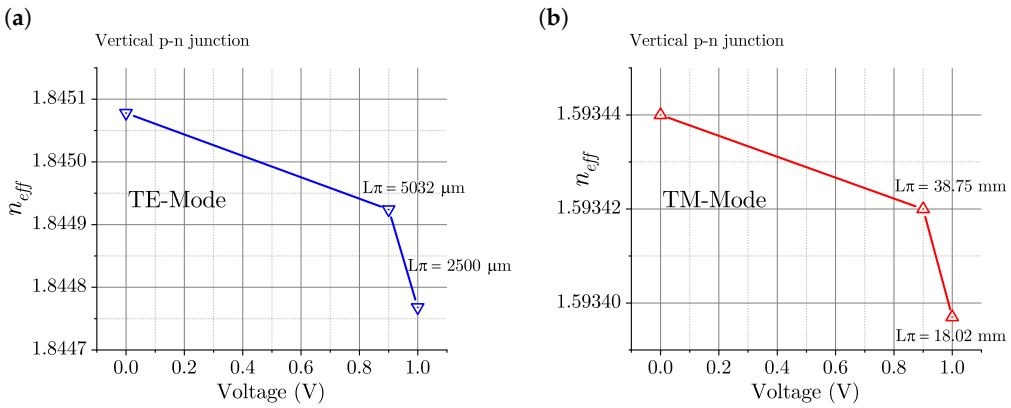

Figure 15. n_{eff} variation as a function of voltage and L_π for the vertical p–n junction for the (**a**) TE mode and (**b**) TM mode.

3.2.3. Comparative Analysis: Lateral and Vertical p–n Junctions on SiN vs. Thermal Tuners

Table 2 summarizes the footprint, operating voltage, power consumption, optical loss, and speed of the various Si/SiN p–n junction modulators studied in this paper. This table details the key findings and advantages of each modulator configuration, providing a comprehensive overview. Moreover, a comparison with the current most exploited CMOS compatible phase modulators in SiN platform, which are the thermal tuners, is presented. In summary, Si/SiN p–n-junction modulators offer high modulation efficiency and faster response times, making them suitable for applications that require rapid and efficient phase modulation, despite their higher losses compared to thermal tuners. These characteristics make them ideal for high-speed optical communication systems, where quick and accurate modulation is essential. On the other hand, thermal tuners provide simplicity, versatility, and reliable performance, making them a popular choice for a wide range of applications. Thermal tuners are particularly favored in scenarios where modulation speed is less critical but ease of integration and robustness are important considerations. The decision to use Si/SiN p–n junction modulators versus thermal tuners should be based on the specific application requirements. For high-speed performance, compact size, reduced thermal crosstalk, and high-efficiency modulation, Si/SiN p–n junction modulators are preferred. For applications where simplicity, versatility, low-loss and reliable performance are more critical, thermal tuners are an excellent choice. The detailed comparison in Table 2 provide a clear understanding of the trade-offs involved in selecting the appropriate modulator type for specific applications.

The speed of the modulator depends on the bias point of the p–n junction. In reverse bias, the speed is determined by the depletion capacitance, promoting an operation frequency up to hundreds of GHz [76]. This is because the capacitance can be reduced by increasing the reverse voltage bias. In forward bias, the depletion capacitance is at its maximum, and an additional capacitance appears due to carrier injection diffusion. The diffusion capacitance is a function of the carrier lifetime (or transit time in short junctions) and increases with the current injection. For silicon, this limits the speed to the order of MHz [77,78].

Table 2. Comparison of CMOS compatible SiN-based optical modulator performance using amorphous or crystalline silicon, detailing modulator length, applied voltage, power consumption, insertion losses, and speed.

Electro-Optical Device	**L_π (μm)**		**Voltage (V)**	**P_C (mW)**		**IL (dB) (c-Si)**		**IL (dB) (a-Si)**		**Speed**
	TE	**TM**		**TE**	**TM**	**TE**	**TM**	**TE**	**TM**	
Lateral p–n	215	1550	$V_F = 1$	16.95	122.2	3.0	3.2	9.63	10.21	∼MHz
Lateral p-shift	168	1107	$V_F = 1$	13.24	87.27	3.2	3.2	9.97	9.67	∼MHz
Lateral n-shift	287	1937	$V_F = 1$	22.62	152.8	2.2	2.2	8.61	8.60	∼MHz
Vertical p–n	5033	38,750	$V_F = 0.9$	21.35	164.40	3.16	3.95	13.77	16.85	∼MHz
Vertical p–n	2500	18,023	$V_F = 1$	39.78	286.82	2.46	2.78	10.52	11.69	∼MHz
Thermal Device	**L_π (μm)**			**P_C (mW)**		**IL (dB)**				**Speed**
Thermal tuners Ref. [79]	1000			5–175		<1				∼kHz

The modulator length L_π for both c-Si and a-Si modulators is comparable because the real part of the refractive index exhibits similar changes in response to the applied electric field in both materials. However, when considering IL, a-Si modulators tend to be more lossy than their c-Si counterparts due to the lower carrier mobility in a-Si. Despite this, a-Si offers several advantages over c-Si. Firstly, a-Si has a larger bandgap, which allows for higher Zener breakdown voltages. This characteristic is particularly beneficial for modulators operating at high electric fields, as it reduces the likelihood of breakdown and allows for greater modulation depths. Moreover, a-Si modulators are well suited for integration into 3D stacking technologies. This compatibility is advantageous for advanced photonic integrated circuits, where the vertical stacking of devices can lead to more compact

and complex architectures. Another significant advantage of a-Si is the ability to tailor its optical properties during the deposition process. This flexibility enables the customization of the film's properties to meet specific requirements, enhancing the versatility of a-Si modulators. The quality of the deposited a-Si film plays a critical role in determining the carrier mobility, and consequently, the modulator loss. In this study, standard mobility values for a-Si were used, but there is potential to reduce losses by optimizing the deposition process to improve the quality of the a-Si film. Enhancing the film quality can lead to higher carrier mobilities, thereby reducing optical losses and improving the overall performance of a-Si modulators, potentially making them competitive with c-Si modulators.

TM polarization has demonstrated lower optical contrast for different applied voltages, which results in the need for a larger modulator footprint to achieve the same modulation as TE polarization. This increased footprint translates to higher power consumption for TM polarized modulators. In terms of IL, both TM and TE polarizations exhibit losses of a similar order of magnitude, offering no significant advantage to TM polarization over TE polarization in this respect. For both polarizations, the design of the lateral p–n junction has a significant impact on the footprint and performance of the modulator. A lateral p–n junction that is completely the p-region exhibits a smaller footprint due to the high contrast provided by the free holes compared to free electrons. This higher contrast leads to more efficient modulation in a smaller area. Conversely, a lateral p–n junction that is completely the n-region results in a larger footprint due to the lower contrast provided by free electrons. A symmetric approach, incorporating both the p-region and n-region, offers a middle ground in terms of footprint and modulation efficiency. For the TE mode and all lateral p–n junction configurations, the footprint is smaller than that of thermal tuners, leading to lower power consumption overall. However, they exhibit higher losses, and due to the inability to cover the entire waveguide width when operating in reverse bias, the power consumption can be comparable to thermal heaters when operating in direct bias.

Vertical junctions have a larger footprint than lateral ones and losses of the same order, being a bit higher when operating at 0.9 V and slightly lower when operating at 1 V. So, even though the vertical approach can work and allows light modulation, it shows no significant benefits when compared with the lateral structures. Overall, the lateral approach shows better performance than the vertical approach. Compared with thermal tuners, vertical junctions operate faster with a similar overall energy consumption but higher losses and larger footprint.

4. Conclusions

The proposed electro-optical modulators for SiN photonics introduce a complementary approach utilizing a thin film of amorphous or crystalline silicon p–n junction on top or under the silicon nitride WG. These modulators leverage the free carrier plasma dispersion effect, demonstrating promising performance and phase shift capabilities through electrical and optical simulations. The compact design allows for modulators below 1 mm in length, reducing optical losses and enabling competitive footprints compared to state-of-the-art modulators in SiN foundries. Furthermore, the proposed devices can be fabricated using CMOS-compatible processes on existing SiN photonics platforms. Considering factors like back-scattering and Zener breakdown, additional structures such as capacitors can provide a trade-off between length and carrier concentration and could offer further enhancements. Experimental design and fabrication are currently underway to refine physics models and validate results for platform development. Additionally, exploring other semiconductor materials with minor refractive index differences could mitigate back-scattering effects, allowing to reduce the length of the tapers while optimizing the device performance. In the future, fabrication and measurements will be conducted to validate the proposed approach and assess its practical applicability.

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