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Research on Electro-Optic Hybrid Multidigit Digital Multiplier Based on Surface Plasmon Polariton Technology

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Abstract: Digital multipliers are the core components of digital computers, and improving the speed of transistor electronic computers during computation has almost reached its limit, with high power consumption. In this paper, we proposed an electro-optic hybrid multidigit digital multiplier based on SPP technology, which has the advantages of high speed and low power consumption in optical logic, as well as flexible electrical operation and easy storage. The electro-optic hybrid digital multiplier mainly consists of an electrical AND logic gate, an electro-optic hybrid half adder, and an electro-optic hybrid full adder. The optical logic unit is controlled by activated ITO materials to achieve optical-domain operations, and then the multiplication calculation results are converted into electrical signals through photoelectric conversion. The experimental results show that when the scale is 64 × 64 bits, compared with transistor digital multiplication, the energy consumption is reduced by 48.8%; the speed is increased by a factor of 28; and the volume of the electro-optic hybrid digital multiplier device is larger than that of the transistor multiplier, saving 59.9% of the area. For optical transmission loss, a single adder outputs 0.31 dB at different device scales, while the carry output continuously increases with device scale. At scales of 8 × 8 bits, 16 × 16 bits, and 64 × 64 bits, the insertion losses at the sum output ports are 1.03 dB/μm and 1.87 dB/μm, respectively.

Keywords: electro-optic hybrid digital multiplier; electro-optic hybrid full adder; activating material; surface plasmon polariton

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1. Introduction

With the continuous improvement of on-chip integration, it has become increasingly difficult to continue increasing the number of transistors in a single area. It seems that Moore's Law has lost its effectiveness [1,2], and the further improvement of transistor computing performance has encountered a bottleneck. Although multi-core processor technology can improve processing speed, effectively managing and scheduling multiple cores to maximize performance remains a challenge [3]. With the improvement of computer performance, energy consumption and heat dissipation issues are becoming increasingly serious, and high energy consumption and heat dissipation will also limit the further improvement of transistor computer performance [4,5]. Optical computing has advantages such as high speed, low power consumption, and avoidance of electromagnetic interference [6,7]. In recent years, computational methods derived from optical high-performance computing systems have been proposed by scholars, attracting a great deal of attention in the industry. Early research mainly focused on utilizing the nonlinear characteristics of nonlinear media for nonlinear thermal/electro-optical modulation, such as utilizing nonlinear characteristics such as semiconductor optical amplifiers, photonic crystals, and electric absorption modulators to achieve all optical logic functions [8–12].

These traditional optical devices have problems such as large volume, high power consumption, and difficulty in making photonic crystals. In order to solve the problem of low modulation rates, scholars have proposed to utilize the high efficiency and electron mobility of single-molecule graphene materials [13]. However, the production process of single-layer graphene materials is complex and not compatible with metal oxide processes, which is not conducive to the integration of large-scale devices [14]. SPP (surface plasmon polariton) technology has been discovered and proposed for application in Wiener optoelectronic devices. The incident photons resonate with metal electrons, limiting them to a small range. This technology solves the problem of optical diffraction in the production of optical devices and creates the opportunity to produce devices smaller than the optical wavelength size [15–18]. However, the severe oscillation of SPPs and the strong Ohmic attenuation of metals result in significant optical insertion losses in devices, making it difficult to integrate them on a large scale. Therefore, it is necessary to find a balance between reducing Ohmic attenuation and resolving optical diffraction problems in SPP technology for silicon-based hybrid waveguides, in order to obtain smaller device sizes and smaller optical attenuation [19,20]. Therefore, this paper proposes a multi-bit digital multiplier for electro-optic mixing based on SPP technology with silicon-based waveguide mixing. This multiplier utilizes the advantages of high speed and low power consumption due to its optical nature, as well as the advantages of transistor multiplier structure, such as easy data manipulation and storage, to achieve a multi-bit digital multiplier for electro-optic mixing. The main innovations of this paper are as follows:

(1) An electro-optic hybrid multidigit digital multiplier based on SPP technology using silicon-based hybrid waveguides was proposed for the first time, providing a system structure and operating mode. The electro-optic hybrid mode combines the advantages of fast optical operation speed and low power consumption, as well as the advantages of easy storage and operation of the electrical structure.

(2) Through simulation verification, it was found that compared with a multi-bit digital multiplier made of transistors, the SPP technology based on silicon-based hybrid waveguides has the advantages of fast operation speed, low power consumption, and a reduction in occupied area.

(3) The insertion loss of a multi-bit electro-optic hybrid digital multiplier using SPP technology was studied, and the results showed that the insertion loss increased with device size. When the device size exceeded 64 × 64 bits, the maximum insertion loss exceeded 1.0 dB/μm.

2. Background and Related Works

At visible and near-infrared wavelengths, metals have complex dielectric constants. Therefore, the surface plasmon wave field undergoes severe Ohmic attenuation during transmission. Reducing the severe attenuation of the surface plasmon wave field during transmission is one of the biggest challenges in the widespread use of plasma technology. In the compromise between loss and limitation, different plasma waveguide designs, such as metal–insulator–metal [21], metal slot [22], insulator–metal–insulator [23], and channel waveguide [24] designs, cannot achieve satisfactory results. In addition, in recent years, hybrid waveguide schemes have received increasing attention [25,26]. For these structures, the waveguide mechanism consists of a combination of plasma and exponential waveguides. A highly anticipated special structure is the hybrid waveguide, which is composed of a high-refractive-index medium separated from the metal surface by low-refractive-index spacers [27–30]. Experiments have shown that this waveguide can provide a good compromise between confinement and propagation distance [27]. In this paper, the four-layer geometric structure shown in Figure 1 is used for theoretical analysis of the surface plasma of the hybrid waveguide. The wave propagates in the z direction, and the structure is infinite in the x direction. The bottom layer is a metallic material, and the other three layers are lossless dielectrics with positive permittivity: ε_{spacer}, ε_{hi}, and ε_{cover}, assuming that $\varepsilon_{spacer} < \varepsilon_{hi}$.

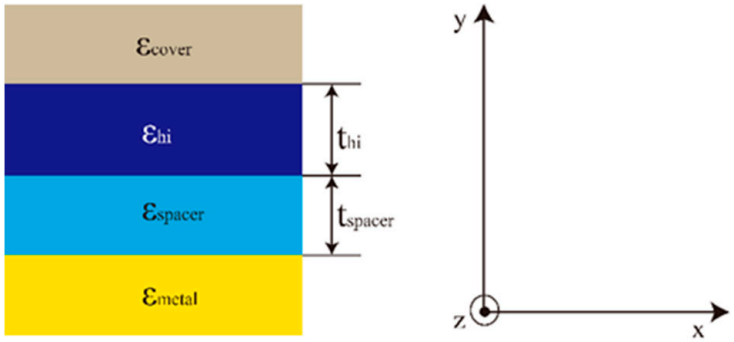

Figure 1. Surface plasma structure model of four-layer geometric hybrid waveguide.

To solve the magnetic field propagation of the structure in Figure 1, the following wave equation of the transverse magnetic field can be used [27]:

$$\nabla_t \times \left(\varepsilon_{ri}^{-1}\nabla_t \times \boldsymbol{H}_t\right) - \nabla_t\left(\mu_t^{-1}\nabla_t \times \boldsymbol{H}_t\right) - \left(k_0^2\mu_{ri} - \beta^2\right)\boldsymbol{H}_t = 0 \quad (1)$$

where $\nabla_t = \hat{x}\frac{\partial}{\partial y} + \hat{y}\frac{\partial}{\partial x}$, β is the propagation constant, while ε_{ri} and μ_{ri} are the relative dielectric constant and the transmittance of medium i, respectively, where i can be a metal, isolator, high exponent, or covered region.

Figure 2 shows the normalized magnetic field intensity, electric field intensity, and guide power density of light field propagation in mixed mode and single SPP mode. Since the hybrid mode is essentially TM, both transverse and longitudinal components of the electric field are present, but the transverse Ey component dominates. As shown in Figure 2a,b, the transverse components of the electric field (Ey) and magnetic field (Hx) are highly concentrated in the low exponential interval layer. Figure 2c shows the boot power curve for the hybrid mode. To compare the power limits of hybrid modes with those of a single SPP, the power distribution is shown in Figure 2c. In the case of a single SPP, the propagation distance is the same as that of the mixed mode. It can be seen that compared with a single SPP mode, the mixed mode provides better constraint ability for the same propagation distance, that is, the mixed mode reduces Ohmic attenuation and achieves a longer propagation distance.

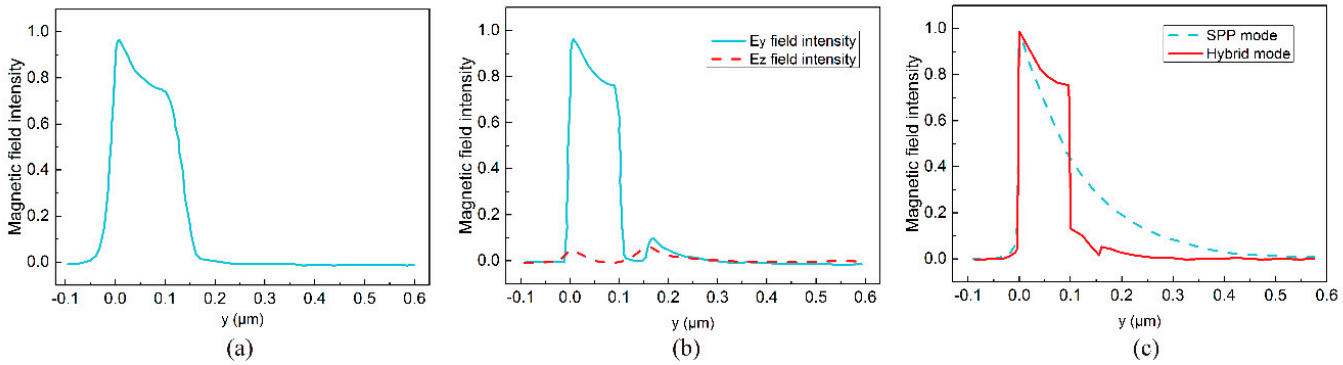

Figure 2. Simulation of optical field transmission in mixed mode and single SPP mode, setting ε_{spacer}, ε_{hi}, and ε_{cover} to 2, 12, and 1, respectively. The thickness values t_{spacer} and t_{hi} are set to 100 nm and 60 nm, respectively. (**a**) Ht electromagnetic field distribution in mixed mode. (**b**) *Ez* and *Ey* component distribution of *Ht* electromagnetic field in mixed mode. (**c**) *Ht* electromagnetic field distribution in mixed mode and single mode.

From the hybrid silicon-based waveguide surface plasmon technology mentioned above, our recent research has proposed electro-optic hybrid half adders and full adders [31,32], as presented in Figures 3 and 4, respectively; Figure 3 shows our proposed model of an

electro-optic hybrid half adder, which has been simulated and analyzed for performance. The electro-optic hybrid half adder and full adder utilize two controlled control units set on a silicon-based waveguide. One type of device, shown in Figure 4a and called an 'optical switch control device', is set in the control area of the silicon waveguide. Another type, shown in Figure 4b and called an 'optical crossover device', consists of three silicon waveguides with a control region set in the middle island waveguide. The control units control the optical path by controlling the effective refractive index change of the SiO_2 interlayer ITO activation material [33]. Under controlled voltage (0 V and 2.35 V), the control units work in two states: 'OFF' or 'ON' and 'CROSS' or 'BAR', respectively. When the 'optical crossover device' under controlled voltage is at 0 V, it works in the BAR state, and when the controlled voltage is 2.35 V, it works in the CROSS state. When the 'optical switch control device' under controlled voltage is 0 V, it works in the 'OFF' state, and when the controlled voltage is 2.35 V, it works in the 'ON' state; the electric field distribution is shown in Figure 5b,c,e,f. In addition, the electrode connection and voltage application mode of the control unit are shown in Figure 4a. The half adder has two types of voltage input control units: x and y. One optical input port and two optical output ports are input, sum, and carry, respectively. The input port is a constant light source input, and sum and carry are logic added sum and carry outputs, respectively. Through voltage control, the electro-optic half adder achieves the logical functions of the electro-optic hybrid half adder in Table 1 and all the dimensions of electro-optic hybrid half adder and full adder structures shown in Table 2. These parameters have been optimized in references [31,32]; the electric field distribution is shown in Figure 6, when the electro-optic hybrid half adder operates in each state.

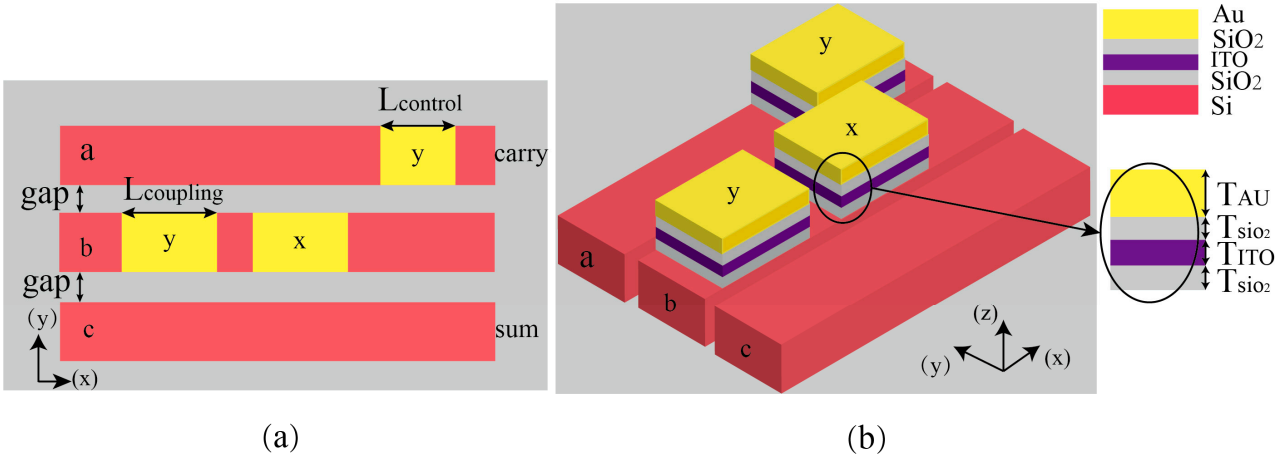

Figure 3. Model of an electro-optic hybrid half adder. (**a**) Top view of the half adder. (**b**) Three-dimensional model of the half adder. It consists of three silicon waveguides (a, b, and c), which are connected in series with two 'optical crossover devices', and an 'optical switch control device' is placed at the end of waveguide 'a'.

We proposed an electro-optic hybrid full adder model in our previous research results and conducted simulation and performance analysis on this model. The control method of the electro-optic hybrid full adder model is the same as the half adder control method mentioned above. Seven control units are set on the silicon waveguide, and the electro-optic hybrid full adder has two types of voltage input control units: x and y. The two optical input ports and two optical output ports are light input, C_{i-1}, light input, sum, and carry, respectively. The input ports C_{i-1} and input are the carry light input and constant light source input, while sum and carry are the logical sum and carry outputs, respectively. Through voltage control, the electro-optic full adder achieves the logical functions of the electro-optic hybrid full adder in Table 3, the electric field distribution is shown in Figure 7, when the electro-optic hybrid half adder operates in each state.

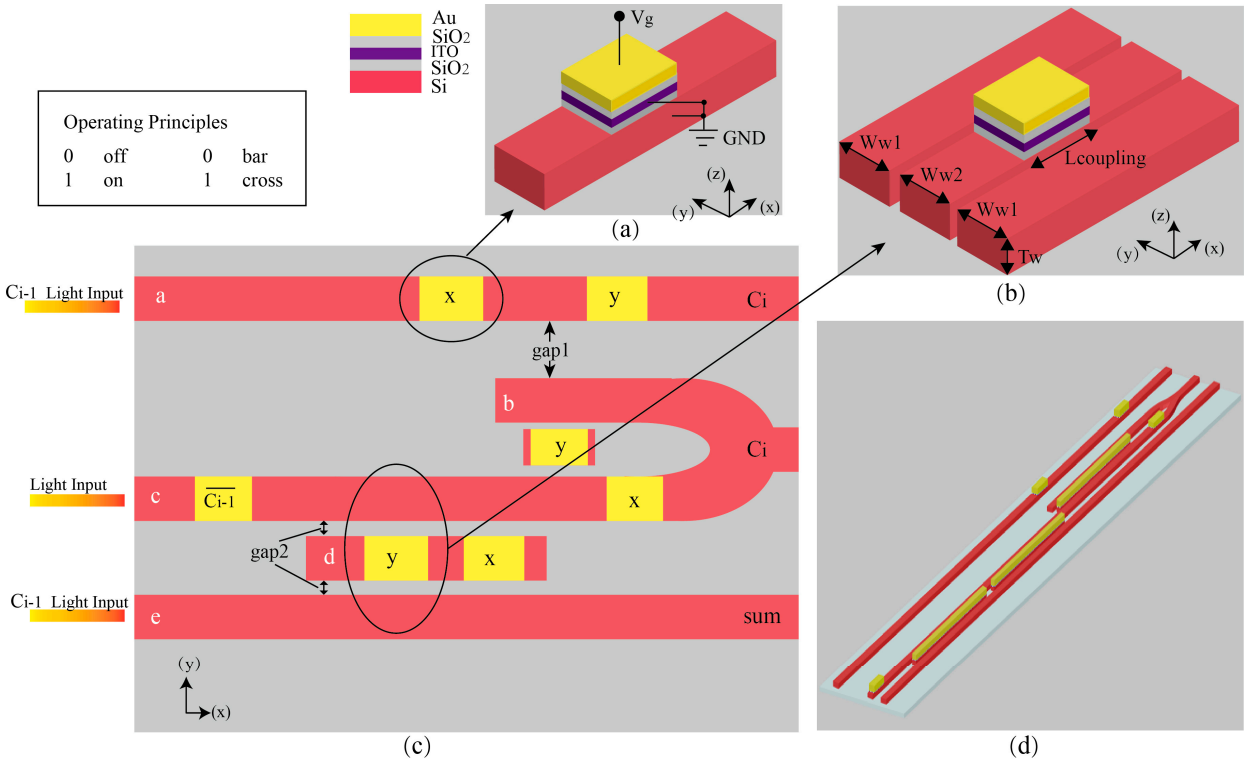

Figure 4. Model of electro-optic hybrid full adder. (**a**) The device called the 'optical switch control device'; the ITO layer and silicon waveguide are defined as negative electrodes, and the AU is defined as the positive electrode. (**b**) The devices called 'optical crossover devices'. (**c**) Top view of electro-optic hybrid full adder; it has five silicon waveguides (a, b, c, d, and e). The values "gap2" in the figure and "gap" in the Table 2 parameters are consistent, but "gap1" must be greater than 800 nm. (**d**) Three-dimensional model of the full adder.

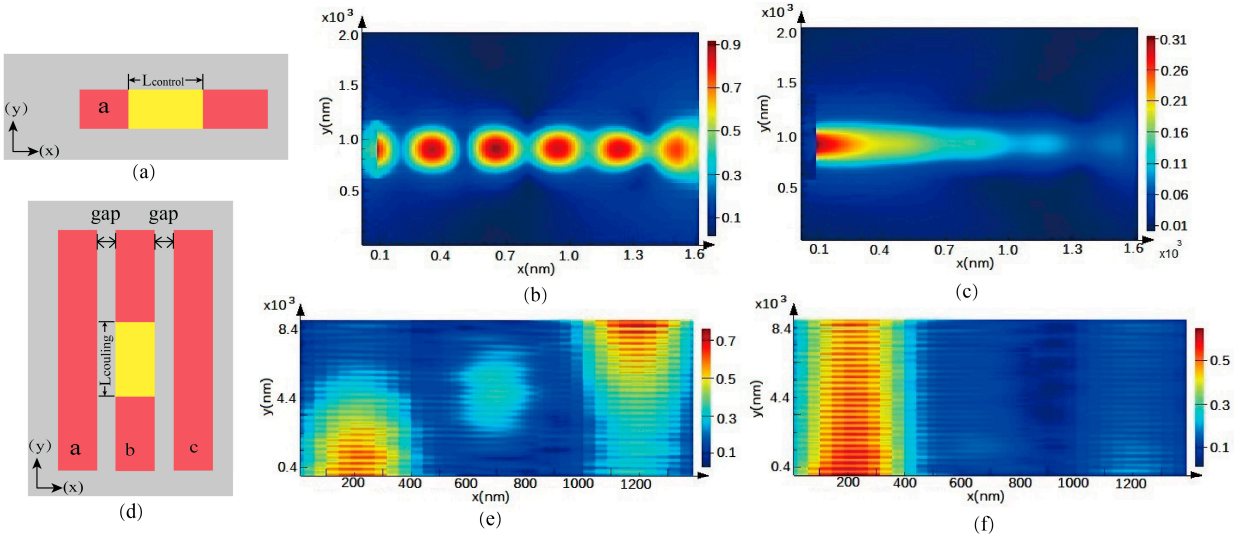

Figure 5. The electro-optic half-adder is separated into single units. (**a**) Straight logic control unit. (**b**) ON state of the straight logic control unit. (**c**) OFF state of the straight logic control unit. (**d**) BAR and CROSS logic control unit. (**e**) CROSS state of BAR and CROSS logic control unit. (**f**) BAR state of BAR and CROSS logic control unit.

Table 1. Truth table of 1-bit half adder function.

Iput		Sum	Carry
x	y		
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Table 2. Dimensions of electro-optic hybrid half adder and full adder structures.

Option	Parameters	Description
gap	140 nm	The optical coupling gap between waveguides
$L_{coupling}$	8700 nm	The optical coupling length between waveguides
$L_{control}$	1350 nm	The optical switch control length
T_{AU}	500 nm	The thickness of AU
$Tsio_2$	14 nm	The thickness of sio_2
T_{ITO}	15 nm	The thickness of ITO
Ww1	400 nm	The width of the side waveguide
Ww2	280 nm	The width of the middle waveguide
Tw	180 nm	The thickness of the waveguide

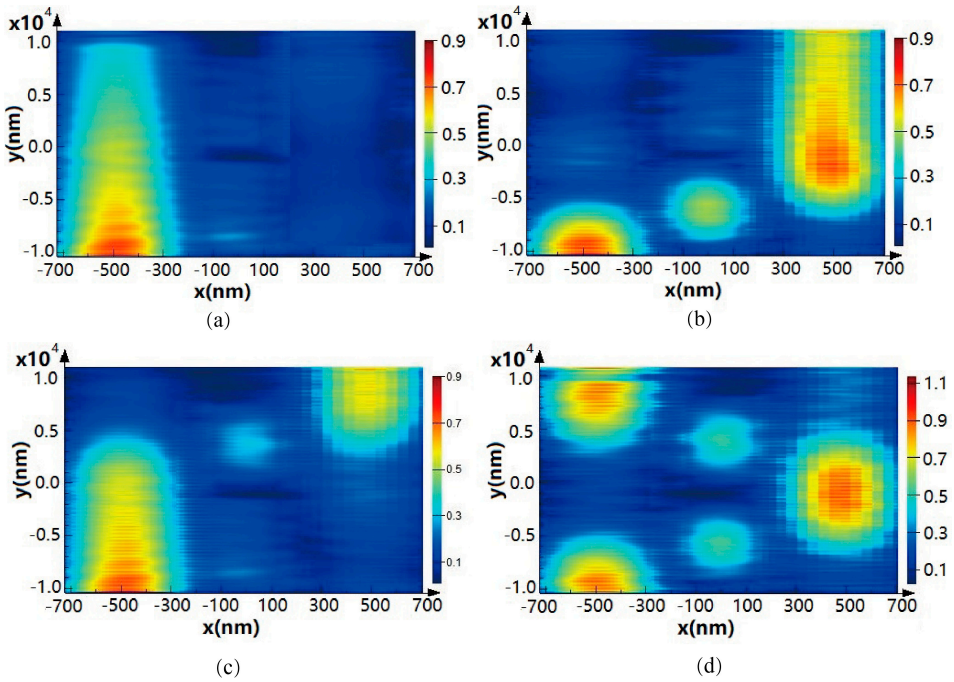

Figure 6. Simulation of the half adder. (**a**) Electromagnetic field distribution with the application of 00. (**b**) Electromagnetic field distribution with the application of 10. (**c**) Electromagnetic field distribution with the application of 01. (**d**) Electromagnetic field distribution with the application of 11.

Table 3. Truth table of 1 bit all adder function.

Input			Output	
C_{i-1}	X	Y	Sum	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1

Table 3. *Cont.*

Input			Output	
C_{i-1}	X	Y	Sum	C_i
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

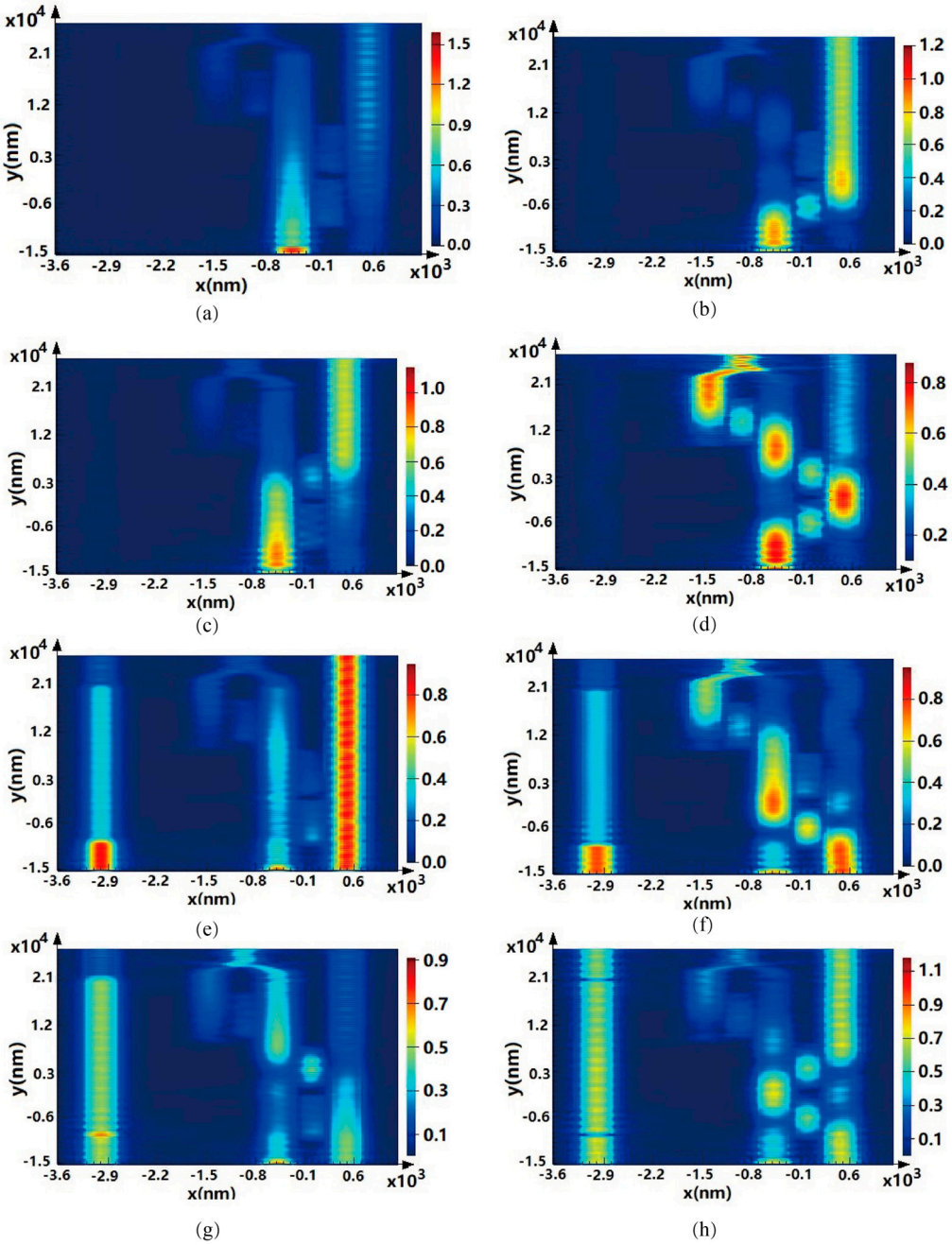

Figure 7. The distribution of electromagnetic fields in the eight operating states of the electro-optic full-adder, (**a**–**h**), in order from 000 to 111.

3. Electro-Optic Hybrid Multidigit Digital Multiplier and Its Operating Method

The designed electro-optic hybrid multidigit digital multiplier consists of the logic AND, half adder, and full adder mentioned above, as shown in Figure 8. It shows the *n*-bit two-stage electro-optic hybrid digital multiplier, with two multipliers $\boldsymbol{a}_{\mathrm{m}}$ and $\boldsymbol{b}_{\mathrm{n}}$ respectively, and the product is $\boldsymbol{Z}_{\mathrm{m+n}}$. In fact, the principle is to shift the binary system of a, then add and add them bit by bit with b, and finally accumulate them bit by bit to obtain the result $\boldsymbol{Z}_{\mathrm{m+n}}$. The above $\boldsymbol{a}_{\mathrm{m}}$ and $\boldsymbol{b}_{\mathrm{n}}$ are both electrical signals, and the logical output is an optical signal. Therefore, the multiplication process requires electro-optical conversion and photoelectric conversion.

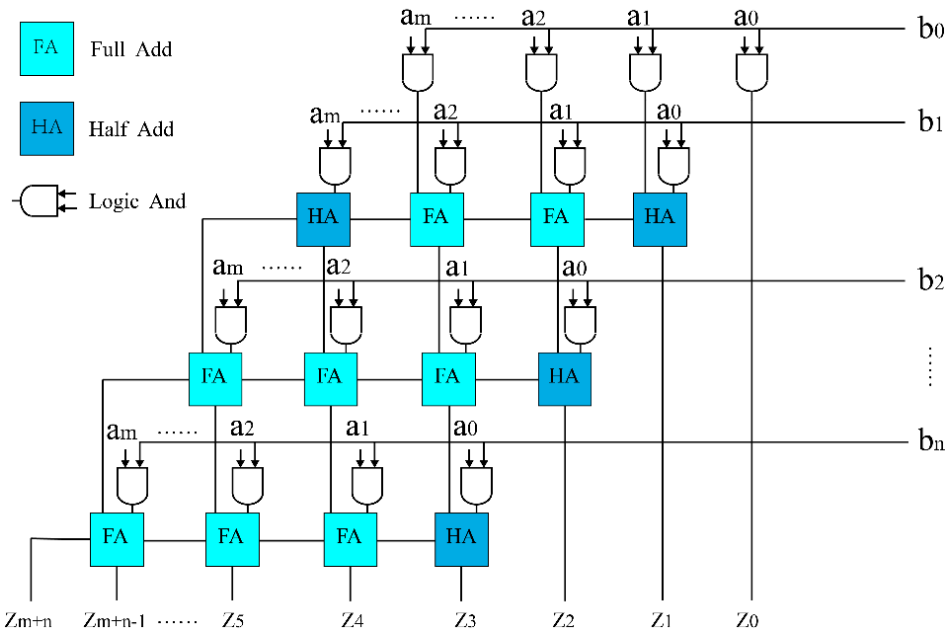

Figure 8. Model of m × n-bit digital multiplier.

Taking a scale of 4 × 4 bits as an example, we can illustrate the operation process of an electro-optic hybrid digital multiplier, as shown in Figure 9. Each electro-optic hybrid half adder and full adder obtains a constant light source input through a light source network. They are connected to each other using internal optical waveguides, and the output of the sum part is cascaded together using electrical connections after OE (optics-to-electronics conversion). The logical AND result of the first row's binary bit b_0 and bits a_0 to a_3 is input to the x-terminal of the first row's electro-optic hybrid half adder and full adder. The AND result of bits a_0 and b_0 is output as Z_0. The logical AND result of the second row's binary bit b_1 and bits a_0 to a_3 is input to the y-terminal of the first row's electro-optic hybrid half adder and full adder. The sum result of the first row's electro-optic hybrid half adder and full adder is output to the x-input terminal of the second row's electro-optic hybrid half adder and full adder after photoelectric conversion. The y input of the electro-optic hybrid half adder and the full adder is the result of the binary b_2 bits of the multiplier and the logical AND of a_0 to a_3, while the sum output of the electro-optic hybrid half adder on the far right is the result of the multiplication. The process continues in the same manner until the third row of the electro-optic hybrid half adder and full adder completes the operation, undergoes photoelectric conversion, and finally outputs Z_3 to Z_7. The 4 × 4-bit electro-optic hybrid multiplier has three rows of electro-optic hybrid half adders and full adders, with four electro-optic hybrid half adders or full adders per row.

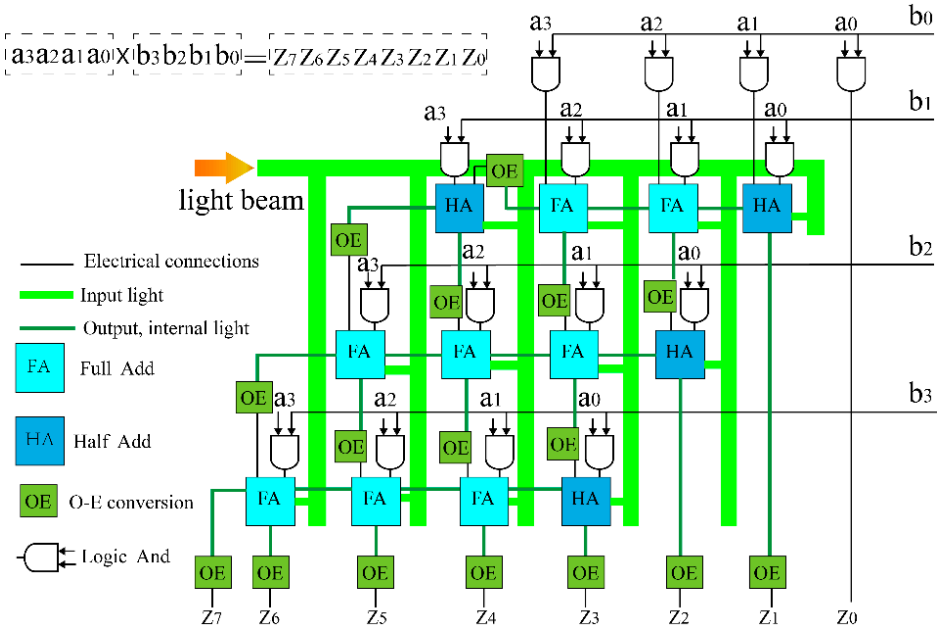

Figure 9. Model of 4 × 4-bit electro-optic hybrid multiplier, The light beam is input from the left silicon waveguide (green) and then reaches each half adder or full adder; the clock circuit is not shown in the diagram.

The operation process of a 4 × 4-bit-scale electro-optic hybrid multiplier is shown in Figure 10. The logical AND operation of the binary bit b_0 and $a_3a_2a_1a_0$ of the multiplier is performed sequentially, resulting in $c_3c_2c_1c_0$. Similarly, b_1 to b_3 repeat the above operation. After each row of AND operation, $d_3d_2d_1d_0$, $e_3e_2e_1e_0$, and $f_3f_2f_1f_0$ are obtained. The result of AND operation needs to be shifted one bit to the left relative to the previous row of AND operation. When all AND operations are completed, they are aligned and accumulated in sequence according to the bit column, and the final result is $Z_7Z_6Z_5Z_4Z_3Z_2Z_1Z_0$.

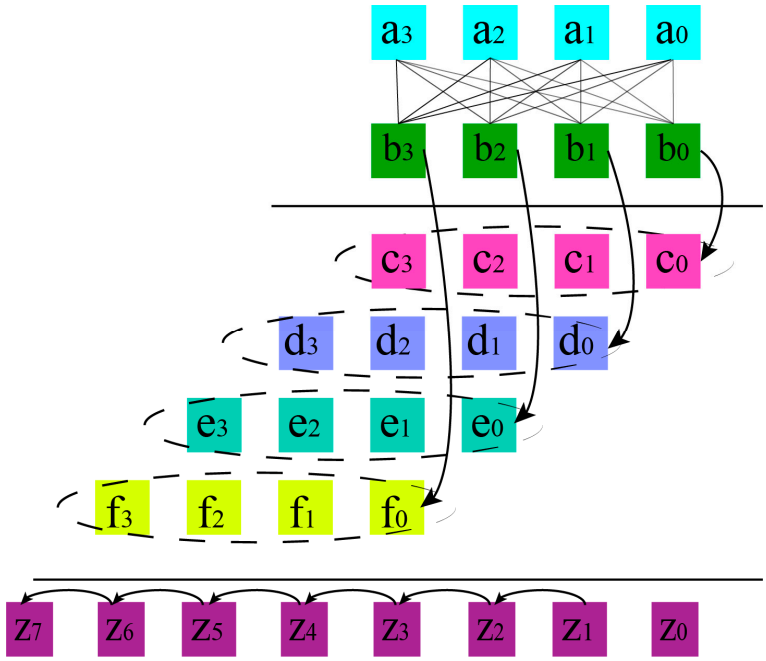

Figure 10. Operation of a 4 × 4-bit electro-optic hybrid multiplier, where $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$ are the multipliers. The bits of the multiplier $b_3b_2b_1b_0$ undergo a logical AND operation with $a_3a_2a_1a_0$ in sequence and are then accumulated. The multiplication result is $Z_7Z_6Z_5Z_4Z_3Z_2Z_1Z_0$.

The operation of the electro-optic hybrid multiplier is carried out according to the clock beat, as shown in Figure 11, which shows the operation timing diagram of the 4 × 4-bit electro-optic hybrid multiplier. Clock is the machine clock, SYNC0 is the frame synchronization head, and SYNC0 triggers the operation of each row of electro-optic hybrid half adder and full adder. Each row of operation of the 4 × 4-bit electro-optic hybrid multiplier requires four machine clock beats, and the operation process is the same as the operation process in Figure 10. Therefore, in order to complete the entire process of the 4 × 4-bit electro-optic hybrid multiplier, four SYNC0 clock triggers are required, and sixteen clock triggers are required. SYNC0 triggers the start of the entire operation, while the departure of SYNC2 marks the completion of the operation and the output of the multiplication result $Z_7Z_6Z_5Z_4Z_3Z_2Z_1Z_0$.

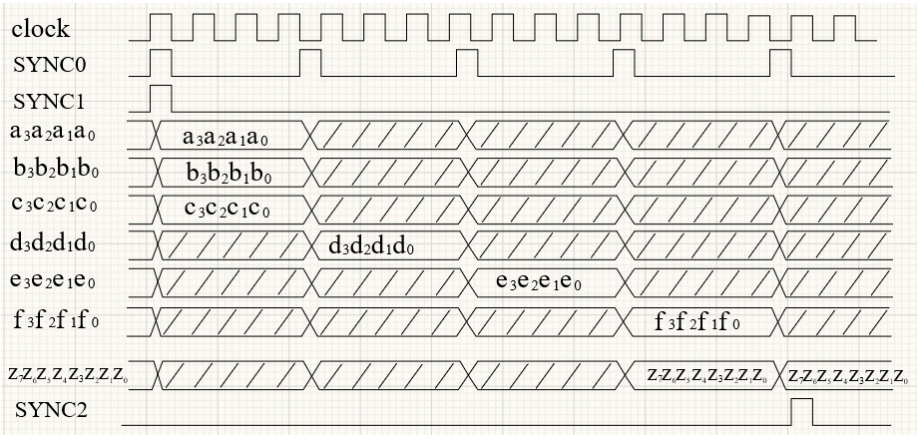

Figure 11. Operation timing diagram of a 4 × 4-bit electro-optic hybrid multiplier, clock is the system clock, SYNC0, SYNC1, and SYNC2 are synchronous clocks, $c_3c_2c_1c_0$, $d_3d_2d_1d_0$, $e_3e_2e_1e_0$, and $f_3f_2f_1f_0$ are intermediate variables.

4. Theoretical Analysis of Performance of Digital Multipliers

4.1. Power Consumption Analysis Methods

The power consumption of a multiplier mainly consists of four parts: electrical logic AND, electro-optical conversion, photoelectric conversion, and optical logic control. Optical logic control is divided into two types: half adder and full adder. The specific equation is described as follows:

$$E_{total} = \sum_{i=1}^{i} E_i + \sum_{j=1}^{j} E_j + \sum_{k=1}^{k} E_k \tag{2}$$

where E_{total} represents the total energy consumed for processing secondary data, while E_i, E_j, E_j, and E_l represent the energy consumed by the electrical logic AND unit, photoelectric conversion, and the optical logic control unit, respectively. The specific calculation methods for the consumed energy are described using the following equations:

$$E_E = \sum_{i=1}^{mn} E_i \tag{3}$$

where E_E represents the total electrical energy consumed by the electrical logic AND units. The number of electrical logic and units depends on the number of digits multiplied by the number of digits, which is $m \times n$.

$$E_{OT} = \sum_{i=1}^{m} E_i + \sum_{j=1}^{(n-1)!-1} E_j \tag{4}$$

where E_{OT} represents the total energy consumed by the optical logic control unit (including the electro-optic hybrid half adder and the full adder), the term before the plus sign

represents the total energy consumed by the electro-optic hybrid half adder, and the term after the plus sign represents the total energy consumed by the electro-optic hybrid full adder. The number of electro-optic control units for a single electro-optic hybrid half adder is three, while the number of electro-optic control units for a single electro-optic hybrid full adder is seven.

$$E_{OE} = \sum_{i=1}^{2(mn-1)} E_i \tag{5}$$

where E_{OE} represents the total energy consumed by photoelectric conversion. The total energy consumed by photoelectric conversion depends on the number of photoelectric converters. For an $m \times n$-bit electro-optic hybrid digital multiplier, the number of photoelectric converters is $2(mn-1)$.

4.2. Speed Analysis Method

The operational speed of a logic unit depends on the response speed of a single logic device and the total number of clock beats. The specific calculation method is described by the following equation:

$$R_{speed} = \left(\sum_{i=1}^{num_e} T_{num_e} + \sum_{j=1}^{num_{eo}} T_{num_{eo}} \right) \tag{6}$$

where R_{speed} is the operating speed of an $m \times n$-bit electro-optic hybrid digital multiplier, divided into two parts. T_{num_e} is the required time for the electrical logic AND unit, while $T_{num_{eo}}$ is the required time for electro-optic conversion. For $m \times n$-bit electro-optic hybrid digital multipliers, $num_e = 2m$, and $num_{eo} = n(m-2)$.

4.3. Device Volume Analysis Method

The volume of the $m \times n$-bit electro-optic hybrid digital multiplier is mainly occupied by the electrical AND logic unit, electro-optic hybrid half adder, and electro-optic hybrid full adder. In this analysis, we temporarily ignore the space occupied by the wiring. The specific calculation method is described by the following equation:

$$S_M = L_m W_n \tag{7}$$

where S_M is the device area of the $m \times n$ bit electro-optic hybrid digital multiplier, L_m is the length of the device, and W_n is the width of the device. The following equations are used to describe each:

$$L_m = (m+n-4)L_{FA} + L_{HA} + L_{EL} \tag{8}$$

$$W_n = (n-1)W_{FA} + (n-1)W_{OE} + 2W_{EL} \tag{9}$$

where, for ease of calculation, the units of both length and width are calculated based on the largest unit. L_{FA}, L_{HA}, and L_{EL} are the lengths of the electro-optic hybrid full adder, electro-optic hybrid half adder, and electrical AND logic unit, respectively, while W_{FA}, W_{OE}, and $2W_{EL}$ are the widths of the electro-optic hybrid full adder, electro-optic hybrid half adder, and electrical AND logic unit, respectively.

4.4. Optical Characteristic Analysis

In the 4×4-bit-scale electro-optic hybrid digital multiplier shown in Figure 5, each electro-optic hybrid half adder or electro-optic hybrid full adder uses an optical network to inject new light sources. Therefore, the insertion loss and extinction ratio of each electro-optic hybrid half adder or electro-optic hybrid full adder have consistent optical characteristics, and their optical performance can be calculated and analyzed according to a single electro-optic hybrid half adder or electro-optic hybrid full adder.

5. Simulation and Performance Analysis

We simulated the electro-optic hybrid digital multiplier through modeling, and the key simulation parameters are set as shown in Table 4. The electrical parameters of the transistor digital multiplier in the table are based on the comprehensive simulation evaluation of the device under the Synopsys company's standard TSMC 28 nm process.

Table 4. Optical simulation parameter configuration.

Option	Parameters	Description
wavelength	1550 nm	Three lowest-order TM modes are spread in the device
E_{Ot}	12.69 fj/bit	Single control unit logic controls the energy consumption of electro-optic conversion
E_{oe}	4.37 fj/bit	The energy consumed by a single photoelectric conversion
E_{e_L}	4.74 fj/bit	Energy consumption of individual electrical logic AND units
E_{e_F}	28.43 fj/bit	The energy consumed by a single electrical full adder
T_{num_e}	0.27 ns	The minimum unit time required for individual electrical logic AND unit operations
$T_{num_{eo}}$	0.00207 ns	The minimum unit time required for electro-optic conversion operation
$T_{num_{oe}}$	0.0021 ns	The minimum unit time required for photoelectric conversion operation
L_{OFA}	41.64 µm	Edge length of electro-optic hybrid full adder
L_{OHA}	21.45 µm	Edge length of electro-optic hybrid half adder
L_{EL}	4.86 µm	Single electrical logic AND unit edge length
L_{EFA}	56.42 µm	Edge length of electrical full adder
W_{OFA}	6.26 µm	Edge width of electro-optic hybrid full adder
W_{OE}	8.65 µm	Edge width of electro-optic hybrid half adder
W_{E_L}	1.8 µm	Single electrical logic AND unit edge width
W_{EF}	8.16 µm	Electrical full adder edge width

The model parameters of the electro-optic hybrid half adder and full adder in Table 3 are from references [31,32], while the other optical model parameters are from reference [34]. The modeling parameters are set according to the parameters in Table 3.

Power consumption is one of the primary indicators for measuring computing devices. Firstly, simulation studies the power consumption of electro-optic hybrid digital multipliers, with simulation scales of 2 × 2 bits, 4 × 4 bits, 6 × 6 bits, 8 × 8 bits, 10 × 10 bits, 12 × 12 bits, 16 × 16 bits, 18 × 18 bits, 20 × 20 bits, 24 × 24 bits, 32 × 32 bits, and 64 × 64 bits, respectively. The simulation results are shown in Figure 12. When the device size does not exceed 32 × 32 bits, the power consumption of the digital multiplier composed of transistors and the electro-optic hybrid digital multiplier is similar, and neither exceeds 30,000 fj/cycle. When the scale is 64 × 64 bits, the power consumption of the electro-optic hybrid digital multiplier is similar. The power consumption of the optical hybrid digital multiplier is 90,995.64 fj/cycle, while the power consumption of the transistor-based digital multiplier is 135,409.32 fj/cycle. The power consumption of the electro-optical hybrid digital multiplier is 59.9% lower than that of the transistor multiplier.

The main reason for the energy-saving of electro-optic hybrid digital multipliers is that the control unit logic controls the energy consumption of electro-optic conversion, and the performance parameters of transistor devices under the 28 nm process are also good. As a digital multiplier composed of electro-optic mixing, when the scale is small, the number of optical devices is relatively small, which cannot reflect the superior energy consumption of optical devices. The larger the scale, the more the superiority of optical device performance can be reflected.

The operating speed of a device is one of the important parameters for measuring computing devices. The same modeling and simulation analysis shows that the size of the device is 2 × 2 bits, 4 × 4 bits, 6 × 6 bits, 8 × 8 bits, 10 × 10 bits, 12 × 12 bits, 16 × 16 bits, 18 × 18 bits, 20 × 20 bits, 24 × 24 bits, 32 × 32 bits, and 64 × 64 bits, respectively. The simulation results are shown in Figure 13. The blue curve represents the time required for a single operation of the electro-optic hybrid digital multiplier, while the black curve represents the time required for a single operation of the transistor digital multiplier. When the device size is less than 10 × 10 bits, the time required for a single operation of the electro-

optic hybrid digital multiplier is almost the same. The time required for a single operation of the electro-optic hybrid digital multiplier does not exceed 10 ns, while the time required for a transistor digital multiplier does not exceed 50 ns. The larger the device size, the more the high-speed performance of the optical device can be reflected. When the device size is 64 × 64 bits, the time required for a single operation of the electro-optic hybrid digital multiplier is 42.77 ns, while the time required for a transistor digital multiplier is 1199.36 ns, which increases the speed by a factor of 28 and has superior absolute performance.

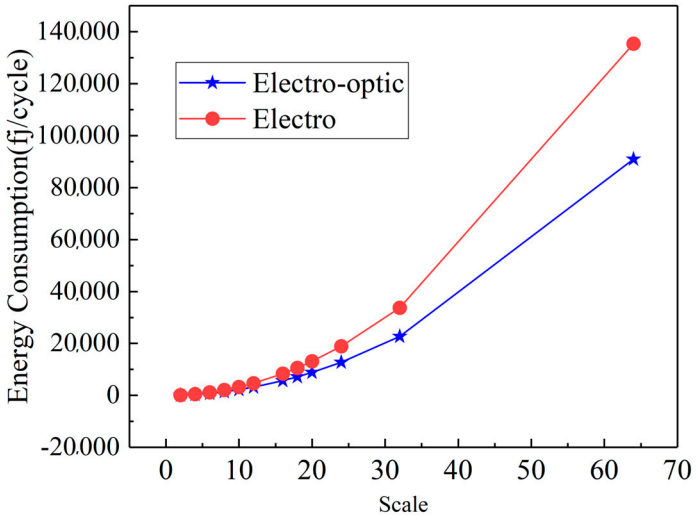

Figure 12. Comparison of energy consumption of digital multipliers. The blue curve represents the energy consumption simulation result of the electro-optic hybrid digital multiplier, and the red curve represents the energy consumption simulation result of the electrical digital multiplier; when the device scale is less than 10, the difference in energy consumption is relatively small.

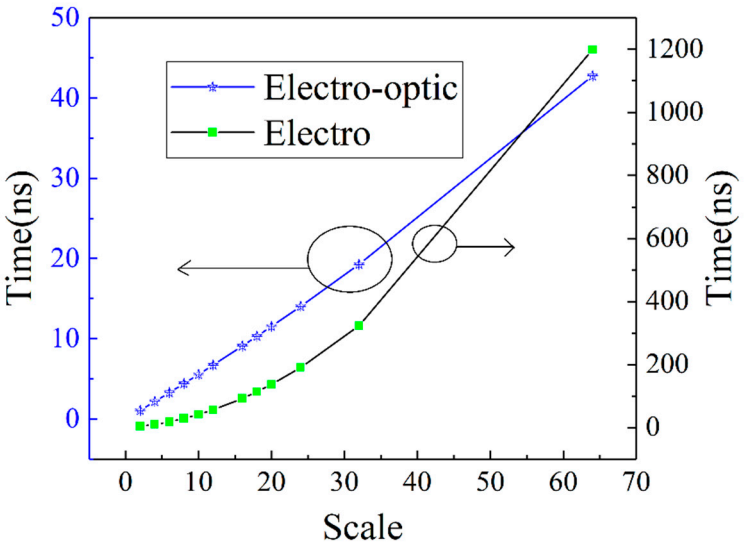

Figure 13. Comparison of operating speeds of digital multipliers. The blue curve represents the speed simulation result of the electro-optic hybrid digital multiplier, and the black curve represents the speed simulation result of the electrical digital multiplier, respectively, at a different scale.

Through research and analysis, it has been found that the junction capacitance of the device in the basic unit of electro-optic mixing is extremely small, and the operation speed of a single control unit has been improved. However, the junction capacitance of the transistor in CMOS technology is relatively large compared to that of the electro-optic

mixing control unit in plasmon polaritons, and the working frequency of the crystal tube in a single device is low. When the device size is small, the number of optical devices is relatively small, meaning that it cannot reflect the superior performance of the high-speed characteristics of optical devices. The larger the scale, the more the superior performance of the high-speed characteristics of optical devices can be reflected.

With the obsolescence of Moore's Law [1], the number of devices that can be integrated on a single chip can no longer grow exponentially over time [2]. Integrating more devices on a single computing chip can increase computing power. As shown in Figure 14, the comparison results show that we have studied and analyzed the volume occupancy of digital multipliers composed of electro-optic mixing and transistors. When the device size is less than 10 × 10 bits, the area occupied by the two is similar. When the device size continues to increase, when the device size is 64 × 64 bits, the volume of electro-optic mixing digital multipliers is larger than that of transistor multipliers, saving 59.9% of the area. Through research and analysis, it has been found that the electro-optic hybrid half adder and full adder use SPP technology, which reduces the size of a single device to a limited extent. The larger the scale of the multiplier, the greater the proportion of electro-optic hybrid devices it contains, and the more area can be saved.

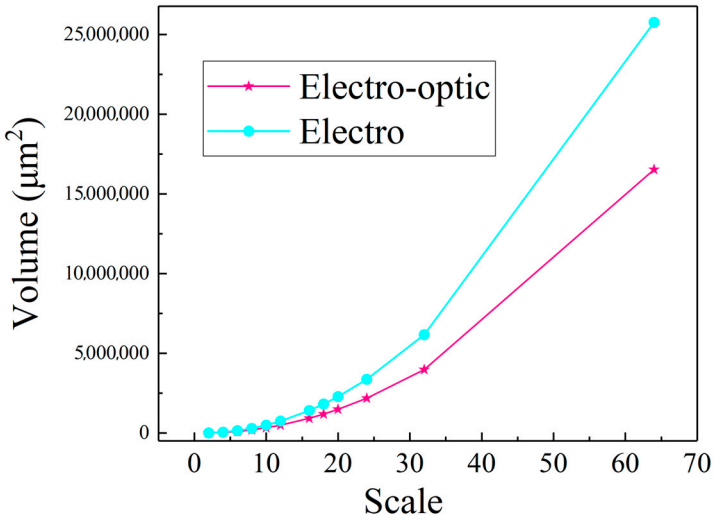

Figure 14. Comparison of volume occupancy of digital multipliers the blue curve represents the volume of the electrical digital multiplier, and the peach curve represents the volume of the electro-optic hybrid digital multiplier, respectively at a different scale.

Insertion loss is an important technical parameter in optical device systems, especially when the cascaded devices cause a sharp increase in insertion loss, resulting in the inability of the entire system to function properly. From the system structure analysis in Figure 4, it can be seen that the optical insertion loss generated by the transmission between the electro-optic hybrid half adder and the electro-optic hybrid full adder only exists in the horizontal direction, while for the vertical transmission, the result of each logical addition or operation undergoes photoelectric conversion. Therefore, in the vertical data transmission process, the maximum optical insertion loss of a single electro-optic hybrid half adder and electro-optic hybrid full adder unit is the maximum optical insertion loss of the multiplier. When studying the optical insertion loss of the multiplier, only the optical insertion loss generated during the horizontal data transmission needs to be studied. The optical insertion loss of a single electro-optic hybrid half adder and an electro-optic hybrid full adder unit can be obtained from references [31,32], and the optical characteristics in the simulation are set to Table 5.

Table 5. Optical parameter settings in simulation.

Device	Input			IL (dB/μm)	
	ci	x	y	Sum	Carry
Half adder	\	0	0	\	\
Half adder	\	0	1	0.0274	\
Half adder	\	1	0	0.0300	\
Half adder	\	1	1	\	0.2052
Full adder	0	0	0	\	\
Full adder	0	0	1	0.37	\
Full adder	0	1	0	0.37	\
Full adder	0	1	1	\	0.30
Full adder	1	0	0	0.44	\
Full adder	1	0	1	\	0.34
Full adder	1	1	0	\	0.39
Full adder	1	1	1	0.31	0.054

When studying the optical insertion loss of an electro-optic hybrid digital multiplier, simulation experiments were conducted with device sizes of 4 × 4 bits, 8 × 8 bits, 16 × 16 bits, and 64 × 64 bits, respectively. However, due to the large quantity of data, only data analysis was conducted for 64 × 64 bits, without data presentation. In order to obtain the maximum insertion loss generated during the operation of the electro-optic hybrid digital multiplier system, it is necessary to ensure that the sum and carry output terminals of each individual electro-optic hybrid half adder and full adder in the system have as much output as possible. Therefore, the inputs for this test are '1111 × 1111', '1111 1111 × 1111 1111', '1111 1111 1111 1111 × 1111 1111 1111 1111', and 'duplicate 1 for 64 times × duplicate 1 for 64 times', respectively. Figure 15, Figure 16, and Figure 17 show the insertion of the sum outputs of each electro-optic half adder and full adder in 4 × 4-bit, 8 × 8-bit, and 16 × 16-bit scale electro-optic hybrid digital multipliers, respectively. From the analysis of experimental results in the graph, it can be seen that the sum output will not increase due to the system size. When the sum has an output, its insertion loss is 0.31 dB, because the result of each logical addition undergoes photoelectric conversion. Therefore, in the vertical data transmission process, the maximum optical insertion loss of a single electro-optic hybrid half adder and electro-optic hybrid full adder unit is the maximum optical insertion loss of the multiplier.

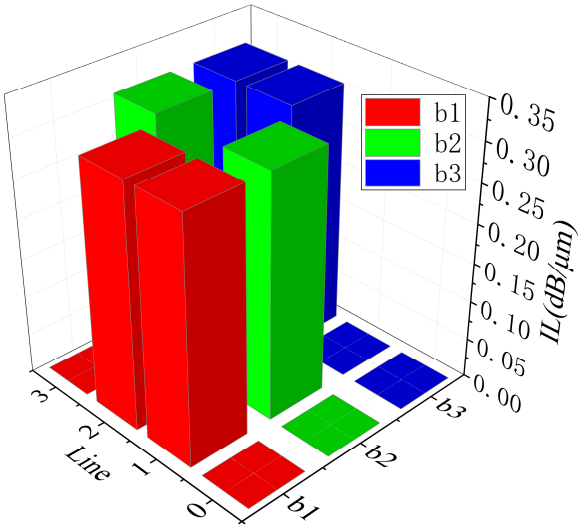

Figure 15. Insertion losses of various sum outputs of a 4 × 4-bit-scale electro-optic hybrid digital multiplier.

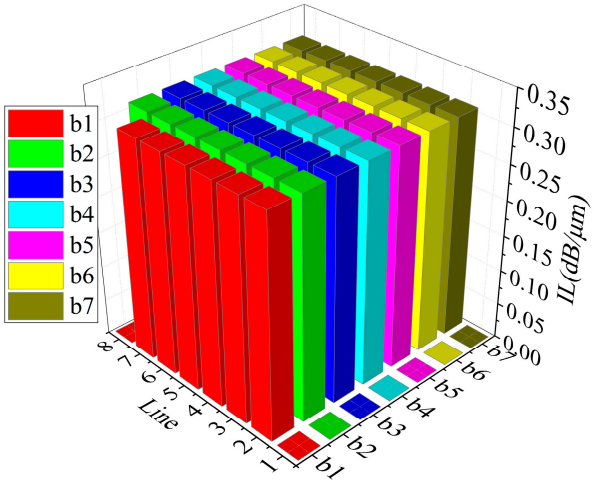

Figure 16. Insertion losses of various sum outputs of an 8 × 8-bit electro-optic hybrid digital multiplier.

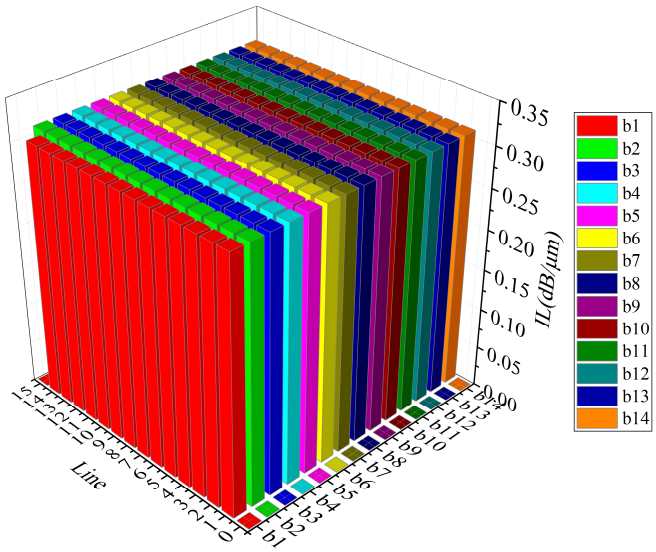

Figure 17. Insertion losses of various sum outputs of a 16 × 16-bit electro-optic hybrid digital multiplier.

From the analysis of the structure of the electro-optic hybrid digital multiplier system, it can be seen that the carry ends of each electro-optic hybrid half adder and full adder in each row of the system are directly connected together through internal optical waveguides, but neighboring rows are electrically connected after photoelectric conversion. Therefore, the carry insertion loss output of each electro-optic hybrid half adder and full adder in the heavy row of the system will be transmitted to the next device.

Figures 18 and 19 show the insertion losses of the carry outputs of each electro-optic half adder and full adder in the electro-optic hybrid digital multipliers with scales of 4 × 4 bits, 8 × 8 bits, and 16 × 16 bits, respectively. From the experimental results, it can be seen that as the device size increases, the carry output insertion losses of each electro-optic half adder and full adder in each row increase sequentially, but the carry output insertion losses of each electro-optic half adder and full adder in the same column do not increase with the device size. From data analysis, it can be seen that when the system size reaches 16 × 16 bits and 64 × 64 bits, the insertion loss will reach 1.03 dB/μm and 1.87 dB/μm, respectively.

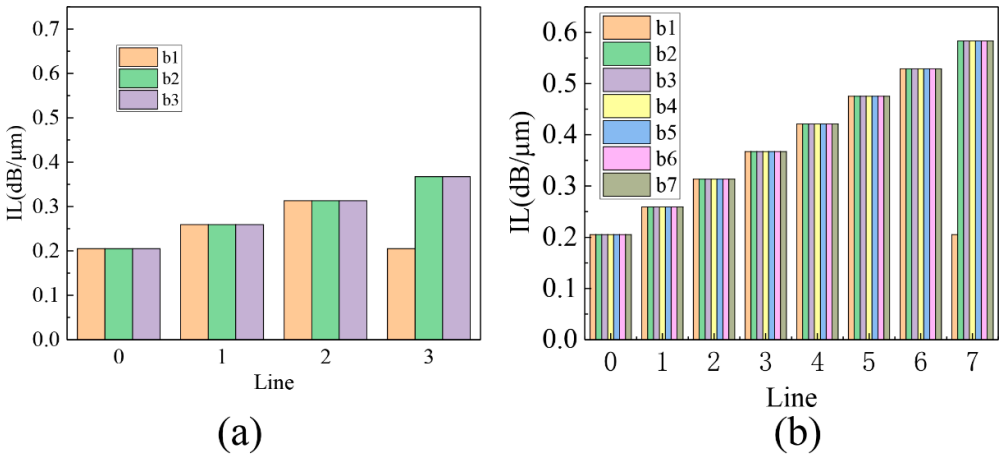

Figure 18. Insertion loss at the carry end output of each electro-optic hybrid half adder and full adder in the electro-optic hybrid digital multiplier. (**a**) Insertion loss at a scale of 8 × 8 bits. (**b**) Insertion loss at a scale of 16 × 16 bits.

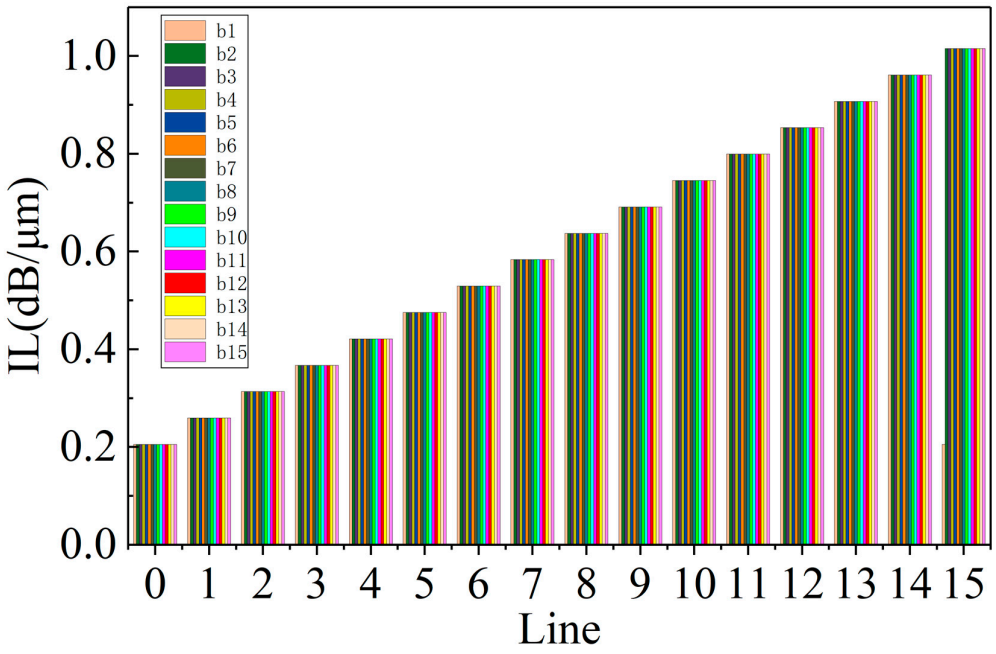

Figure 19. Insertion loss at the carry output of each electro-optic hybrid half adder and full adder when the electro-optic hybrid digital multiplier input is at a scale of 16 × 16 bits.

In addition, in order to maintain generality, we also simulated the carry insertion losses of various electro-optic half adders and full adders at a device size of 16 × 16 bits under other types of data input conditions. The experimental results are recorded in Table 6.

Table 6. Carrier output insertion loss of devices under other data input conditions.

Multiplier1 (Binary)	Multiplier2 (Binary)	Result (Decimalized)	The Maximum IL (dB/μm)
1010101010101010	1010101010101010	1,908,816,100	0.69
1010101010101010	1111111111111111	2,863,224,150	0.74
1111111100000000	1111111100000000	4,261,478,400	0.98
1111111100000000	1111111111111111	4,278,124,800	0.67

From the experimental results data in Table 5, it can be seen that when the input is '111111110000000 × 111111110000000 = 4,261,478,400', the maximum insertion loss is 0.98 dB/μm, which is close to the insertion loss of 1.03 dB/μm when the input data are '111111111111111 × 111111111111111'.

6. Discussion

We have studied the power consumption, volume, and operating speed of an electro-optic hybrid multidigit digital multiplier, as well as the insertion loss of optical characteristics, by creating a simulation platform. When the device scale is less than 4 × 4, the power consumption and volume of the two types of multipliers are not significantly different. The electro-optic hybrid multiplier and electrical multiplier require a maximum of 338 fj/cycle and 495 fj/cycle, respectively, and the volumes of the two types of multipliers are 33,031 μm^2 and 44,466 μm^2, respectively. As the device scale increases, the power consumption and volume of electrical multiplication rapidly increase. Additionally, we compared the designed electro-optical hybrid digital multiplier with an electrical digital multiplier and found that the operating speed of the electro-optical hybrid multidigit digital multiplier far exceeded that of the electrical digital multiplier. In addition, we reviewed and compared literature [35] that proposes an optical implementation of an approximate parallel multiplier; when the scale of the device is 16 × 16, the time required for one operation of the device is 27.136 ns, and the electro-optical hybrid multiplier we proposed requires 9.103 ns, reducing the time by 2/3. In terms of the estimated area, when the scale of the devices proposed by us and in the literature [35] is 16 × 16, they measure 0.9 mm^2 and 0.7 mm^2, respectively.

In the literature [36], there are many extensive explorations and developments in integrated photonics for various material systems, such as silicon (Si), silicon nitride (SiN), lithium niobate (LN), III–V semiconductors, aluminum nitride (AlN), silicon carbide (SiC), and so on. Due to the fact that hybrid silicon-based waveguides surface plasmon polaritons are SPP, silicon-based waveguides are added to vacuum transmission media to reduce severe Ohmic attenuation [27]. Silicon-based photonic devices have the characteristics of being compatible with complementary metal oxide semiconductor (CMOS) processes; therefore, the proposed electro-optical hybrid digital multiplier based on SPP technology can be fabricated using this SOI-platform-compatible CMOS technology for high-performance computing. Our research [31,32] studied the working speed of the control unit and found that the junction capacitance of the control unit is 2.07 fF, which is smaller than the tens of fF (35 fF) mentioned in the reference [37]. This is due to the application of surface plasmon excimer technology, which effectively reduces the area of the junction capacitance and the thickness of the dielectric film, thereby reducing the junction capacitance. At the same time, from our research [31,32], we show that the equivalent resistance of the contact electrode of our device is 200 Ω, which is much larger than the 24 Ω made in practice in the reference. Therefore, according to the current advanced production process, the contact resistance made in practice is smaller than the theoretical value. It is necessary to have higher requirements for the process to ensure that the control of X and Y in the device is synchronized; otherwise, the problem of logic gate competition will occur, resulting in logic errors.

7. Conclusions

In this paper, we designed an electro-optic hybrid multi-bit digital multiplier based on a hybrid silicon-based waveguide using the recently proposed electro-optic hybrid half adder and full adder. The feasibility of the scheme was verified through simulation, and the model parameters of the transistor digital multiplier were obtained based on a comprehensive simulation evaluation of the device using the Synopsys company's standard TSMC 28 nm process. Through simulation and comparative analysis, it was found that the hybrid multi-bit digital multiplier has the advantages of fast operation speed, low power consumption, and a reduction in occupied area compared to a transistor-based multi-bit

digital multiplier. In addition, the optical insertion loss parameters of the electro-optic hybrid multi-bit digital multiplier were analyzed.

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Conflicts of Interest: The authors declare no conflicts of interest.

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