



Communication

Ultra-Broadband and Low-Loss Silicon-Based Power Splitter Based on Subwavelength Grating-Assisted Multimode Interference Structure

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Abstract: High-performance and compact power splitters are fundamental components in on-chip photonic integrated circuits (PICs). We propose a silicon-based power splitter based on a subwavelength grating (SWG)-assisted multimode interference (MMI) structure. To shorten the device size and enhance the device performance, an inverse-tapered SWG is embedded in the central region of the MMI and two rows of uniform SWG are embedded on both sides, together with two right-angled cutting structures on the input side. According to the results, the MMI length was obviously reduced to 3.2 μ m (5.2 μ m for conventional MMI structure under the same waveguide width), while the insertion loss (IL) and reflection loss were 0.08 dB and < -35 dB, respectively. Moreover, the allowable working bandwidth could be extended to 560 nm by keeping IL <0.6 dB, covering the whole optical communication band. On the basis of these features, we believe that such a power splitter is very promising for building on-chip large-scale PICs where power splitting is indispensable.

Keywords: subwavelength grating; multimode interference; power splitter



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1. Introduction

Silicon-on-insulator (SOI), a mature and promising platform for silicon photonics, has been commonly employed to realize compact, high-performance, and high-yield photonic integrated circuits (PICs) [1–5]. To construct such on-chip PICs, power splitters are fundamental and indispensable components, which play a key role in separating the input light power into different output ports [6–10]. For the power splitter, different waveguide structures have been reported, e.g., typical Y-junctions [6], adiabatic tapers [7], directional couplers (DCs) [8], photonic crystals (PCs) [9], and multimode interference (MMI) couplers [10]. With overall consideration of the device size, performance, and fabrication tolerance, MMI couplers are the best choice since Y-branches require a large device size, while DCs and PCs have limited working bandwidths and tight fabrication tolerances, respectively. Therefore, MMI-based power splitters are vital components applied in on-chip Mach–Zehnder interferometer (MZI) modulators [11,12], optical switches [13,14], and other on-chip optical circuits requiring a light power-splitting function [15,16]. Within these application cases, a smaller device size and better device performance have become the new requirements for silicon-based power splitters.

To further shorten the device size of MMI-based power splitters (e.g., typical MMI length of \sim 5.2 μ m under a waveguide width of 2.5 μ m [17,18]), we should enlarge the effective index difference of the transmitted interference modes within the MMI region, which needs to change the refractive index distribution of the conventional MMI structure. Fortunately, a subwavelength grating (SWG) structure whose grating pitch is obviously shorter

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than the grating Bragg period behaves as a homogenous medium without a reflection and diffraction effect for the input light (e.g., $\lambda = 1.55 \,\mu\text{m}$) [19–22]. Furthermore, the effective refractive index of SWG structure can be easily changed by varying its grating duty cycle, offering a new degree of freedom for the device design [19–22]. Therefore, by adding such an SWG structure into the conventional MMI waveguide, the refractive index distribution of the whole structure becomes no longer uniform in the waveguide region, contributing to a reduction in MMI length [19]. Under this condition, various device schemes have been proposed. For instance, through embedding a row of SWGs in the central region of the MMI, the required MMI length was clearly reduced to 3.8 μm (waveguide width 2.2 μm) for power splitting [23]. Meanwhile, a dual polarization operation could also be achieved with the help of the tunability of the effective refractive index for an SWG structure [23]. To further shrink the MMI length, a tapered SWG structure was embedded in the central region of the MMI along the propagation direction, and the MMI length was reduced to only 1.92 µm (waveguide width 2.0 µm) with an insertion loss (IL) of 0.39 dB, which is quite beneficial for on-chip compact integration [24]. In addition to these schemes, an SWG-based MMI power splitter was shown to be a useful structure, where the MMI region was formed by SWGs with identical or different orientations for the grating component [25]. The corresponding MMI lengths could even be reduced to 3.2 µm (waveguide width 2.8 μm) with a large bandwidth of 400 nm (IL < 1 dB) [25]. However, we should note that the IL and working bandwidth of the power splitter still need to be efficiently reduced and increased, respectively, since the fundamental power splitter will be greatly required and heavily used in current and future on-chip large-scale PICs for splitting light power [26–28].

In this paper, we propose a silicon-based MMI power splitter, where the key MMI region is embedded by an inverse-tapered SWG in the center and two rows of uniform SWG slots on both sides along the propagation direction. The embedded central SWG is employed to change the whole refractive index distribution of the multimode silicon waveguide, which can help enlarge the effective index difference between excited modes and further reduce the MMI length. The embedded bilateral SWG slots are used to increase the coupling efficiency with the output waveguides via mode matching, corresponding to a reduction in power splitting loss. Through these two main techniques applied in the MMI structure for the power splitter, the key MMI length could be reduced to 3.2 μ m (waveguide width 2.5 μ m), while the obtained IL was only 0.08 dB at a wavelength of 1.55 μ m, along with a quite low reflection loss (RL) of <-35 dB. Note that the device working bandwidth could be over 550 nm (covering the whole optical communication band) even under a strict criterion of IL < 0.6 dB. In addition, the fabrication tolerances of the key structural parameters were also analyzed. We hope that the proposed device can find important applications in the field of on-chip PICs.

2. Device Structure and Principle

Figure 1 illustrates the three-dimensional schematic of our proposed SWG-assisted MMI power splitter, which consisted of an inverse-tapered SWG and two rows of uniform SWG slots embedded in the MMI center and on both sides, respectively. For a conventional MMI power splitter, as the input fundamental TE_0 mode is injected into the MMI region from the central port, the new TE_0 and TE_2 mode are excited dominantly within the MMI region, thus leading to a clear mode interference along the propagation direction. Once the accumulated phase difference between these two excited modes (TE_0 and TE_2 mode) is equal to π , a double image of the input TE_0 mode with the same phase can be achieved after mode interference [17]. Finally, using two waveguides to separate and output such a double image, we can realize the function of power splitting. To efficiently shorten the MMI length and reduce the power splitting loss, we embedded an inverse-tapered SWG in the MMI center, where the width of the SWG was linearly tapered from w_{g1} (=200 nm) to w_{gn} in a period number of n, and we embedded two rows of uniform SWG slots (period number N) on both sides of the MMI region, whereby their central positions along the propagation direction were aligned with those of the output waveguides. These embedded

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SWG structures had the same grating pitch and duty cycle of $\Lambda=200$ nm and $a/\Lambda=0.5$, respectively. The gap length between the left side of the inverse-tapered SWG (uniform SWG slot) and the left side of the MMI region was $L_{\rm S}$ ($L_{\rm E}$), shown in the inset of Figure 1. Moreover, the length and width of MMI region were $L_{\rm M}$ and $W_{\rm M}$ (=2.5 µm), respectively. The widths of the central input waveguide and bilateral output waveguides were tapered from w_1 to w_2 in a length of $L_{\rm I}$ and from w_3 to w_4 in a length of $L_{\rm O}$, respectively, where the input and output waveguide widths were the same ($w_1=w_4=500$ nm). In addition, we also introduced two right-angled cutting structures on both sides of the input port of MMI region symmetrically to further enhance the device performance, where the corresponding length and width of the cutting structures were $L_{\rm T}$ and ($W_{\rm M}-w_2$)/2, respectively. The whole device was analyzed and simulated on the basis of a commercial SOI wafer with a 220 nm thick top silicon layer and a 2 µm thick buried oxide layer (SiO₂), while the upper cladding was also SiO₂ with a thickness of 2 µm.

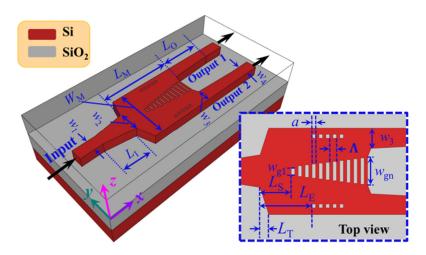


Figure 1. Schematic of our proposed power splitter based on SWG-assisted MMI structure, where an inverse-tapered SWG and two rows of uniform SWG slots were embedded in the center and on both sides of the MMI waveguide respectively. The inset shows the top view of the key MMI region in detail. The material and structural parameters are also labeled.

Figure 2a shows the calculated effective indices $n_{\rm eff}$ of guided modes under different waveguide widths, where the TE polarization modes were analyzed. From this figure, we can easily find the effective index of every supported mode for the waveguide width. For example, the silicon waveguide could support seven modes (from TE₀ to TE₆) when the waveguide width was 2.5 µm. For the multimode waveguide transmission, only even modes (TE₀, TE₂, TE₄, TE₆) could be adequately excited for the central injection from the input single-mode waveguide [17]. Meanwhile, the TE₀ and TE₂ modes of the multimode waveguide would dominate among the excited modes according to our calculations. On the basis of these two modes, we could roughly determine the required multimode waveguide length for the power splitting, where more precise length should be optimized using a numerical method. By adding SWG structures into the conventional MMI waveguide, the effective index difference of dominant excited modes (TE₀ and TE₂ mode) within the MMI region was increased, leading to a reduction in beat length L_{π} [17–19].

$$L_{\pi} = \frac{\lambda}{2(n_{\text{TE}_0} - n_{\text{TE}_2})}, \qquad (1)$$

where n_{TE0} , n_{TE2} are the mode effective indices of the excited TE₀ and TE₂ modes, and λ is the working wavelength. If we set the MMI length L_{M} equal to the beat length L_{π} , we can obtain two TE₀ modes (double image of the input TE₀ mode) with the same phase and same power, corresponding to the power splitting. The SWG structure can be treated

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as a homogeneous medium, and its equivalent refractive index n_{SWG} can be estimated as follows [19]:

 $n_{\text{SWG}} = \frac{a}{\Lambda} \cdot n_{\text{c}}^2 + \frac{\Lambda - a}{\Lambda} \cdot n_{cl}^2, \tag{2}$

where $n_{\rm c}$ and n_{cl} denote the refractive index of the core (silicon) and cladding (silica) of the grating, respectively. Using Equation (2), we can roughly obtain the equivalent refractive index of the SWG structure. Figure 2b shows the calculated effective indices $n_{\rm eff}$ of guided modes for the multimode waveguide ($W_{\rm M}=2.5~\mu{\rm m}$) embedded with the central SWG structure as a function of the SWG width $w_{\rm g}$. Note that the effective index difference between dominant excited TE₀ and TE₂ modes is really increased with the increase in embedded SWG width $w_{\rm g}$. This is the reason that the required MMI length can be reduced compared with the conventional MMI structure. In the analyses below, we study the embedded SWG structures in detail to achieve larger bandwidth and lower loss compared with previous reports [23–25].

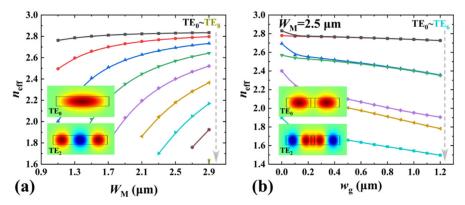


Figure 2. (a) Effective indices $n_{\rm eff}$ of guided modes as a function of the waveguide width for the TE polarization state. Insets show the electric field distributions of TE₀ and TE₂ modes. (b) Effective indices $n_{\rm eff}$ of guided modes for the multimode waveguide embedded with the central SWG structure as a function of the SWG width $w_{\rm g}$. The multimode waveguide width was chosen as $W_{\rm M}=2.5~\mu{\rm m}$. Insets show the electric field distributions of TE₀ and TE₂ modes.

3. Results and Discussion

For the device performance analyses, the three-dimensional finite-difference timedomain (3D-FDTD) method was employed to help design and optimize the device parameters [29,30]. Figure 3 shows the device transmission of several typical silicon-based MMI power splitters as a function of the MMI length L_{M} under the same MMI width $(W_{\rm M}=2.5~\mu{\rm m})$. As shown in Figure 3, three types of MMI power splitter were considered, conventional MMI structure, uniform SWG embedded MMI structure, and inverse-tapered SWG embedded MMI structure. One can clearly find that the variation of device transmission became small within the calculation range of $L_{\rm M}$ when the MMI region was embedded with a uniform or inverse-tapered SWG structure, corresponding to an increased MMI length tolerance. Moreover, we can also observe that the optimum MMI length was obviously decreased from 5.0 μm to 3.6 μm (3.3 μm) due to the embedded uniform (inversetapered) SWG structure in the center of the MMI region along the propagation direction, contributing to on-chip compact integration. If we further added linearly tapered structures connecting the input/output waveguides with the MMI region, the device transmission could be obviously increased, while the variation range of transmission could be reduced, as shown in Figure 3. By comparison, we can find that the inverse-tapered SWG embedded MMI structure with input and output tapers obtained the best power splitting function together with largest tolerance for MMI length $L_{\rm M}$, where the device transmission was about -0.25 dB at $L_{\rm M}$ = 3.3 μ m.

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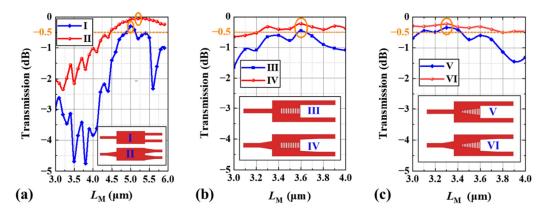


Figure 3. Transmission of several typical silicon-based MMI power splitters as a function of their respective MMI lengths $L_{\rm M}$. (a) I and II represent the conventional MMI structure without and with input/output tapers, respectively. (b) III and IV represent the MMI structure embedded with a uniform SWG waveguide without and with input/output tapers, respectively. (c) V and VI represent the MMI structure embedded with an inverse-tapered SWG waveguide without and with input/output tapers, respectively.

To perform a more detailed analysis of the inverse-tapered SWG structure, the embedded SWG parameters were defined as follows:

$$n = \frac{L_{\rm M} - L_{\rm S}}{\wedge} \,, \tag{3}$$

$$w_{\rm gn} = w_{\rm g1} + k(n-1)$$
, (4)

where *k* is the width increment of the inverse-tapered SWG along the *y*-direction; *k* was chosen as 50 nm during structural optimization. More details about the choice of k can be found in the tolerance analyses described later. Therefore, L_{M} , L_{S} , and n are closely related. Figure 4a shows the detailed device transmission with MMI length $L_{\rm M}$, where the optimal half period number m (n = m/2) of the SWG structure under different $L_{\rm M}$ is also plotted. From Figure 4, we can find that the device transmission was higher than -0.5 dB within the whole range from $L_{\rm M} = 2.6$ to $4.0~\mu m$, and the optimal period number almost increased with the increase in $L_{\rm M}$. Note that the device transmission reached a high value with relatively small fluctuation when $L_{\rm M}$ varied from 3.2 μ m to 3.5 μ m, marked by the oval in Figure 4a. By consideration of the device size and required grating number, we set $L_{\rm M}$ to 3.2 µm for the subsequent analysis, where the optimal half period number m was 18 (n = 9). Figure 4b shows the device transmission with gap length L_S between the left side of the inverse-tapered SWG and the left side of the MMI region, where $L_{\rm M}$ was equal to 3.2 μm . According to Equation (2), the period number of the embedded SWG structure decreased as the gap length $L_{\rm S}$ increased within the calculation range shown in Figure 4b. Meanwhile, the obtained transmission curve presented a nearly flat top as L_S changed from 1.1 to 1.4 μ m, and we chose $L_S = 1.4 \mu$ m, corresponding to the highest transmission shown in Figure 4b.

According to above analyses, the best device transmission of the MMI power splitter embedded with the inverse-tapered SWG was limited to about -0.25 dB at the wavelength of 1.55 μ m. To further enhance the device transmission or reduce the power splitting loss, we embedded two rows of uniform SWG on both sides of the MMI region, where the period number was N. Such embedded uniform SWG structures were employed to match the separated modes (double image of the input TE₀ mode) within the MMI region with the output waveguide modes. Therefore, we set the central positions of embedded uniform SWGs along the propagation direction aligned with those of the output waveguides. Thus, the period number N and relative position $L_{\rm E}$ of such a uniform SWG was also determined. Figure 5 illustrates the device transmission as a function of $L_{\rm S}$, where the optimal period

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number N and relative position $L_{\rm E}$ of the embedded uniform SWG are plotted for every gap length L_S . The grating parameters of the added uniform SWG were the same as those of the inverse-tapered SWG (grating pitch $\Lambda = 200$ nm, duty cycle $a/\Lambda = 0.5$), and the etching width of the uniform SWG in the y-direction was set as 100 nm, corresponding to the square etching slots. As shown in Figure 5, the optimal value of L_S was reduced compared with no embedded uniform SWG structure shown in Figure 5b. The reason is that the embedded uniform SWG could reduce the effective index on both sides of the MMI waveguide, and such a structure also required a further reduction in the effective index on the central side, leading to a reduction in L_S or an increase in period number n of the inverse-tapered SWG. Therefore, L_S decreased from 1.4 to 0.9 μ m, corresponding to the optimal values of N = 5 and $L_{\rm E} = 1.45 \,\mu{\rm m}$. For the device transmission of our proposed power splitter, its value was obviously reduced to -0.08 dB at a wavelength of 1.55 μ m upon embedding the extra uniform SWG structures on both sides of the MMI region. Such a low transmission loss of the power splitter would be very beneficial to construct on-chip photonic devices (e.g., MZI modulators [11,12] and optical switches [13,14]) and large-scale PICs. During the calculation process shown in Figure 5, the choice of optimal values of N and L_E for every gap length L_S was also important. Here, we used $L_S = 0.9 \mu m$ as an example, and the results are plotted in Figure 6, where the period number of the embedded uniform SWG was set as N = 4, 5, and 6. Note that the obtained device transmissions revealed some fluctuations as the relative position $L_{\rm E}$ increased from 0.85 to 2.15 μ m, and the largest transmission loss was almost lower than 0.5 dB, as shown in Figure 6. These transmission fluctuations may have resulted from the interaction of the separated modes with the uniform SWG structure embedded on both sides of the multimode waveguide, where different interact positions led to different transmission losses due to the wave features of input light. In addition, we also introduced two right-angled cutting structures on both sides of the input MMI side in a symmetric manner ($L_T = 0.25 \mu m$) to further reduce the device reflection loss (RL < -35 dB) and stabilize the light evolution through the proposed device. Therefore, through these structural designs and optimizations applied in the MMI region for power splitting, the device transmission loss was reduced to only 0.08 dB, while the required MMI length was $3.2 \mu m$, representing an improvement compared to the conventional MMI power splitter without an embedded SWG structure.

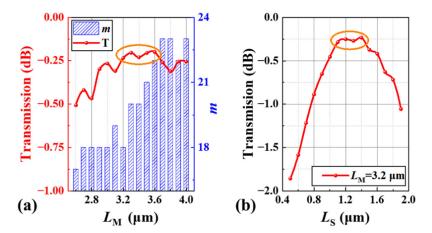


Figure 4. (a) Device transmission with MMI length $L_{\rm M}$ and optimal half period number m of the embedded SWG structure in the power splitter. SWG period number n=m/2. (b) Device transmission with the gap length $L_{\rm S}$, where $L_{\rm M}=3.2~\mu{\rm m}$. The marked regions represent the recommended structural parameter ranges.

Next, we conduct wavelength spectrum analyses for the proposed device, where IL is used to denote the device transmission loss. Figure 7 shows the wavelength dependence of IL for the proposed device and conventional MMI power splitter, where the inset shows the device schematics, and key parameters are also marked. For a better comparison, we

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chose quite a large wavelength range calculated from 1.15 to 1.95 µm, and the MMI width was set as the same ($W_{\rm M}$ = 2.5 µm) for both devices, where the material dispersions of silicon and silica were also considered [31]. From Figure 7, we can clearly find that the allowable working bandwidth of the conventional MMI power splitter was very large (1360–1770 nm) when keeping IL < 0.6 dB. This is the main reason for the MMI structure's superiority over the DC or PC structure for power splitting [8–10]. By comparison, the allowable working bandwidth of our proposed power splitter could be extended from 1240 nm to 1800 nm covering the whole optical communication band if IL < 0.6 dB was also satisfied. Therefore, the obtained working bandwidth (560 nm) of the power splitter based on our proposed structure could be even higher than that of the commonly used broadband MMI power splitter (410 nm), revealing the ultra-broadband feature of our proposed device. Table 1 compares our proposed power splitter with other MMI power splitters embedded with an SWG structure reported recently, where the MMI dimension, IL, RL, and allowable working bandwidth were all considered. It can be noted that the proposed power splitter had obvious advantages of ultra-broadband, low IL, and low RL, while the required MMI dimension was comparable with other reports. Therefore, the present device can be employed as an efficient and broadband power splitting component applied in on-chip PICs.

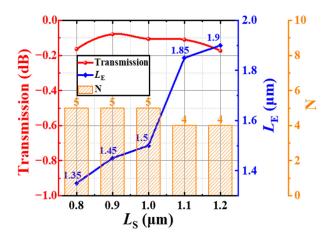


Figure 5. Device transmission of the new designed power splitter as a function of its gap length L_S , where the optimal period number N and relative position L_E of the embedded uniform SWG are also plotted for every gap length L_S .

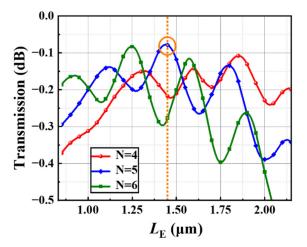


Figure 6. Device transmission of the new designed device as a function of its period number N and relative position L_E of the embedded uniform SWG. L_S is set as 0.9 μ m.

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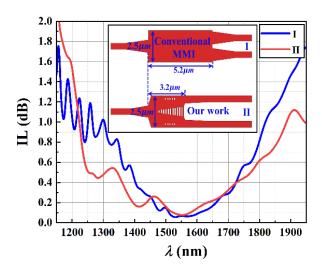


Figure 7. Wavelength dependence of IL for the conventional MMI power splitter (I) and the proposed device (II). The inset shows the corresponding device schematics.

Table 1. Device comparison of typical MMI power splitters embedded with SWG structure.

Reference	Dimension of MMI Region (µm²)	IL (dB) @ 1550 nm	RL (dB) @ 1550 nm	Bandwidth (nm)
[23]	2.2×3.8	0.07	-28.29	280 (IL < 0.3 dB)
[24]	2.0×1.92	0.39	-30.51	~105 (PDL < 0.1 dB) *
[25] **	2.8×3.2	0.20	-	420 (IL < 1.0 dB)
This work	2.5×3.2	0.08	-35.61	560 (IL < 0.6 dB)

^{*} PDL, polarization-dependent loss. ** Experimental results. "-": not mentioned.

For the device fabrication, we only needed one-step lithography and etching processes on a commercial SOI wafer with 220 nm-thick top silicon layer, since the proposed device had a uniform etching depth (220 nm). Moreover, the required minimum linewidth was 100 nm, which can be easily achieved by current E-beam lithography [1,32]. Within our proposed device, the most important structures were the inverse-tapered SWG embedded in the MMI center and the two rows of uniform SWG embedded on both sides of the MMI region. Here, we mainly considered the device performance affected by the lateral shift of the embedded SWG structure in the *y*-direction with respect to the MMI waveguide, and the results are shown in Figure 8, where $\Delta w_{\rm S}$ and $\Delta w_{\rm E}$ represent the lateral shift (*y*-direction) of the inverse-tapered SWG and uniform SWG from their designated positions mentioned above. Moreover, we introduce a new index called the splitting ratio (SR) to characterize the ratio of light power received at output ports due to structural parameter deviations,

$$SR = \frac{P_{\text{Output2}}}{P_{\text{Output1}}}, (5)$$

where $P_{\text{Output}1}$ and $P_{\text{Output}2}$ are the receiving power at the two output ports illustrated in Figure 1. Considering the structural symmetry of our proposed power splitter, performance variation due to lateral shift of $\Delta w_{\rm S}$ was only calculated on one side (positive *y*-direction, $\Delta w_{\rm S} > 0$), as shown in Figure 8a,b, and the results due to a shift on the other side (negative *y*-direction, $\Delta w_{\rm S} < 0$) were the same. To keep SR higher than 0.9, $\Delta w_{\rm S}$ should be controlled within the interval [-30 nm, 30 nm]. Moreover, for the two rows of uniform SWGs embedded on both sides of the MMI region, we considered one row shifting from its optimal position due to fabrication imperfections, while the other row's effect on device performance was considered identical due to structural symmetry. As shown in Figure 8c,d, the available variation of $\Delta w_{\rm E}$ was within the interval [-140 nm, 200 nm] when keeping SR > 0.9. By comparison, the central SWG structure had a tighter tolerance range with

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regard to device fabrication because such a structure had a strong influence on the mode splitting in the MMI region. Thus, the variation range of SR for the central inverse-tapered SWG shift was larger than that for the bilateral uniform SWG shift. Under such conditions, we further analyzed the effect of the central inverse-tapered SWG shift on the power ratio between the two output ports, as shown in Figure 8e. Note that we could achieve a change in power ratio from nearly 30:70 to 70:30 by only shifting the central inverse-tapered SWG structure relative to the silicon waveguide along the y-direction. Such a characteristic would introduce new applications for the power splitter. We also analyzed the effect of the width increment k of the inverse-tapered SWG on the device performance, as shown in Figure 9a. As shown in this figure, the highest IL was lower than 0.3 dB within the whole calculation range from k = 20 nm to k = 100 nm, and the optimum value of k was located at the position of k = 40 nm or k = 50 nm. This is why we chose k as 50 nm in the previous analyses. Figure 9b shows the effect of grating size variation on device performance (IL). Here, we considered the grating width variation along both x- and ydirections. For example, a grating size of 100% corresponded to the optimum widths along the x- and y-directions, while a grating size of 120% corresponded to a width increment of 20% relative to the optimum widths along the x- and y-directions. According to the results, the available grating width variation range should be controlled within the range of 53% to 135% relative to the optimum values by keeping IL < 0.3 dB, where 53% indicates a grating width decrement of 47% relative to the optimum width. Such a relatively large width variation range is beneficial for device fabrication. Therefore, these obtained tolerance ranges of the key embedded SWG structures in the MMI region need to be guaranteed during practical device fabrication [32].

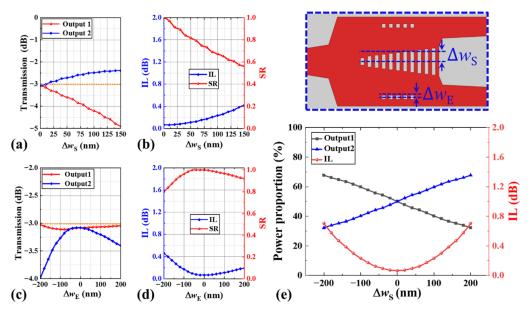


Figure 8. Fabrication tolerance analyses. Device performance (transmission, IL, and SR) variation due to (\mathbf{a} , \mathbf{b}) lateral shift (positive y-direction) $\Delta w_{\rm S}$ of inverse-tapered SWG structure, and (\mathbf{c} , \mathbf{d}) lateral shift (y-direction) $\Delta w_{\rm E}$ of one row of uniform SWG structures embedded in the MMI region. (\mathbf{e}) Power proportion between the two output ports and the obtained device IL as a function of the lateral shift $\Delta w_{\rm S}$ of the inverse-tapered SWG structure. The inset shows the device schematic.

On the basis of the abovementioned device design and optimization processes, the final device parameters were as follows: $w_1=w_4=0.5~\mu\text{m}$, $w_2=0.94~\mu\text{m}$, $w_3=0.6~\mu\text{m}$, $L_{\rm I}=1.38~\mu\text{m}$, $L_{\rm O}=2.0~\mu\text{m}$, $W_{\rm M}=2.5~\mu\text{m}$, $L_{\rm M}=3.2~\mu\text{m}$, $L_{\rm S}=0.9~\mu\text{m}$, $L_{\rm E}=1.45~\mu\text{m}$, $L_{\rm T}=0.25~\mu\text{m}$, m=23, N=5, $w_{\rm g1}=0.2~\mu\text{m}$, and waveguide thickness = 220 nm. Figure 10 plots the electric field evolution through the designed power splitter, where the working wavelength was 1.55 μ m. From Figure 10, we can clearly observe that the input fundamental TE mode could be evenly separated into the two output ports, and the electric

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field evolution was quite stable without any fluctuations or ripples. In comparison to the conventional MMI structure, no clear periodic interference pattern could be observed. The reason is that the embedded SWG region had a lower refractive index compared with the silicon waveguide, and the inverse-tapered shape of the SWG structure broke the period interference behavior in the conventional MMI structure. Furthermore, we can find that its evolution pattern was similar to that of a typical Y splitter. Thus, we cannot find a standard period interference pattern in the SWG assisted MMI region, but its working principle is still based on the MMI effect since the power splitter based on the Y junction nearly cannot be realized in a length of only 3.2 µm. Both a small branch angle and a large conversion length are required for the Y junction-based power splitter. For the proposed power splitter, its total device length is ~6.5 µm when both considering the input and output tapers, while the MMI length is only 3.2 μm. Using such a device, we can efficiently realize the power splitting function with an ultrabroad bandwidth, low insertion loss, and low reflection loss in a compact size, which can be used as the fundamental component for constructing other photonic devices and would be very promising for building on-chip large-scale PICs [26–28].

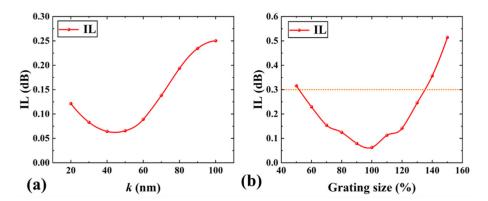


Figure 9. Fabrication tolerance analyses. IL dependence on (**a**) the width increment k of the inverse-tapered SWG for the proposed device and (**b**) the grating size variation. A grating size of 100% corresponds to the optimum widths along the x- and y-directions. A grating size of 120% corresponds to grating width increments relative to the optimum widths along the x- and y-directions. The horizontal line represents IL = 0.3 dB.

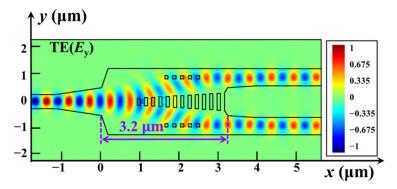


Figure 10. Electrical field evolution of input fundamental TE_0 mode (dominant component: E_y) along the propagation direction through the proposed device, where the MMI length was 3.2 μ m.

4. Conclusions

In summary, by embedding an inverse-tapered SWG and two rows of uniform SWG structures into the conventional MMI waveguide, the input fundamental TE_0 mode could be evenly separated into two output ports, corresponding to a power splitting function. Compared with the conventional MMI power splitter, the added SWG structures could help to shorten the MMI length and enlarge the working bandwidth, as well as reduce

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the insertion loss and reflection loss. According to the results, the required MMI length was reduced to 3.2 μm under a waveguide width of 2.5 μm , while the IL was only 0.08 dB, together with a low reflection loss <–35 dB. Moreover, the device working bandwidth was quite large (>550 nm) while keeping IL < 0.6 dB. Considering its performance and size, the proposed power splitter has obvious advantages compared to previous reports, especially in terms of the working bandwidth and IL. Moreover, the fabrication processes of the proposed device are similar to those of previous reports without introducing extra processing requirements. Therefore, with these advantages, the proposed device could be a good candidate for application in on-chip PICs requiring a power splitting function.

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