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Review

Double Heterojunction Crystalline Silicon Solar Cells: From Doped Silicon to Dopant-Free Passivating Contacts

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Abstract: Carrier-selective passivating contacts for effective electron and hole extraction are crucial to the attainment of high efficiency in crystalline silicon (Si) solar cells. In this comprehensive review, the principle of carrier extraction and recombination mechanisms in conventional industrial Si solar cells are discussed first. Passivating contacts based on (i) amorphous hydrogenated Si and (ii) polysilicon/silicon oxide are next reviewed, with emphasis on carrier selectivity mechanisms including contact layer band alignment with silicon, and localized carrier transport in ultrathin oxides. More recent developments in dopant-free passivating contacts deposited by lower-cost fabrication processes with lower thermal budget are then described. This third category of non-Si based electron- and hole-selective passivating contacts include transition metal oxides, alkali/alkali earth metal fluorides and organic conjugated polymers. The photovoltaic performance of asymmetric double heterojunction Si solar cells fabricated using these non-Si passivating contacts and their stability in damp heat conditions are discussed and compared with Si based passivating contacts.

Keywords: silicon photovoltaics; passivating contacts; carrier selectivity; recombination; heterojunction; transition metal oxides

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1. Introduction

Solar energy is the most abundant and fundamental renewable energy resource for mankind [1]. As a result of thermonuclear fusion of hydrogen, the sun continuously emits a broad spectrum of electromagnetic waves in the ultraviolet (UV), visible and infra-red (IR) spectral range. The solar insolation (intensity) at the top of the Earth's atmosphere is 1.36 kW/m^2 [2]. Due to atmospheric absorption and scattering, this is attenuated to a maximum of 1 kW/m^2 at sea level. In principle, solar energy alone can more than fulfil the electricity demand for the entire planet, which was about 23,300 TWh in 2020 [3]. According to ref. [4], the energy used by the world's population in one year can be delivered in less than 1 h from sunlight. It is critical to increase the renewables component in electricity generation because, in 2020, this sector accounted for 12.3 Gt of CO_2 emission, mainly due to combustion of coal and natural gas [3]. There are two approaches to convert the energy in sunlight: (i) photovoltaics (PV) and (ii) solar thermal. For PV, a semiconductor solar cell is used to convert the visible and UV portion of sunlight directly into direct current (DC) electricity. Solar thermal, on the other hand, uses the IR radiation in sunlight to heat up a working fluid and generate alternating current (AC) electricity with a steam turbine. According to a recent report [5], the total installed PV capacity worldwide reached 760 GW in 2020 with 139 GW added during that year. This contrasts with the corresponding figures of 39 GW and 17 GW respectively for the year 2010. This rapid increase in the installed capacity of PV has resulted in an 85% drop in the levelized cost of electricity from US$ 0.381/kWh in 2010 to US$ 0.057/kWh in 2020 [5]. The cost of PV generated electricity to end users is already competitive with respect to conventional electricity in some countries. This cost parity is an important driver for the transition to a net zero emission energy infrastructure.

The crystalline silicon (c-Si) solar cell is the most important category of PV device for renewable power generation and at present accounts for about 90% of the PV device market [6]. This dominance of c-Si solar cells in terrestrial PV began in the mid-1970s and has continued ever since [7]. Second in importance are the various types of second-generation thin-film solar cells fabricated on large area glass, steel or polymeric substrates. C-Si solar cells are based on Si wafers and can be sub-divided into monocrystalline and multi-crystalline Si solar cells. Monocrystalline Si solar cells are fabricated from single crystal wafers while multi-crystalline Si solar cells are based on pseudo-square-shaped polycrystalline Si wafers with large, randomly oriented, grains [8]. The dominance of c-Si solar cells since the inception of the PV industry is due to its non-toxic nature and its availability. Si is the second most abundant element in the Earth's crust (after oxygen) with a crustal abundance of 28.2% by mass [9]. Furthermore, Si is the semiconductor used for manufacturing microprocessors and memory integrated circuits. A vast body of technical knowledge pertaining to the processing of Si has been built up since the 1950s. The technical knowledge regarding passivation of Si surfaces is especially important to c-Si solar cells [10,11]. Despite recent breakthroughs, there is still a need to increase the certified power conversion efficiency (PCE) of monocrystalline c-Si solar cells from the present 26.7% towards the theoretical Shockley–Queisser limit of 29.4% [12,13]. This is because ~48% of the cost share per Watt peak of a PV module is related to the Si material [14]. Moreover, the current record c-Si PCE mentioned above is for experimental cells only and industrial cells have significantly lower PCE. A higher PCE can reduce the number of c-Si wafers needed for the same output power. Cost reduction in turn can raise the amount of PV electricity from ~3% of electricity generated from all sources in 2020 [3]. Another approach to reduce the cost of c-Si solar cells is to simplify the wafer processing by using alternative thin film materials that can be deposited using solution processing at or near ambient temperature.

This review concerns the latest developments in the double heterojunction (DHJ) c-Si solar cell, also known as the dopant-free asymmetric hetero-contact (DASH) cell. There are two main aims to this article. First, the main carrier selective passivating contact materials for electron and hole extraction from the DASH cell will be surveyed. Second, the device structure, PV performance, stability and limitations of state-of-the-art DASH cells are reviewed and compared with earlier heterojunction c-Si solar cells with doped Si passivating contacts. Unlike prior works [15–17], all three types of passivating contacts are surveyed to provide a more comprehensive review.

2. Diffused Homojunction Carrier Selective Contacts

Figure 1a shows a simplified schematic diagram of an earlier manufactured conventional c-Si solar cell [16]. It precedes the present passivated emitter and rear cell (PERC). The substrate which acts as a light absorber is a p-type Si wafer. The wafer surface region is doped heavily n-type and there is a top passivation and anti-reflection (AR) layer. Both the silver (Ag) and aluminum (Al) contacting electrodes are screen printed. A wafer is used because Si is an indirect band-gap semiconductor, and its absorption coefficient is relatively low (1 cm^{-1} at band-gap energy increasing to 10^4 cm^{-1} at 2.5 eV) [18]. Sunlight incident at the top side of this wafer is either reflected to the ambient or transmitted into the wafer. After absorption in the wafer, each incident photon in sunlight with an energy greater than the bandgap E_g of Si (1.1 eV) is converted into an electron hole pair (EHP). An electron originally in the valence band of Si is excited into the conduction band and leaves behind a free hole in the valence band. For completion of the PV energy conversion process, the photogenerated excess electrons and holes in Si must move by diffusion-drift transport to the respective electrodes where carrier collection takes place. This carrier separation is performed by an internal electric field at a junction [19]. If the carriers reach the respective electrodes (negative for electrons and positive for holes) without recombination, a useful output current can be supplied to a load.

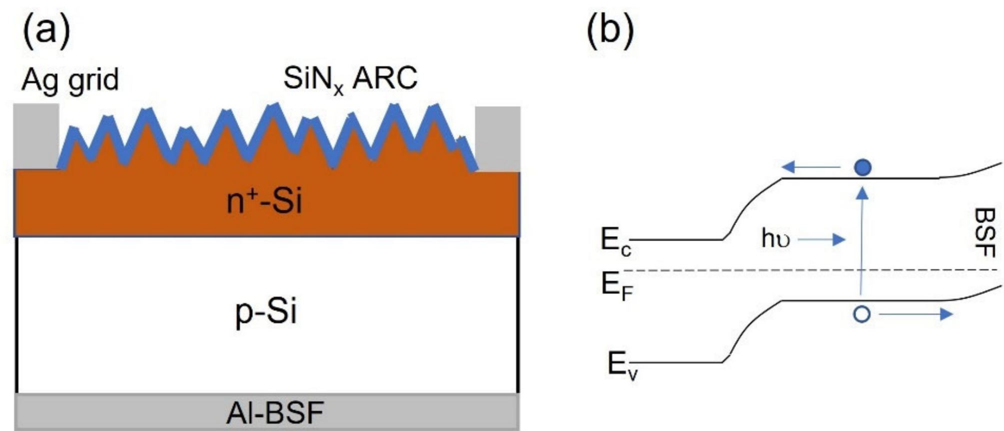

Figure 1. (**a**) Schematic cross-sectional diagram of a p-type Al-BSF c-Si solar cell with surface texturing; (**b**) energy band diagram of p-type Al-BSF solar cell.

In Figure 1a, the contacts are defined as the area of the Si wafer where a screen-printed electrode forms a junction with the c-Si. Since light is incident from the top side of the wafer, the footprint of the top contact needs to be much smaller than the uniform bottom contact to maximize light coupling into the Si (note: this condition does not apply to bifacial cells.) For any c-Si solar cell, the top and bottom contacts, regardless of device structure, must have a carrier selectivity property. This means that for the electron contact at the top of a p-type cell, the electron (minority carrier) conductivity must be high while the hole (majority carrier) conductivity must be low. For the bottom contact, the hole conductivity is high and the electron conductivity low. The carrier selectivity requirement is based on the fundamental principle that, for recombination to occur at the contact region, there must be electrons and holes present [10]. If one type of charge carrier is excluded from the contact region, the other carrier type will have a greater probability of being collected. The selective exclusion of charge carriers from the contact region can be achieved by using an electric field. This field can be in the form of a p-n homojunction or by introducing fixed charges into a dielectric layer deposited on c-Si [10]. In conventional p-type c-Si solar cells, electron selectivity is realized by using high-temperature diffusion of phosphorus (P) to form a heavily n-type (n^+) region at the sub-surface region of the Si wafer [16]. Since this n^+ region forms a n^+-p homojunction in the substrate, the same nomenclature as that for bipolar junction transistors (BJT) is used for this junction, namely emitter for the n^+ diffusion region and base for the p-type substrate [20]. Electron selectivity at the top contact is due to band bending at the lightly doped side of the n^+-p homojunction as shown in the equilibrium energy band diagram of Figure 1b. Once a photogenerated electron reaches the junction, the electric field in the depletion region will facilitate the collection of this electron. On the other hand, any hole moving in the same direction as the electron will encounter an opposing electric field and will not be collected. This results in the asymmetric conductivity mentioned above.

An identical principle is used for the hole-selective contact at the back of the p-type c-Si solar cell. Here, a p^+ diffusion doped region of Al with a graded dopant profile is used to set up a high–low homojunction or back surface field (BSF) to facilitate hole collection [21]. The principle is the same as the graded dopant profile in the base region of a npn BJT where the magnitude of the base electric field is proportional to the local concentration gradient of acceptor dopants in the base [22]. The BSF attracts holes and repels electrons from the sheet contact at the bottom of the wafer. In the cell of Figure 1a, which is sometimes called an Al-BSF cell, the Al is diffused from the screen-printed Al film into c-Si during post metallization annealing. The PCE of a typical manufactured Al-BSF cell is ~20% [16].

Carrier selectivity is a critically important property for the two contacts in Figure 1a because the metal electrode is directly contacting the c-Si. The surface of the c-Si is where the periodicity of the single crystal ends, and this abrupt termination gives rise to many

dangling bonds or localized surface states in the bandgap of Si which is an indirect band gap semiconductor. When both electrons and holes are present near these surface states, Shockley–Read–Hall (SRH) recombination can readily occur and result in a high surface recombination velocity S. For surface recombination within a unit area via a single trap with energy E_t, S can be written as [10]:

$$S = \frac{U_s}{\Delta n_s} \tag{1}$$

Here, U_s is the surface recombination rate with the unit of $cm^{-2}s^{-1}$ and Δn_s is the excess minority carrier concentration at the surface of the semiconductor. The surface recombination rate U_s is given by the SRH theory as [10]:

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s+n_1}{S_{p0}} + \frac{p_s+p_1}{S_{n0}}} \tag{2}$$

where n_s and p_s are the surface concentration of electrons and holes respectively and n_i is the intrinsic carrier concentration. S_{n0} $(= \sigma_n v_{th} N_{st})$ and S_{p0} $(= \sigma_p v_{th} N_{st})$ are respectively the surface recombination velocity parameters for electrons and holes [10]. The quantities σ_n and σ_p are the capture cross sections of electrons and holes respectively; v_{th} is the thermal velocity of the carriers and N_{st} is the number of surface traps per unit area. The carrier concentrations n_1 and p_1 in Equation (2) are given respectively by: $n_1 = n_i \exp((E_t - E_i)/kT)$ and $p_1 = n_i \exp((E_i - E_t)/kT)$, where E_i is the intrinsic Fermi level and kT is the thermal energy.

SRH surface recombination must be minimized because it reduces the number of collected electrons and holes. This carrier loss can cause the short circuit current density J_{sc} and the shunt resistance R_{sh} of the solar cell to decrease. In addition, the reverse saturation current density J_0 is related logarithmically to the open circuit voltage V_{oc} of a c-Si solar cell by the equation [23]:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_0} + 1\right) \tag{3}$$

where n is the ideality factor; k is the Boltzmann constant; T is the absolute temperature, q is the electron charge and J_L is the photocurrent density. Hence, an increased J_0 will result in a smaller V_{oc} causing the PCE to be reduced. When surface states cannot be eliminated, the SRH recombination at the Si surface can be suppressed by ensuring that only the majority carrier is present near the contact. This is because each SRH recombination involves an electron and a hole. When there is a lack of minority carriers, the recombination of electrons and holes at the contact cannot proceed.

Apart from contact recombination, carrier loss can occur through (i) surface recombination and (ii) bulk recombination [24,25]. In Figure 1a, surface recombination at the phosphorus doped emitter surface (excluding the electron-selective contact) can be reduced by using a dielectric passivation layer. The atoms of the passivation form covalent bonds with the Si atoms at the surface and reduces the amount of Si dangling bonds which are the origin of the surface states. In principle, the best passivation layer for c-Si is thermally grown silicon dioxide (SiO_2) formed by oxidizing Si in dry O_2. This is because it can lead to the lowest interface state density in the bandgap of Si [26]. However, high-quality SiO_2/Si interfaces can only be grown at high temperature (~900 °C). Hence, in the PV industry, amorphous non-stoichiometric silicon nitride (SiN_x) deposited by plasma enhanced chemical vapor deposition (PECVD) at much lower temperatures (~350 °C) is used instead for passivating n^+-Si surfaces of p-type Al-BSF solar cells [16]. Since the refractive index of SiN_x can be easily tuned by modifying the deposition conditions, the SiN_x passivation layer also serves as an AR layer [16]. For the targeted AR wavelength, the light reflected from the air-SiN_x interface has a 180° phase shift with respect to the light reflected from the SiN_x-Si

interface, causing destructive interference of light. The AR layer ensures better coupling of sunlight into the c-Si solar cell and improves the light management in the solar cell.

The passivation of boron-doped p^+-Si surfaces for n-type c-Si substrates is by contrast considerably more challenging. Initial attempts to use thermal oxide as passivation layer were not successful due to the loss of passivation with storage time, even for initially well-passivated p^+-Si wafers [27]. The use of PECVD SiN_x as passivation was also found to be unsatisfactory due to the presence of large amounts of positive fixed charge in SiN_x [27]. Eventually, plasma-assisted atomic layer deposited (ALD) non-stoichiometric aluminum oxide (AlO_x) was found to be suitable for passivating p^+-Si [28]. When an AlO_x passivation layer is incorporated into the back side of the p-Si substrate of the cell in Figure 1a and small contact holes are etched before deposition of the metallization layer, the device becomes a PERC cell. In 1989, the first p-type PERC solar cells fabricated by Blakers et al. using float zone (FZ) Si showed a PCE of 22.8% [29]. In addition to the backside passivation by thermal oxide, this cell featured anisotropic wet-etched inverted pyramids and anti-reflection coating on the front side to increase the coupling and trapping of sunlight. PCE is limited in part by the lateral charge transport on the backside because of contact holes. When localized diffusion of p-type dopants through contact holes is performed prior to Al deposition to form small BSF regions, the cell is a passivated emitter rear locally diffused (PERL) cell [30]. A variant of the PERL cell is the passivated emitter rear totally diffused (PERT) cell in which thermal diffusion of p-type dopants is applied to the entire back surface [31]. Note that for the PERC, PERL and PERT cells, there is lateral carrier transport at the back of the wafer due to the use of small contact holes and this can adversely affect the FF. In 1999, Zhao et al. at the University of New South Wales reported a PERL cell fabricated on p-type FZ Si wafer with a measured PCE of 24.7% [31]. Following a revision of the reference solar spectrum by the International Electrotechnical Commission in 2008, the PCE of this device was eventually revised upward to 25.0% in 2009 [32]. This represents a major milestone in the development of c-Si solar cells.

Bulk recombination refers to electron-hole recombination inside the c-Si wafer. This can take place via: (i) direct band to band radiative recombination, (ii) Auger recombination and (iii) SRH recombination [24]. Since Si is an indirect bandgap semiconductor, the direct radiative recombination mechanism is the least likely. Nevertheless, it is important because consideration of this mechanism alone will lead to the theoretical maximum PCE for a single junction c-Si solar cell. In the detailed balance analysis by Shockley and Queisser [25], radiative recombination is considered because the solar cell needs to be in thermal equilibrium with its surroundings. For a bandgap of 1.1 eV, the maximum PCE for a single junction c-Si solar cell is 29.4% [13].

The Auger recombination mechanism also involves the direct band-to-band recombination of an excess electron with a hole [24]. However, unlike radiative recombination, the energy of the excess electron is used to excite another electron or hole in Si. Auger recombination is therefore a three-particle process. The excited third particle (electron or hole) loses its energy by exciting phonons in the Si lattice. As explained in [10], the Auger recombination lifetime $\tau_{Auger,n(p)}$ for $n(p)$ type semiconductors is given by:

$$\tau_{Auger,n} = \frac{1}{C_n n^2 + C_p n \Delta n} \tag{4}$$

$$\tau_{Auger,p} = \frac{1}{C_p p^2 + C_n p \Delta n} \tag{5}$$

In Equations (4) and (5), C_n and C_p are the Auger coefficients for an Auger process that results in the excitation of an electron and hole respectively. The symbols n, p and Δn refer to the electron concentration, hole concentration and the excess electron concentration, respectively. These two equations illustrate the main limitation of the diffused junction approach to obtain carrier selective contacts in c-Si solar cells. For low level injection into the emitter, the Auger lifetime will vary approximately with the inverse square of the

majority carrier concentration. If the emitter doping is excessive (typically > 10^{17} cm^{-3}) [10], Auger recombination in the emitter will become significant because the recombination rate depends on the inverse of the Auger lifetime. Hence, there is a limit to the dopant concentration that can be used in the diffused contact. The use of an expensive high-temperature diffusion step also adds to the fabrication cost and mandates careful cleaning of the Si wafer prior to solar cell processing. Hence, a better carrier selective contact scheme is needed.

The bulk SRH recombination mechanism is similar to surface recombination discussed above. It is the main mechanism by which excess carriers in indirect band gap semiconductors such as Si recombine and equilibrium is restored. SRH recombination is a two-step process and involves a localized defect state in the band gap called a trap. This is because the band to band transition in an indirect band gap semiconductor is a three particle process and the probability is increased by the momentum uncertainty associated with the trap. An excess electron in the conduction band first occupies an empty trap state. In the second step, this electron returns to the valence band by recombining with a hole. The energy released by the excess electron is used to excite phonons in the crystal lattice. For a single trap state with energy E_t in the band gap, the SRH theory shows that the recombination rate U_t is given by [10]:

$$U_t = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \quad (6)$$

In this equation, n and p are the electron and hole concentrations respectively. $\tau_{p0} = (\sigma_p v_{th} N_t)^{-1}$ and $\tau_{n0} = (\sigma_n v_{th} N_t)^{-1}$ are the capture time constant of electrons and holes, respectively, and N_t is the concentration of the trap [10]. Note that, for a larger carrier capture cross section and a higher trap concentration, the SRH theory predicts a higher bulk recombination rate U_t. By assuming that the excess electron concentration Δn and excess hole concentration Δp are equal, U_t can be expressed instead as an injection level dependent SRH recombination lifetime, τ_{SRH} given by [10]:

$$\tau_{SRH} = \tau_{p0}\frac{n_0 + n_1 + \Delta n}{n_0 + p_0 + \Delta n} + \tau_{n0}\frac{p_0 + p_1 + \Delta n}{n_0 + p_0 + \Delta n} \quad (7)$$

Bulk recombination via the SRH mechanism can be reduced by using thinner wafers and improving crystal growth techniques. It is known that Czochralski (CZ) Si wafers typically contain C and O impurity atoms originated from the crucible used to hold the molten Si during crystal growth [8]. The FZ growth method on the other hand does not involve the use of crucibles and hence there are fewer recombination centers in FZ Si. The key material properties for SRH recombination are the minority carrier lifetime τ and minority carrier diffusion length $L = \sqrt{D\tau}$ where D is the carrier diffusion coefficient. For state-of-the-art c-Si solar cells, both bulk recombination and surface recombination are well optimized [24]. As a result, further reduction in carrier loss must be focused on the contact region. This explains the growing research interest in passivating contacts.

3. Passivating Contacts Involving Doped Si

The highest certified PCE of c-Si solar cells remained at 25% from 1999 until 2014, when Masuko et al. reported a silicon heterojunction (SHJ) solar cell with a PCE of 25.6% [33]. The SHJ is one of several types of carrier selective passivating contacts which is the focus of this article. All passivating contacts are based on the principle that the c-Si surface at the contact is passivated like the rest of the top and bottom surfaces of the c-Si solar cell. In most current passivating contacts, the contacting electrode is deposited onto an ultrathin interfacial passivation layer which reduces the amount of Si dangling bonds. This reduces the amount of surface recombination centers at the contact for electron hole recombination to take place [18]. In practice, band bending of the type discussed in Section 2 and heterojunction band offsets are utilized to enable carrier selectivity.

The concept of the passivating contact can be traced back to the pioneering work of Yablonovitch et al. in 1985 [34]. These investigators argued that the structure of an ideal solar cell should resemble that of a DHJ light emitting diode (LED) or semiconductor laser [35]. Figure 2a shows the energy band diagram of a DHJ LED comprising a narrower direct band gap active layer sandwiched between lattice matched p- and n-doped layers with a wider band gap. As shown, the DHJ LED is under forward bias and electrons and holes are injected into the active layer. Due to the favorable conduction and valence band offsets in the DHJ, electrons and holes are confined in the respective potential wells. As a result, the probability of radiative recombination (photon emission) is enhanced over the simpler p-n diode configuration [35]. The reverse process of what is shown in Figure 2a is the PV process. This process can be made efficient by using the asymmetric energy band diagram of Figure 2b in which one hetero contact has a small conduction band offset to facilitate electron extraction and a larger valence band offset to block holes. The other hetero contact has a small valence band offset to facilitate hole extraction and a larger conduction band offset to block electrons. Figure 2b corresponds to the open circuit condition. An important insight of Yablonovitch et al. is that, unlike the DHJ LED, it is not strictly necessary to find lattice-matched wider bandgap semiconductors for c-Si for this solar cell structure to work. So long as the interfaces between c-Si and the two other layers are well passivated, these layers can be polycrystalline or even non-crystalline semiconductors. This concept of the passivating contact has been experimentally demonstrated repeatedly since 1985.

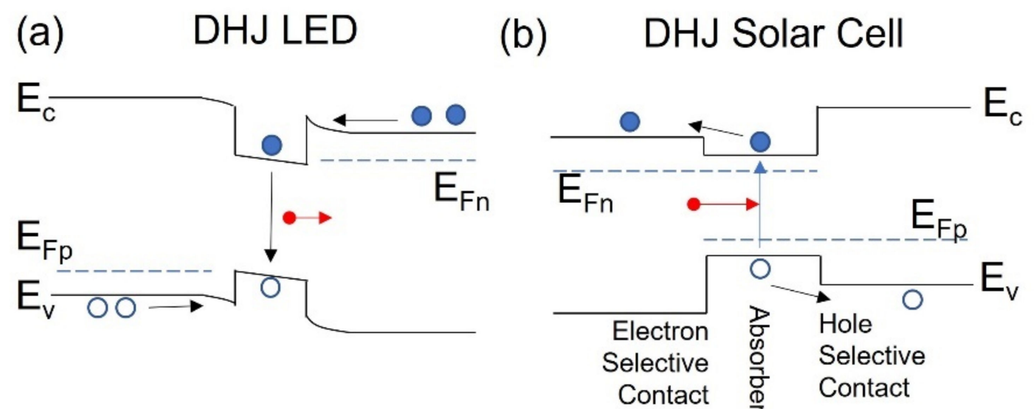

Figure 2. (**a**) Energy band diagram of a forward biased DHJ LED with lattice matched wider band gap injection and narrow band gap active layers; (**b**) energy band diagram of a DHJ c-Si solar cell with asymmetric hetero contacts.

The passivating contacts to c-Si solar cells can be divided into two categories: (i) doped Si and (ii) dopant-free (non-Si) passivating contacts. Here, 'dopant free' refers to the absence of extrinsic dopants in the contacting thin film layers. In the following, passivating contacts involving doped Si will be discussed first even though this topic has been comprehensively covered in earlier reviews [17,36]. It is necessary to discuss passivating contacts with doped Si because the passivation layers involved are still used in many dopant-free passivating contacts. This is due to the current passivation limitations of most dopant-free passivating contact films [37].

The two key parameters of a passivating contact are the reverse saturation current density component due to contact recombination, J_0 (or J_{0c} [16]) and the specific contact resistivity ρ_c. J_0 can be determined from S (surface recombination velocity) by using the quasi-steady-state photoconductance technique [38]. Here, ρ_c refers to the resistivity presented by the contact to the carrier being collected and is usually characterized by the method of Cox and Strack [39] or the transfer length method [40]. Note that, for an excellent carrier selective contact, both J_0 and ρ_c should be as low as possible.

In the literature [27], a more theoretical parameter called contact selectivity S_c has been proposed to characterize a carrier selective contact. S_c is defined in terms of the minority carrier resistance R_m and the majority carrier resistance R_M, where majority carrier here refers to the carrier that is supposed to be collected at the contact. The general definition of S_c is given by:

$$S_c(V) = \frac{R_m}{R_M g(V)} \tag{8}$$

where $g(V)$ is a voltage dependent factor [27]. For an ideal contact without voltage dependence, $S_c = kT/\rho_c J_0$.

3.1. Silicon Heterojunction

The SHJ passivating contact is a bilayer stack comprising an ultrathin intrinsic amorphous hydrogenated silicon (a-Si:H(i)) passivation layer and a p- or n-type a-Si:H contact layer [33]. Both these layers are deposited by PECVD from silane glow-discharge plasmas. Since PECVD can be performed at lower temperatures than thermal oxidation, the SHJ can reduce the production cost of c-Si solar cells [33]. The passivation property of intrinsic a-Si:H(i) for c-Si surfaces was first reported by Pankove and Tarng in 1979 [41]. Hydrogen (H) atoms in a-Si:H(i) act as the passivating species because H can only form one covalent bond. When H is chemically bonded to a surface Si atom with a dangling bond, it becomes a terminating atom and one surface state is thereby passivated by the H atom [41]. The effectiveness of a-Si:H(i) in passivating c-Si was demonstrated experimentally by using meandering diffused p-n junctions with a large perimeter-to-area ratio. When a-Si:H(i) was deposited onto the p-n junction, the reverse biased leakage current was found to be two orders of magnitude smaller than those control junctions that were passivated by thermal SiO_2 [41]. By assuming that the leakage current mechanism is lateral tunneling assisted by generation-recombination centers, it was inferred that the a-Si:H(i) layer results in fewer such centers at the c-Si surface compared with thermal oxide. The role of the a-Si matrix material is to provide a solid-state medium so that the weak Si-H bonds are encapsulated and the passivated Si surface is stable. Since the energy band gap of a-Si is 1.7 eV [42], the a-Si:H/Si contact is an isotype heterojunction. This junction, which can be readily fabricated by industrial PECVD systems, was first studied by researchers at Sanyo Electric Ltd. (Osaka, Japan) in 1990 because of its potential for low-cost high efficiency c-Si solar cells [43]. Due to sustained research efforts, the PCE of SHJ cells improved from 14.5% in 1990 to >20% after 2000. In the PV industry, the SHJ solar cell is often referred by the trade name heterojunction with thin intrinsic layer (HIT) cell [44]. In this article, the scientific term SHJ will be used instead.

The benefits of a-Si:H(i) in reducing surface recombination in solar cells was demonstrated by Taguchi et al. in 2013 using a high efficiency bifacial SHJ cell structure [44]. This cell with a symmetrical device structure and full area front and back contacts was fabricated on a thin (98 μm) n-type CZ wafer with random surface texture. The top surface has a hole-selective a-Si:H(p)/a-Si:H(i) contact while the bottom surface has a a-Si:H(n)/a-Si:H(i) electron-selective contact. Since the thickness of each layer is limited to ~10 nm, transparent conducting oxide (TCO) and metal grid electrodes were deposited on both sides of the wafer. As a result, lateral charge transport is involved during carrier collection. The bifacial SHJ cell by Taguchi et al. has a high PCE of 24.7%, which is mainly due to improvements in V_{oc} and FF relative to an earlier SHJ cell by the same group [44]. The very high V_{oc} of 0.750 V was due to improvements in the surface preparation of the Si wafer and optimization of the deposition of a-Si:H(i) which reduced the surface recombination velocity to 2 cm/s [44]. The FF, which has a high value of 83.2%, is due to smaller recombination loss and reduced parasitic resistance in the TCO film and the Ag paste used for screen printing the grid electrodes. J_{sc} is slightly improved to 39.5 mA/cm^2 over the previous device due to improvement in the aspect ratio and shadowing loss of the front grid electrodes. A smaller footprint for the grid electrodes increases the percentage of Si surface available for absorbing sunlight.

The 25% efficiency record long held by the PERL cell (Section 2) was exceeded by the SHJ cell fabricated by Masuko et al. at Panasonic Corporation in 2014 [33]. The main limitation of the bifacial cell of Taguchi et al. is the parasitic absorption of sunlight at the TCO and a-Si:H(p)/a-Si:H(i) layers. In addition, the use of a front grid contact reduces the amount of wafer area available for absorption as mentioned above. Higher PV performance can be realized by using an interdigitated back contact (IBC) cell structure. In the IBC cell, the illuminated side of the cell is entirely light absorbing because the a-Si:H(p)/a-Si:H(i) and a-Si:H(n)/a-Si:H(i) passivating contacts are situated at the back of the wafer. The absence of a-Si:H at the front side allows SiN_x antireflective layer to be deposited to reduce reflection. As a result, both J_{sc} and external quantum efficiency (EQE) are improved and a high certified PCE of 25.6% was achieved [33].

Using the same IBC cell structure, Yoshikawa et al. of Kaneka Corporation reported an even higher certified PCE of 26.3% for their SHJ solar cell in 2017 [45]. This champion cell was fabricated on a n-type CZ Si wafer with a thickness of 165 μm and a designated area of 180.4 cm^2. The V_{oc}, J_{sc} and FF of the cell are 744 mV, 42.3 $mAcm^{-2}$ and 83.2% respectively [45].

The carrier selectivity of the a-Si:H(p)/a-Si:H(i) and a-Si:H(n)/a-Si:H(i) passivating contact layers can be understood from the fundamental study of the a-Si:H(i)/n-Si(111) heterojunction by Schulze et al. [46]. In this work, a-Si:H(i) films (~10 nm) was deposited by PECVD with different silane to hydrogen flow ratio onto n-type (111) Si (n-Si) wafers. n-Si substrates are used because typical high performance SHJ cells are fabricated using this type of wafer. The reason for this will be elaborated below. Unlike prior studies, the a-Si:H(i) layer thickness is comparable to that used in SHJ solar cells and the composition of H in a-Si:H(i) was varied [46]. The H content determined from quantitative Fourier transform infra-red (FTIR) spectroscopy was found to affect the optical band gap $E_{g,a-Si:H}^{opt}$ deduced from spectroscopic ellipsometry data. The optical band gap increases from ~1.6 eV to 1.8 eV when the H content is varied from ~12% to 24 at%.

Figure 3 shows the schematic equilibrium energy band diagram of the a-Si:H(i)/n-Si(111) heterojunction. Note that this is a type I straddling heterojunction [19]. The key energetic parameters of Figure 3 are the valence band offset ΔE_v and conduction band offset ΔE_c. These band offsets are not straightforward to determine. The energy of the valence band edge of a-Si:H(i) is complicated by the band tail in amorphous semiconductors. The band tail states of the valence band are localized states arising from the lack of long-range order. In an energy band diagram, these states are situated above the extended valence band states. The mobility edge, $E_{v,a-Si:H}^{\mu}$, which marks the transition from extended to band tail states, is used as the valence band edge for a-Si:H(i). This, together with the $E_{v,c\text{-}Si}$ of Si, were characterized by near ultra-violet photoelectron spectroscopy (NUVPES) in the constant final state yield mode [47]. The valence band offset is calculated from the following equation:

$$\Delta E_V = E_{V,c\text{-}Si} - E_{V,a\text{-}Si:H}^{\mu} + e\varphi \quad (9)$$

Here, $e\varphi$ is the amount of band bending in n-Si and can be measured by a surface photovoltage (SPV) method [48]. The SPV signal after applying the Dember correction is the band bending $e\varphi$ in n-Si [46].

The conduction band offset ΔE_c can be found similarly from the equation:

$$\Delta E_C = E_{C,a\text{-}Si:H}^{\mu} - E_{C,c\text{-}Si} + e\varphi \quad (10)$$

The extracted ΔE_v is significantly larger than ΔE_c across this entire composition range of H studied. Although ΔE_v increases linearly from 0.4 eV (~12 at.% H) to 0.6 eV (~24 at.% H) and not affected by the c-Si dopant type, the fitted ΔE_c only has a weak negative linear correlation with H content over this range with an average value of ~0.25 eV.

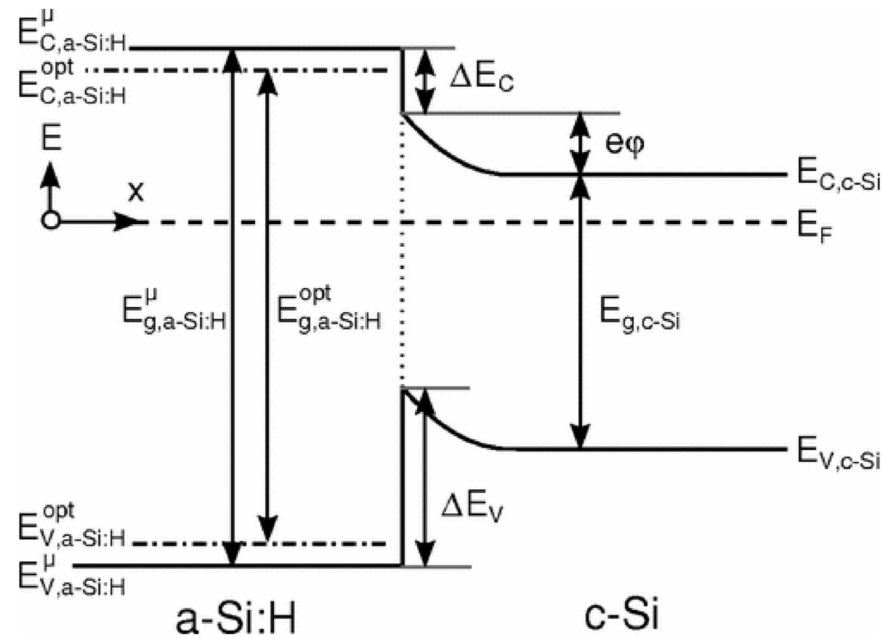

Figure 3. Energy band diagram of the a:Si-H(i)/n-Si heterojunction showing conduction and valence band offsets and band bending in n-Si (Adapted with permission from Ref. [46] 2011, American Physical Society, http://dx.doi.org/10.1103/PhysRevB.83.165314 (accessed on 16 June 2022)).

By using the known conduction and valence band offsets for the SHJ junction, an equilibrium energy band diagram for n- and p-type SHJ solar cells can be constructed as shown in Figure 4. Depending on the direction of incidence of sunlight (from left or right), the Figure can represent a front or rear emitter SHJ cell. The band diagram shows that, for both types of SHJ solar cell, it is the band bending in c-Si and the band offsets that give rise to asymmetric carrier conductivity. Collections of holes should involve carrier transport through a spike-like energy barrier. The asymmetry in the valence and conduction band offsets of the a-Si:H(i)/c-Si heterojunction may explain the empirical observation that SHJ cells fabricated on n-Si wafers tend to have better performance than p-type SHJ cells and why, in the literature, n-Si wafers are used more often for SHJ devices. In a comparative study [49], Descoeudres et al. fabricated front emitter SHJ solar cells from n- and p type FZ Si wafers. The device structures are Ag(grid)/ITO/a-Si:H(p^+)/a-Si:H(i)/n-Si/a-Si:H(i)/a-Si:H(n^+)/ITO/Ag for n-type devices and Ag(grid)/ITO/a-Si:H(n^+)/a-Si:H(i)/p-Si/a-Si:H(i)/a-Si:H(p^+)/ITO/Ag for p-type devices. Although the energy band diagram for the minority carrier is different in these devices due to the different band offsets, the V_{oc} for both devices were found to be identical. In addition, the p-type SHJ device has only a slightly lower FF than the n-type device. As a result, the PCE of the p-type device is only 0.2% (absolute) lower than that of the n-type device. Thus, the different band offsets actually do not have a strong effect on the carrier recombination and current transport. The difference is more likely due to the larger SRH capture cross section for electrons than for holes [49]. Experimental evidence for this is the much lower effective carrier lifetime for p-type wafers at low level injection conditions where Auger recombination is not dominant [49].

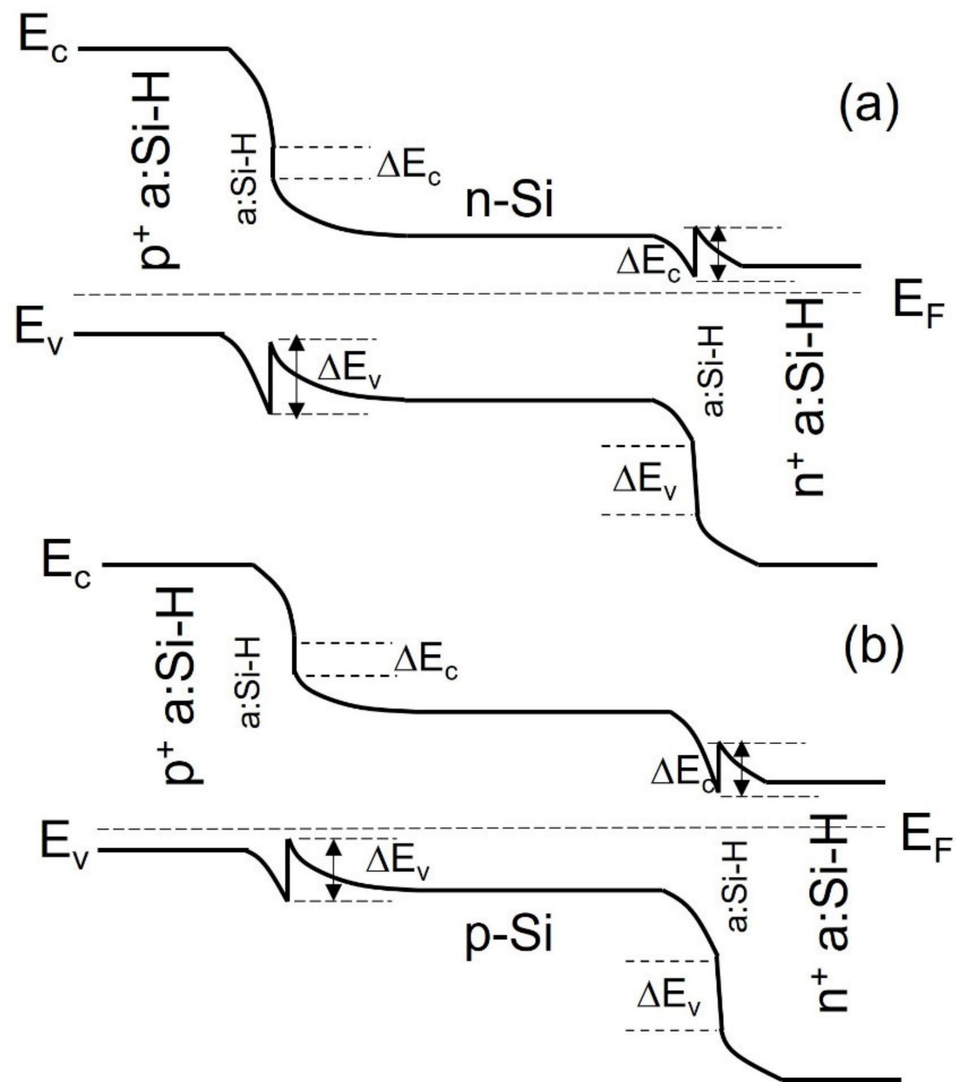

Figure 4. Schematic energy band diagram of (**a**) n-type SHJ solar cell; (**b**) p-type SHJ solar cell.

Despite its high efficiency, the SHJ solar cell has two limitations. The first is that, for a bifacial cell structure, the doped a-Si:H contact layer at the front can absorb short wavelength sunlight leading to reduced absorption in the c-Si [33]. The parasitic absorption caused by the ~1.7 eV band gap of a-Si:H can result in reduction of EQE at shorter wavelengths. In addition, it has been shown experimentally by De Wolf and Kondo that the passivation capability of a-Si:H(i) can be degraded by an overlayer of a-Si:H(p^+) especially when the a-Si:H(i)/a-Si:H(p^+) stack is annealed at temperatures above 220 °C [50]. The degradation is due to hydrogen loss from the a-Si:H(i). As a result of this constraint, the SHJ cell cannot be annealed at above 220 °C once the a-Si:H layers are deposited. All backend process steps, such as annealing and packaging, will have to be customized for such cells and performed at moderate temperatures.

3.2. Polysilicon on Oxide

The polysilicon on oxide (POLO) passivating contact consists of an ultrathin interfacial silicon oxide and a layer of heavily doped polysilicon. The ultrathin oxide can be formed on c-Si by thermal oxidation [51], by wet chemical oxidation [52] or by reaction with ozone [27]. The doped polysilicon layer can be deposited by low-pressure chemical vapor deposition (LPCVD) or PECVD [53]. Like the SHJ, the POLO contact is a promising passivating contact because the materials involved are silicon based, and the contact properties had been

extensively studied for the polysilicon bipolar transistor [54]. The fabrication process can therefore be readily used for manufacturing.

In terms of technology development, the POLO passivating contact pre-dates the SHJ. This is because the first demonstration (in 1985) of a c-Si solar cell with two passivating contacts was based on an early version of the POLO contact [34]. The proof-of-principle device by Yablonovitch et al. was fabricated on a p-type FZ Si (100) wafer with the SiO_x passivation layer grown by dry oxidation [34]. The semi-insulating polycrystalline silicon (SIPOS) was deposited on both sides of the wafer by atmospheric-pressure chemical vapor deposition (APCVD). SIPOS is a complex composite material consisting of heavily n-doped microcrystalline silicon embedded in a non-stoichiometric SiO_x matrix. The SiO_x provides the passivation needed for the Si(100) surface. Although the device structure studied was not optimized for high PCE in [34], a remarkable V_{oc} of 720 mV was observed at 1.3 sun illumination and 25 °C. By measuring photoconductivity decay lifetimes on high quality thin wafers with known dopant density, the saturation current density J_0 for the SIPOS-Si contact was determined to be 10 $fAcm^{-2}$ [34]. Both V_{oc} and J_0 are comparable to values obtained for state-of-the-art SHJ solar cells in the 21st century and demonstrate the excellent passivation provided by SIPOS. It should be pointed out that meticulous attention to device processing conditions are crucial for the realization of excellent passivation. One important difference between the POLO contact and the SHJ is that thermal annealing at temperatures above 700 °C is required after SIPOS deposition [34]. This high-temperature step is needed for activation of the dopants incorporated in polysilicon. As a result of high-temperature annealing, some dopants will diffuse into crystalline silicon, and this may be accompanied by the appearance of pinholes in the SiO_x layer [55]. Both these phenomena have also been observed in the emitters of polysilicon bipolar transistors [54].

The idea of a POLO contact for a c-Si solar cell was revived by Feldmann et al. in 2014 [53]. These investigators fabricated a hybrid n-type c-Si cell as shown in Figure 5a, in which the full-area rear electron-selective contact was a tunnel oxide-passivated contact (TOPCon). Note that TOPCon is another equivalent term used for the POLO contact. The hole-selective contact at the front is a conventional boron-diffused p^+ emitter with an AlO_x passivation layer and AR layer. For the TOPCon, the ultra-thin oxide layer was formed by wet chemical oxidation of Si and the n-doped polysilicon film was deposited by PECVD. The details of the polysilicon deposition have not been disclosed in the publications [53]. However, it is known that a-Si is deposited first and is followed by annealing. The post-deposition annealing temperatures ranged from 600–1000 °C. For annealing between 800–900 °C, a low J_0 ~10 $fAcm^{-2}$ can be obtained. However, above 900 °C, the formation of silicon monoxide (SiO), which is gaseous, led to a rapid deterioration of J_0. Hybrid c-Si cells with TOPCon contact has a PCE of 21.7% versus 19.5% for the reference device with un-passivated back contact. The improvement in PCE is due to a significantly higher V_{oc} resulting from reduced contact recombination.

When the TOPCon contact is used for both electron- and hole-selective contacts (Figure 5b), an independently measured PCE of 24.4% was observed [56]. In subsequent work [57], the hybrid ToPCon solar cell in Figure 5a was further improved by depositing a double layer anti-reflection coating (DARC) comprising SiN_x/MgF_2 on the randomly textured front side of the device. In addition, to reduce the contact recombination at the front electrodes, a locally diffused p^{++} emitter was formed after contact hole etching. These modifications to the fabrication process resulted in a PCE of 25.7% measured under standard test conditions [57].

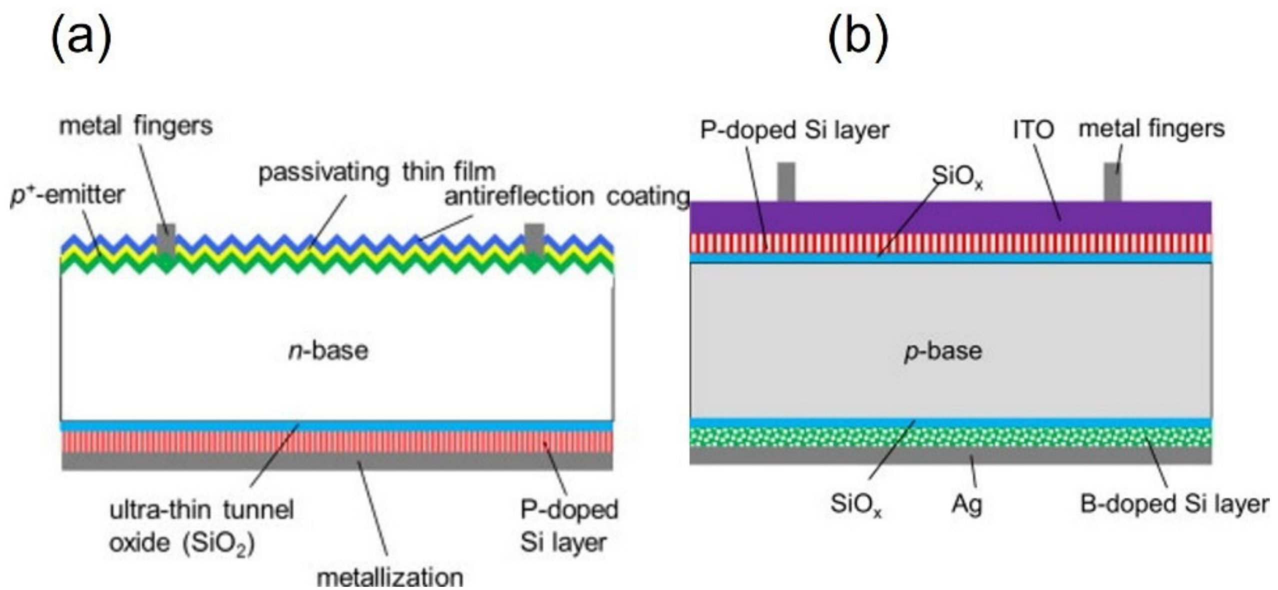

Figure 5. (**a**) Schematic diagram of hybrid n-type c-Si solar cell with full area p^+ polysilicon/SiO_2 rear contact (Reprinted from Ref. [53] Solar Energy Materials and Solar Cells, Vol. 120, F. Feldmann, M. Bivour, C. Reichel, M. Hermle, S.W. Glunz, Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics, 270–274, 2014, with permission from Elsevier); (**b**) schematic diagram of p-type c-Si solar cell with full area n^+ polysilicon/SiO_2 front contact and p^+ polysilicon/SiO_2 rear contact (Reprinted from Ref. [56] Solar Energy Materials and Solar Cells, Vol. 131, F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, S.W. Glunz, Efficient carrier-selective p- and n-contacts for Si solar cells, 100–104, 2014, with permission from Elsevier).

As with the SHJ, even higher PCE can be realized by using the IBC device structure in which both the electron-selective and hole-selective POLO contacts are located on the back side of the wafer. An early example of the POLO-IBC cell is the black IBC c-Si cell by Yang et al. [58]. The interdigitated back contacts were fabricated by selective ion implantation of P and B followed by anisotropic trench etching to form the gaps. The front side of this cell featured a novel modulated surface texturing (MST) ARC structure which consists of a nano-textured SiO_2 layer deposited on the random pyramids. The MST reduces the front reflectance (<1%) to that of black Si. For front surface passivation of a-Si:H/a-SiN_x:H, a device PCE of 23% was obtained. An improved POLO-IBC cell was reported by Hollemann et al. in 2019 [59]. In this work, the n-POLO and p-POLO contacts were separated by masked ion implantation of B and P into a LPCVD intrinsic a-Si layer deposited on oxide. After high-temperature annealing and Al evaporation, the Al is patterned into separate contacts by a laser contact opening process [60]. The POLO-IBC device fabricated with this back contact process has a measured PCE of 26.1% which is comparable to the PCE of the SHJ-IBC cell in Section 3.1.

The carrier selectivity mechanism of the POLO contact is more complicated and subtle than the SHJ. Figure 6 shows an idealized equilibrium band diagram of the n^+ poly/n-Si and p^+ poly/n-Si contacts. Here, it is assumed that the grain size of the polysilicon is not in the nanoscale so that a bulk value of the band gap can be used for polysilicon. The short lines in the band gap represent the numerous defect states in the polysilicon. It is also assumed that the ultrathin SiO_x is continuous and without pinholes. The band bending in the c-Si next to SiO_x contributes to carrier selectivity with J_0 that can be in the sub 10 fAcm^{-2} range [61]. However, the oxide layer is also involved. This is because when the interfacial oxide is removed and the polysilicon is allowed to directly contact the n-Si, the J_0 was observed to be much higher (>0.5 pAcm^{-2}) even though the same band bending is present [61]. Since the SiO_x in the POLO contact is typically <4 nm, a direct tunneling model

was proposed to account for the role of the SiO_x. This model makes use of the conduction band offset (3.1 eV) and the valence band offset (4.8 eV) in Figure 6 between SiO_x and n-Si. These offset values are determined from internal photoemission spectroscopy [60]. Since the tunneling probability depends exponentially on the square root of the barrier height, electron tunneling is more efficient than hole tunneling. For the n^+ poly/n-Si POLO contact, this can explain the low J_0 and ρ_c observed experimentally (see Figure 2 in [60]). On the other hand, the tunneling model cannot account for the observed J_0 and ρ_c in p^+ poly/n-Si contacts. This is because according to this model, both J_0 and ρ_c should be higher than n^+ poly/n-Si contacts due to the larger hole barrier height. This however is not consistent with experiment which showed on the whole little difference between the J_0 and ρ_c of the two types of contacts [61].

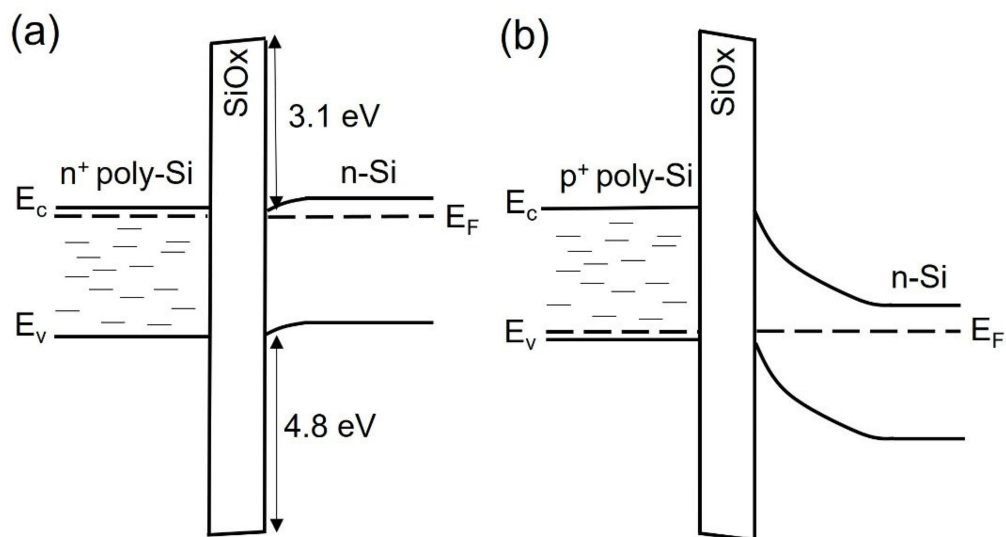

Figure 6. Schematic energy band diagram of (**a**) n^+ polysilicon/n-Si POLO contact; (**b**) p^+ polysilicon/n-Si POLO contact.

An improved model was proposed by Peibst et al. that can account for both types of POLO contacts [61]. The main feature of this model is that the SiO_x layer is not of uniform thickness after thermal annealing. As shown in Figure 7, there can be localized areas where the SiO_x is of reduced thickness or where it is absent. Pinholes in ultrathin oxide has been observed by conductive atomic force microscopy [62]. At pinholes, the direct contact between the polysilicon and the c-Si can cause epitaxial regrowth to occur [55]. In addition, as with the polysilicon BJT, there is diffusion of dopants from the heavily doped polysilicon into the c-Si forming a heavily doped surface region in the c-Si. In this non-uniform SiO_x layer, electrons and holes will flow mainly through pinholes or localized spots of reduced oxide thickness. However, since the tunnelling probability decreases with increasing oxide thickness, the current will flow mainly through pinholes in thicker oxides. The direct tunneling current should play only a minor role. By considering the localized current flow and using the fitting parameters in the equations of the alternative model, the experimental J_0 and ρ_c data for both types of POLO contacts can be fitted satisfactorily [61].

The POLO contact has been actively investigated for industrial production and commercialization. Mewe et al. reported a full wafer size (156 mm × 156 mm) n-type CZ IBC cell fabricated by industrial equipment [63]. The p- and n- POLO contacts are stabilized by H-rich Al_2O_3/SiN_x capping layer. This capping bilayer especially improves the passivation quality of the hole extraction contact with a measured J_0 of 10 $fAcm^{-2}$. However, the FF of this IBC cell was low due to high series resistance and the device PCE was not reported.

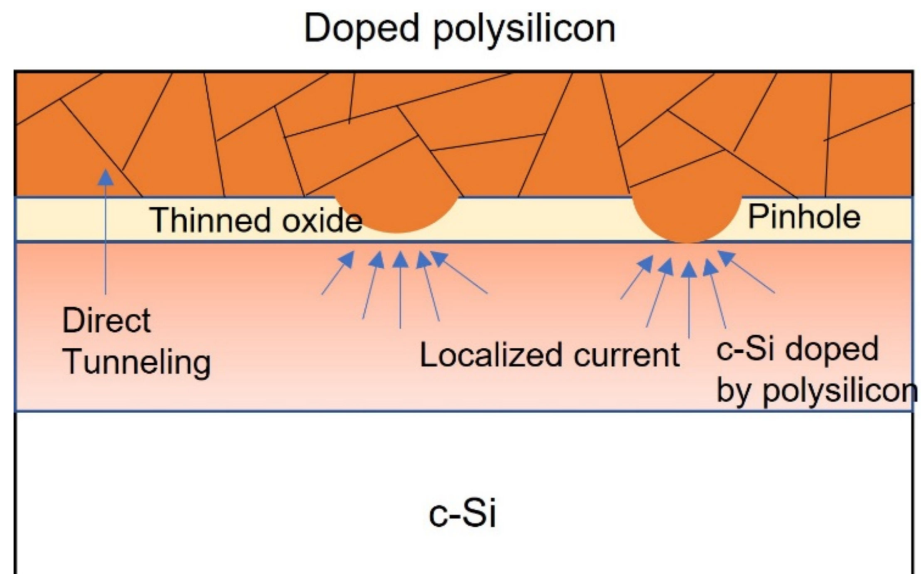

Figure 7. Schematic diagram of a POLO contact with a non-uniform SiO_x layer. The possible conduction paths include direct tunneling, localized conduction near thinned SiO_x and localized conduction through pinholes.

Very recently, Liu et al. used an industrial i-TOPCon process and 157.4 mm × 157.4 mm quasi-monocrystalline cast wafers to fabricate high efficiency bifacial Si solar cells with a rear n-POLO contact with SiN_x passivation and screen-printed electrodes. The champion device has a measured V_{oc} of 712 mV and a certified efficiency of 23.22% [64]. When this process is applied to n-type CZ wafers, a certified best cell efficiency of 23.57% and median module power over 345 W were obtained [65]. In [66], this group reported a higher median efficiency of 23.91% and certified total area efficiency of 24.58% for the same substrate type.

4. Dopant-Free Passivating Contacts

In recent years, the literature in the field of silicon photovoltaics has been dominated by non-silicon based passivating contact schemes. This third type of passivating contact for c-Si is often referred to as dopant-free passivating contacts. The dopant-free passivating contacts are wide band gap (transparent) thin film materials that have been used previously as charge injection layers in organic light emitting diodes (OLED) [67] or as charge extraction layers in dye sensitized solar cells (DSSC) [68], organic solar cells (OSC) [69], chalcogenide [70] and perovskite thin film solar cells [71]. Depending on carrier selectivity, they either have high or low work function. The use of these non-Si thin film materials for forming the DHJ in high efficiency c-Si solar cells is motivated by the cost reduction requirement for solar cell manufacturing. While both the SHJ and POLO contacts have demonstrated high PCE in c-Si solar cells, the cost of manufacturing is nonetheless high. For the SHJ, the deposition of the a-Si:H(i), a-Si:H(p) and a-Si:H(n) layers require the use of PECVD cluster tools and cleanroom environments which incur significant capital expenditure. In addition, since the precursor gas (SiH_4) is pyrophoric and the dopant gases (B_2H_6 and PH_3) are highly toxic and flammable, the installation of mandatory health and safety facilities and staff safety training will add further to the running cost. For the POLO contact, the deposition of the a-Si layer by LPCVD can cause yield issues and must be followed by a high-temperature annealing step to form the semicrystalline Si. This requires furnace processing and can result in added cost and longer production time.

Many thin film materials have been studied for possible application as dopant-free passivating contacts [16]. Amongst these, the most important group are the transition metal oxides (TMO) [72]. In addition, there are organic conducting polymers [73], alkali metal fluorides (AMF) and alkali earth metal fluorides [16]. An important distinction between the dopant-free passivating contacts and the doped Si contacts is that since the former is

not extrinsic, a given dopant-free contact material can only be either electron selective or hole selective but not both. In the following sub-sections, we discuss several dopant-free passivating contacts beginning with electron-selective contacts. These passivating contact materials are highlighted because they have been successfully integrated into c-Si solar cells with demonstrated high energy conversion efficiency.

Electron-selective contacts are important to the fabrication of n-type c-Si solar cells. This is due to the anomalous junction characteristics of Al/n-Si contacts [74]. If the Mott–Schottky theory were applicable, the Al/n-Si contact should, in principle, be ohmic with low contact resistance. This is because of the similar values for the work function of Al and the electron affinity of Si. However, in practice, deposition of Al onto n-Si with or without subsequent annealing will always result in a substantial Schottky barrier height (0.65–0.7 eV) and a rectifying contact [74]. This anomaly is usually attributed to a high density of interface states for Al/n-Si and the Fermi level pinning effect. Similarly, according to the Mott–Schottky theory, the Al/p-Si contact should be rectifying because the work function of Al is smaller than that of p-Si. However, in practice this barrier height is very small and the Al/p-Si contact is actually ohmic. This explains why as mentioned in Section 2, p-Si wafers are normally used for the manufacturing of Al-BSF cells.

4.1. Titanium Oxide

Titanium oxide (TiO_x) is an n-type semiconductor or electron transport layer (ETL) with a wide band gap of 3.7 eV [75]. TiO_x exhibits polymorphism and several crystalline structures such as the anatase, rutile, brooklite and the Magneli phase of TiO_x are known [75]. Between 1970 and 1990, TiO_x was used as an AR coating for c-Si solar cells because of its higher refractive index of 2.4 [76]. In its mesoporous form, TiO_x is often used as the ETL in DSSCs for extracting electrons originated from the photo-excited state of adsorbed organometallic dye molecules [68]. The porosity of TiO_x increases the available surface area for adsorption. Kim et al. reported the use of TiO_x as a hole-blocking contact for bulk heterojunction OSCs in 2015 [75]. In this application, the TiO_x layer prevents holes in the percolation path of the donor material from reaching the cathode and recombining with electrons. In the same study [75], these investigators also reported the observation of hole-blocking properties of TiO_x for the TiO_x/Si junction which suggests suitability for c-Si photovoltaics.

The passivation of c-Si surfaces by TiO_x was initially investigated by depositing TiO_x using various deposition techniques. For APCVD and sol-gel-deposited TiO_x, a light-enhanced passivation effect for c-Si was observed [76,77]. However, the light-enhanced passivation effect is not stable and the minority carrier lifetime decreases exponentially within minutes to the pre-illumination value after the light source is turned off [77]. Much more stable passivation of low resistivity FZ n-Si and p-Si wafers after light soaking, however, was reported by Liao et al. for thermal ALD deposited TiO_x films [76]. These films, with a thickness of 60 nm, were annealed at 200–250 °C after ALD before light soaking under a halogen lamp at an intensity of 0.2 sun for about 2 h. The effective surface recombination velocity S_{eff} calculated from the measured effective carrier lifetime are 8.3 cm/s and 2.8 cm/s for p-Si and n-Si respectively. These extremely low S_{eff} values were found to remain stable after storage in the dark for 8 months [76].

The first demonstration of electron-selective TiO_x contacts for c-Si solar cells was reported by Avasthi in 2013 [78]. Their proof-of-concept device structure consists of Al/TiO_x/Si/Ag. The 3 nm thick TiO_x passivating contact was deposited by a modified CVD process using a single organometallic precursor, titanium (IV) tetra-(tert-butoxide) [78]. Both n-Si and p-Si (100) wafers were used as substrates. The top Al electrode (15 nm) was deposited through a metal mask while a blanket Ag film was deposited at the back of the Si wafer to form an ohmic contact. When a n-Si wafer is used as the substrate, the dark J-V characteristic is linear, and the usual rectifying characteristic of Al/n-Si is no longer observed. This shows that there is no energy barrier impeding the flow of the majority carrier (electrons) for both forward and reverse bias. For the devices with p-Si substrates,

the opposite is observed. Instead of an ohmic J-V characteristic, a rectifying characteristic with a negative turn-on voltage of ~−0.5 V was observed [78]. Since holes are the majority carriers in these p-type devices, there must be an energy barrier for holes at the TiO_x/Si interface. The magnitude of these energy barriers can be determined from the published electron affinity and ionization potential for TiO_x and Si. The electron affinity for TiO_x and Si are 4.0 eV and 4.05 eV respectively [78]. For the ionization potential, the values for TiO_x and Si are ~7.1 eV and 5.17 eV respectively [78]. Thus, the type II TiO_x/Si heterojunction has a ΔE_c of ~50 meV and a ΔE_v of ~1.9 eV. Since $\Delta E_c << \Delta E_v$, the heterojunction will block holes and allow electrons to flow through with low contact resistance. When illuminated by a solar simulator with AM1.5 spectrum, an Al/TiO_x/p-Si/Ag device shows a photovoltaic response with a J_{sc} of 19.3 mAcm^{-2}, V_{oc} of 520 mV and FF of 70%. Although this device is not optimized for PCE, the results nonetheless demonstrate that TiO_x can be used as a hole blocking passivating contact in c-Si solar cells. The thickness of the TiO_x layer prevents holes from reaching the Al where recombination can occur.

The effectiveness and mechanism of TiO_x as an electron-selective passivating contact were demonstrated in more detail by Yang et al. in 2016 [79]. In this work, the TiO_2 or SiO_2/TiO_2 passivation layers (4–5 nm) deposited by ALD on n-Si formed a full-area passivating back contact for electrons. This was followed by thermal evaporation of an Al/Ag metallization layer. The front side structure of the 'hybrid' c-Si solar cell follows the Al-BSF cell (Figure 8). When illuminated under AM1.5 conditions, the device with the TiO_2/Al back contact showed a PCE 19.8% while the SiO_2/TiO_2/Al contact had a PCE of 21.6%. Both these efficiencies are significantly higher than the control device (17.6%) [79].

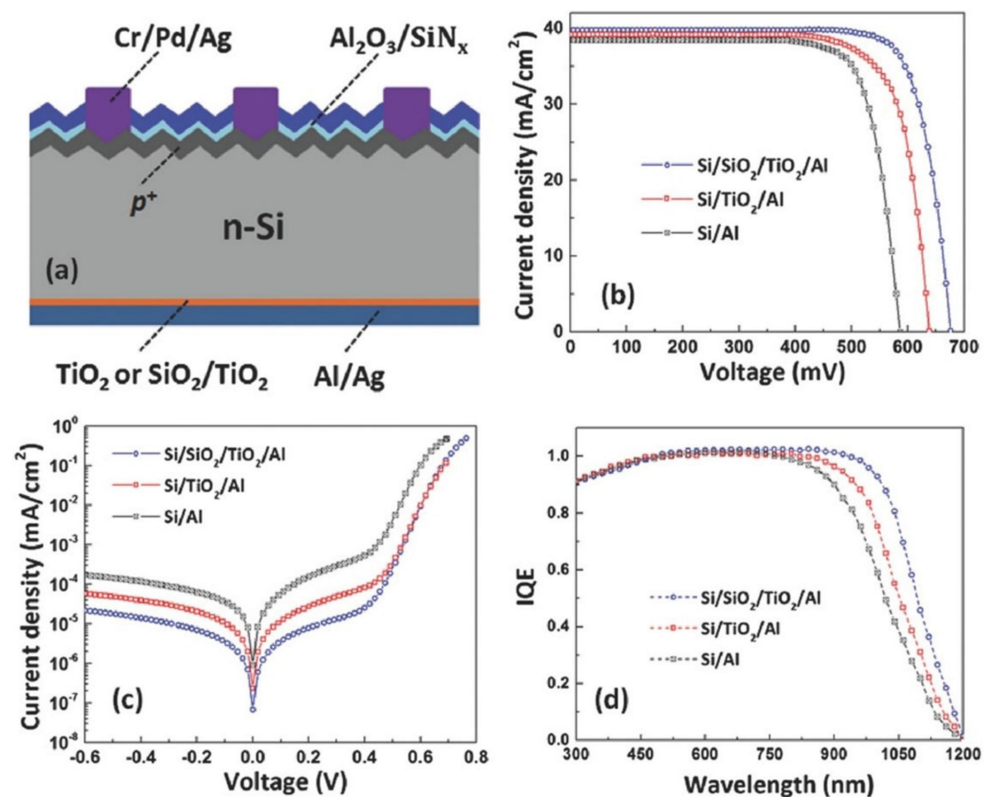

Figure 8. (**a**) Schematic diagram of hybrid n-type c−Si solar cell with full area TiO_2 or SiO_2/TiO_2 rear contact and diffused front junction; (**b**) current density−voltage characteristics of three devices under illumination; (**c**) dark current density−voltage characteristics of three devices; (**d**) internal quantum efficiency spectra of three devices (Reprinted from Ref. [79] X. Yang, Q. Bi, H. Ali, K. Davis, W.V. Schoenfeld, K. Weber, High-performance TiO_2-based electron-selective contacts for crystalline silicon solar cells, Advanced Materials, ©2016 WILEY−VCH Verlab GmbH & Co. KGaA, Weinheim).

In a subsequent article [37], Yang et al. also investigated the applicability of TiO_2 contacts to industrial c-Si solar cell production. The experiments, which involved devices with a full area TiO_2 rear contact, considered the effects of n-type Si wafer resistivity, exposure to air, Si substrate thickness and the firing temperature on PCE. N-type wafers were chosen because, for this type of Si wafer, there is a tendency for a larger distribution of resistivity along the ingot, a consequence of the segregation coefficient of P [37]. The PCE of devices with the TiO_2 passivating contact was found to vary little with wafer resistivity from 0.1 Ωcm to 100 Ωcm. Similarly, the PCE remained stable after storage in air for several months. A PCE of 21.5% was obtained for a device fabricated on ultrathin (80 µm) Si wafers. The main improvement required is the firing temperature because the firing was only performed at a temperature of 575 °C. Overall, TiO_2 contacts are well suited to industrial c-Si solar cell manufacturing.

4.2. Magnesium Oxide

In its stoichiometric form, magnesium oxide (MgO) is an insulator with a band gap of 6.06 eV [80]. MgO crystallizes as an ionic solid with a rock salt structure [80]. The use of non-stoichiometric MgO_x as a contact material was first reported by Choi et al. for top emitting OLEDs with an inverted structure [81]. In photovoltaics, MgO_x can function as an electron-selective passivating contact for n-Si as demonstrated by Wan et al. in 2017 [82]. In this study, MgO_x was deposited by simple thermal evaporation from a high purity powder source. From Hall-effect characterization, the evaporated MgO_x film was determined to be n-type with an electrical conductivity of 173 Scm^{-1}. The much higher conductivity compared with MgO is due to the oxygen deficiency of MgO_x with x = 0.75 determined from X-ray photoelectron spectroscopy (XPS). As with SnO_x, the oxygen vacancies (V_O) behave as dopant levels and form an impurity band near the Fermi level, resulting in n-type conductivity.

Hybrid (single heterojunction) c-Si solar cells with MgO_x as a passivating contact were fabricated with the structure $Ag/SiN_x/Al_2O_3$/n-Si/MgO_x/Al. The starting substrate is a n-type CZ (100) Si wafer. The device structure of the top (sun-facing) side is conventional and consists of a randomly textured surface obtained by anisotropic wet etching. After boron diffusion to form the p+ layer, the SiN_x and Al_2O_3 were deposited by PECVD and ALD respectively. The full area electron-selective back contact consists of a 1 nm thick MgO_x layer and a 100 nm Al layer [82] (note that this is much simpler than the back contact for a conventional n-type c-Si cell). When illuminated under standard test conditions, this proof-of-concept device showed a high PCE of 20.0% compared with 15.3% for the control device without MgO_x. As shown in ref. [82], the V_{oc}, J_{sc} and FF of the solar cell with MgO_x passivating contact are all substantially higher than the control device. This is due to improved passivation at the back contact and a lower contact resistivity when MgO_x passivation layer is used. The lower contact resistivity is evidenced by a low equivalent series resistance of 0.3 Ωcm^2.

Wan et al. also investigated the stability of the fabricated solar cells with MgO_x with respect to thermal cycling. It was found that the photovoltaic parameters are stable for annealing at temperatures up to 400 °C for 10 min. However, when the annealing was performed at 500 °C for 10 min, there is a large decrease in V_{oc}, J_{sc} and FF [82]. This shows that MgO_x is also a viable electron-selective passivating contact material for n-type c-Si solar cells.

4.3. Lithium Fluoride

Lithium fluoride (LiF_x) is a widely used electron injection layer (EIL) in OLED technology [83]. During the 1990s, ultrathin layers of vapor deposited LiF_x were reported to facilitate electron injection from a metal cathode into the EIL of small-molecule OLEDs [83]. The improved electron injection enhances the charge balance factor which is one of the factors determining the internal quantum efficiency of an OLED. LiF_x is an insulator with a band gap of >10 eV [84]. The main method of depositing ultrathin LiF_x is thermal evapora-

tion. The use of evaporated LiF_x as electron-selective passivating contacts in c-Si solar cells was first demonstrated in 2016 [84]. As will be discussed in Section 5, LiF_x is nowadays the preferred passivating contact material for DHJ or DASH silicon solar cells.

The electron extraction mechanism for LiF_x passivating contacts in c-Si cells was elucidated by Bullock et al. using analytical scanning transmission electron microscopy (STEM) and measurement of ρ_c. From high resolution STEM observation and in-situ energy dispersive X-ray spectroscopy, the structure of the n-Si/LiF_x/Al passivating contact was found to consist of an ultrathin continuous layer of LiF_x (~1.5 nm) sandwiched between n-Si and Al with no evidence of intermixing of these two elements. The ρ_c of n-Si/LiF_x/Al contact measured by TLM decreases with LiF_x thickness up to about 1 nm and then increases significantly with thickness from 1.5–2.5 nm [84]. In addition, room temperature ρ_c decreases with the phosphorus concentration in the Si wafer. Similarly, ρ_c for a lightly n-doped Si wafer decreases with temperature from 77 K to about 200 K [84]. These experimental observations suggest that LiF_x forms a continuous interfacial layer between n-Si and Al and prevents the Fermi level pinning effect which can lead to Schottky barrier formation for direct n-Si/Al contacts. Since the LiF_x is an insulator with a band gap of 10 eV [84], the electrons are mainly extracted by a tunneling mechanism. This is supported by the increase in ρ_c for LiF_x thickness from 1.5–2.5 nm. However, direct tunneling through LiF_x is not the only carrier transport mechanism because of the temperature dependence of ρ_c for low temperatures. This trend suggests a thermionic emission process over a small surface energy barrier at the n-Si. The existence of this small surface energy barrier is also supported by the decrease of ρ_c with the dopant surface concentration of the Si wafer. The small surface barrier is thought to be a consequence of the greatly reduced work function (2.8 eV) of LiF_x/Al [84].

In their study, Bullock et al. demonstrated the effectiveness of LiF_x/Al contacts for electron extraction by using a hybrid lightly doped n-Si cell with a partial rear contact (PCR) structure. The PCR structure resembles the PERL structure and was chosen to show that the low ρ_c of LiF_x/Al contacts enables a small contact area to be used for the wafer backside. A hybrid PCR cell utilizing the LiF_x/Al contact and fabricated using n-type float zone Si wafer has a high PCE of 21.5% under standard test conditions [84]. The V_{oc}, J_{sc} and FF are 676 mV, 38.9 mA/cm^2 and 78.3% respectively. The FF value in this work is especially significant because the contact fraction at the back of the solar cell is less than 1%. Note that, due to the dependence of ρ_c on the wafer dopant concentration, the choice of optimum combination of wafer bulk resistivity and ρ_c is not trivial.

4.4. Molybdenum Oxide

Molybdenum oxide (MoO_x) is the most promising dopant-free passivating layer for hole extraction [85]. Using MoO_x a high PCE of 22.5% has been demonstrated in a hybrid device structure [86] The first key property of MoO_x films is their high bandgap. Mallem et al. have made a solar cell by substituting the a-Si:H (p) layer with MoO_x, and the MoO_x film is estimated to have a bandgap of 2.96 eV. This high bandgap is significantly larger than the typical bandgap of the a-Si:H (p) layer (1.7–1.8 eV) and explains why the external quantum efficiency (EQE) of the MoO_x cell is significantly better at the 300–600 nm wavelength range. However, a lower EQE for wavelengths > 600 nm is also recorded, as MoO_x has a higher absorbance in the near-infrared region. Nevertheless, the MoO_x cell recorded a higher short-circuit current density (J_{sc}) of 1.5 mA/cm^2 [87]. Similarly, a simulation done by Gregory et al. showed that an Indium Tin Oxide (ITO)/MoO_x/a-Si:H (i) stack has higher generation current (J_G) than an ITO/a-Si:H (p)/a-Si:H (i) stack (40.1 vs. 39.4 mA/cm^2), which is attributed to the lower parasitic absorption in the MoO_x film [88]. Dreon et al. also found that an MoO_x film 4 nm thick incurs a current loss of close to 0.5 mA/cm^2 from parasitic absorption, which is lower than the current losses observed for a-Si:H (p) layers, which can range up to 2.8 mA/cm^2 [89].

The second key property is its high work function, which leads to significant band bending at the crystalline silicon (c-Si) when it is deposited. Many studies have noted

that a higher work function leads to a larger extent of band bending and better hole-selectivity, resulting in better electrical properties, such as higher open-circuit voltages (V_{oc}) and fill factor (FF), and better passivation, as evidenced by higher minority carrier lifetimes or lower surface recombination velocities (for a cell with no surface recombination occurring, no minority carriers diffuse towards the surface and recombines, and hence has a surface recombination velocity of 0). This idea (and why it may not be true) is further discussed below.

The deposition and annealing of MoO_x at various temperatures has been studied; various studies and experiments have agreed that depositing MoO_x at lower temperatures (less than around 200 °C) leads to more effective passivation. This is because depositing or annealing MoO_x at higher temperatures causes the MoO_x film to become crystalline; specifically, it adopts the structure of the orthorhombic α-MoO_x. A study which modelled the α-MoO_x/Si and β-MoO_x/Si surfaces showed that the interfacial interaction from α-MoO_x is long-ranged, and distorts the structure of silicon close to the surface. This gives rise to more electronic states at the MoO_x/Si surface (i.e., higher probability of recombination), and a worse surface passivation compared to passivation with β-MoO_x, hydrogen (H_2), or oxygen (O_2) [90]. Davis and Strandwitz, in their characterization of MoO_x films, found that MoO_x, when deposited at 300 °C, had the structure of α-MoO_x [91]. Another study found that annealing at 150 °C gives the best passivation; at this temperature and 200 °C, the MoO_x film is amorphous, but when annealing temperature is increased to 250 °C, the MoO_x film becomes crystalline with the orthorhombic structure [92]. The study similarly posits that the crystallinity may be the most important reason for why passivation quality degrades at higher temperatures. Another possible reason is that depositing or annealing at higher temperatures would introduce more O vacancies into the MoO_x bandgap, and lower the band-bending at the c-Si surface; this is the explanation provided by Gregory et al. to explain why the passivation quality of their Si/Al_2O_3/MoO_x cell dropped when it is annealed at 200 °C [88].

The passivating and hole-collecting properties of MoO_x are also affected by the environment in which the annealing takes place; in general it is observed that annealing in O_2 leads to poorer electrical and optical characteristics. Mallem et al. found that annealing in O_2 and H_2 created more oxygen vacancies in the MoO_x film in indium tin oxide (ITO)/MoO_x/a-Si:H (i)/c-Si stacks, and decreased the minority carrier lifetime (i.e., poorer passivation performance), whereas annealing in Argon or ambient air improved the minority carrier lifetime [87]. In addition, the paper showed that the solar cell stacks annealed in O_2 had lower V_{oc} and FF. The authors argued that, with more oxygen vacancies, the work function of the MoO_x layer is reduced, which means less band bending at the c-Si and poorer hole extraction capabilities. A study mentioned previously also similarly showed that annealing in nitrogen (N_2) or forming gas annealing (FGA) with a mixture of 95% N_2 and 5% H_2 gave rise to a higher minority carrier lifetime; the cell annealed in FGA had a lifetime of 201.2 µs, as compared to a lifetime of 158.3 µs for the cell annealed in O_2. Annealing in FGA also increased the implied V_{oc} (i-V_{oc}) from 583 to 603 mV. However, the authors recognize that other papers have demonstrated that annealing in O_2 leads to better passivation [92]. Davis and Strandwitz also notes that annealing in O_2 has been shown to yield more oxidizing MoO_x, and hence a higher work function from a greater extent of band bending [91]. Interestingly, β-$MoO_{2.87}$/Si (which corresponds to 5% oxygen vacancy) is shown to have the lowest concentration of electronic states at the Fermi energy level (even lower than stoichiometric β-MoO_3), implying that a 5% vacancy gives the best passivation effect, and that more oxidized MoO_x may not result in better passivation and cell performance [90].

Recent papers have also investigated the effect of MoO_x thickness on the passivating quality. Dreon et al. have discovered that thinning the MoO_x layer from 9 to 4 nm improved photocurrent greatly, while maintaining a good level of passivation and hole selectivity. Further reducing the thickness of the MoO_x layer improved the current density (except from 1 to 0 nm), as mentioned previously, but passivation and hole selectivity deteriorated:

After the deposition of MoO_x and sputtering of ITO layer onto a-Si:H (i), the minority carrier lifetime of cells with MoO_x layers thinner than 4 nm dropped to 0.01 to 0.2 ms, while cells with thicker MoO_x layers had a lifetime of greater than 1 ms. Furthermore, the work function of the MoO_x films were low; the 2 and 4 nm films were estimated to have a work function of around 5 eV (although the 4 nm films should have a higher work function in reality; the similar figure for 2 and 4 nm films is due to a limitation of the estimating method), which is much lower than typical values of around 6.5 eV, and explains the worsening of the electron-blocking and hole-collecting ability of the contact [89]. Mallem et al. compared the effect of depositing 10 nm MoO_x films with 20 nm films, and concluded as well that the thinner 10 nm films give a higher minority carrier lifetime, as the 20 nm films have higher defect density. They recommend keeping the MoO_x films as thin as possible, until a thin uniform MoO_x layer with fewer defects is formed [87]. Additionally, in their study, Davis and Strandwitz used MoO_x layers of 4 nm, as layers of 10 nm MoO_x in direct contact with silicon yield contact resistivities that were orders of magnitude higher than when 4 nm layers were used [91]. On the other hand, Song et al. observed that for MoO_x/c-Si/MoO_x stacks, the i-V_{oc} rose to a maximum of 630.3 mV as the thickness of the MoO_x layers increased to 15 nm, which means that thicker MoO_x layers (up to 15 nm) may result in better hole selectivity and electrical properties [93].

Despite the strengths of MoO_x as a passivating and hole-selective layer, many studies agree that solar cells with MoO_x layers are unstable; the optical and electrical properties of these cells degrade upon leaving them in ambient air for an extended period of time, as air exposure causes additional oxygen vacancies. Mallem et al. stored two cells with a deposited MoO_x layer in two different conditions for 5–6 months: one was stored in a glove box, while the other was exposed to air. The MoO_x layer of the cell exposed to air had a much higher ratio of Mo^{5+}: Mo^{6+} due to the increase in oxygen vacancies, while the MoO_x layer deposited using the sample stored in the glove box had no oxygen deficiency. The additional oxygen vacancies reduced the MoO_x work function, and increased series resistance, resulting in lower V_{oc} (695 mV for glove-box stored vs. 650 mV for air-exposed), J_{sc} (38.88 vs. 38.7 mA/cm^2), FF (74% vs. 69%), and efficiency (20.0% vs. 17.35%) [87]. Also, Jun Chen et al. observed that the effective minority carrier lifetime of their MoO_x films decreased from 180.2 to 59.6 μs after being left in an ambient environment of around 30% humidity for 48 h, showing that the passivation quality of MoO_x drops significantly as well if it is exposed to air for a prolonged period of time [92]. To improve the stability of MoO_x/Si solar cells, Cao et al. suggest using SiO_x and V_2O_x in a Si/SiO_x/MoO_x/V_2O_x/ITO/Ag cell structure. The SiO_x layer reduces the number of oxygen vacancies in MoO_x, thereby increasing the work function of the MoO_x layer and improving its hole selectivity. It also has the secondary benefit of reducing the parasitic absorption experienced in the infrared region. The V_2O_x layer shields the MoO_x layer from ITO sputtering damage and air exposure, and depletes electrons on the right side of the MoO_x film, leading to a favourable path for electrons to reach the Si/MoO_x interface. Thus, cells with V_2O_x have a stronger hole selectivity, and higher V_{oc} and FF. More significantly, the solar cells achieved a power conversion efficiency (PCE) of 20.0%, and maintained more than 98% of their initial PCE after 2 weeks of ambient air exposure (humidity was around 80%) [94]. Jingye et al. tried counteracting this issue by including a CrO_x layer between the MoO_x and Ag layers in the cell, and they found that the control c-Si/MoO_x/Ag cell experienced a fall in PCE from 15.86% to 10.20% only after 2 days of storage in air, while the cell with CrO_x (c-Si/MoO_x/CrO_x/Ag structure) saw a 0.3% increase in PCE after 8 months, after a minor decrease in PCE in the first few days [95].

One key area which is not well understood is the mechanism behind how MoO_x acts as such an efficient hole-selective and passivating layer. In an attempt to understand this, Bhatia et al. have constructed a few models, and fit each of them against the observations in the literature. They conclude that a model whereby electron transfer from c-Si (n) to the MoO_x side is over the barrier, hole extraction through either interface recombination or tunneling is allowed and (negative) interface charge is present is the best for explaining the

observed J-V characteristics of MoO_x/Si cells (Figure 9) [96]. The band bending at the c-Si (n) is explained by this interface charge, and not merely due to MoO_x's large work function. Numerical simulations show that increase in the concentration of interface charge increases V_{oc} and efficiency significantly, whereas increasing the MoO_x work function from 5.1 to 5.6 eV (and keeping electron affinity constant) did not improve the electrical properties of the MoO_x/Si cell. This somewhat contradicts many of the other studies which have explained improvements in electrical properties by a larger work function, and vice versa. One possibility for this discrepancy might be that the work function variation (5.1 vs. 5.6 eV) is not significant enough for changes to be observed. However, other studies are in agreement with this model regarding the mechanisms for hole extraction. Singh et al. demonstrated that, for MoO_x films with a work function >6 eV, the primary mechanism of hole extraction is through band-to-band tunneling. For MoO_x films with a work function between 5 and 6 eV, carrier transport occurs through trap states in the MoO_x bandgap. For films with work function <5 eV, a hole transport barrier which worsens the hole selectivity of the MoO_x film is seen [97].

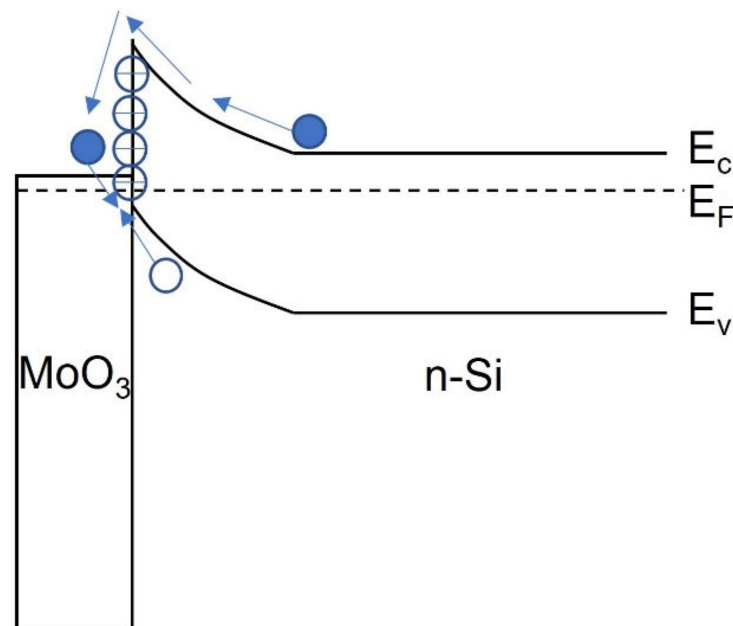

Figure 9. Hole selectivity mechanism of the MoO_3/n-Si passivating contact involving electron excitation over barrier, negative fixed charge and recombination with holes.

4.5. Other Metal Oxides

For completeness, we discuss briefly several other TMOs that have shown potential as passivating contacts in c-Si solar cells. Vanadium oxide (V_2O_x) and tungsten oxide (WO_x) have material properties similar to MoO_x and can be used as hole-selective contacts. Both TMOs are wide band gap, n-type semiconductors [98]. The band gaps for V_2O_x and WO_x after exposure in air are 3.6 eV and 3.1 eV respectively. Like, MoO_x, these TMOs have low Fermi levels. For V_2O_x, the work function (after exposure in air) is 5.3 eV while that for WO_x is 5.0 eV [98]. Using thermally evaporated V_2O_x and WO_x films with a thickness of 15 nm, Gerling et al. fabricated DHJ c-Si solar cells with the generic structure Ag/ITO/V_2O_x o_x/n-Si/a-SiC_x:H/a-Si:H(n)/a-SiC_x:H/Ti [98]. Under 1 sun illumination, the device with V_2O_x hole contact has a measured PCE of 15.7%. This is higher than the PCE (=12.5%) of the WO_x device. For comparison, Gerling et al. also fabricated a device with MoO_x as the hole contact which showed a PCE of 13.6% at 1 sun. Thus, for this study, the best performing hole-selective contact material is V_2O_x. As a result of their wider band gaps, c-Si solar cells with V_2O_x, WO_x and MoO_x hole contacts all have improved EQE spectral

response at the shorter wavelengths (300–550 nm) relative to a-Si:H. This is because of less parasitic absorption in the TMO hole contacts.

Two other emerging TMOs for passivating contacts worth highlighting are nitrogen doped copper oxide (CuO_x:N) [99] and niobium oxide (Nb_2O_5) [100]. CuO_x:N is an extrinsic p-type hole-selective contact material that can be deposited by reactive sputtering using a Cu target and an $Ar/O_2/N_2$ plasma [99]. When deposited onto p-Si, CuO_x:N forms an ohmic contact with a ρ_c between 10–1000 mΩcm^2 [99].

Nb_2O_5 has properties akin to TiO_x and is therefore a n-type electron-selective passivating contact material. Macco et al. deposited Nb_2O_5 onto Si by thermal ALD from an organometallic Nb precursor and water [100]. The ρ_c of ALD Nb_2O_5 films was characterized by the method of Cox and Strack. The contact resistivity after forming gas anneal ranged between 0.1–1 Ωcm^2 depending on film thickness. Thus far, neither CuO_x:N nor Nb_2O_5 have been integrated into c-Si solar cells.

One other metal oxide with potential as a passivating contact is lanthanum oxide (LaO_x) deposited by physical vapor deposition. LaO_x is a high dielectric constant (k) insulator that had been used for reducing the parasitic source drain resistance in silicon metal oxide semiconductor field effect transistors [101]. Upon deposition of ~1 nm LaO_x onto thin SiO_2, an interface dipole is formed due to difference in areal oxygen density between the high-k dielectric and SiO_2 [102]. The potential offset due to this dipole layer allows the Schottky barrier height (Φ_{SBH}) for a TaN/Si junction to be tuned [101]. For n-Si (p-Si) substrates, a minimum Φ_{SBH} of 20 meV (100 meV) was measured at optimal LaO_x thickness. Similar dipole effects have also been observed in terbium- and aluminum oxide-based interface layers [103]. Since this Φ_{SBH} tuning effect involves ultrathin SiO_2, it should be applicable to c-Si solar cells as passivating contacts.

4.6. Organic Passivating Contacts

The conjugated (conducting) polymer poly(3,4-ethylenedioxythiophene) poly (styerenesulfonate) (PEDOT:PSS) is a widely used transparent p-type contact material for both OLEDs and organic solar cells [73]. Its optical band gap, which is the energy difference between the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), is about 1.6 eV [73]. Unlike inorganic transparent conducting oxides such as ITO, PEDOT:PSS can be easily spin coated onto a substrate from a dispersion of PEDOT and PSS in a polar organic solvent such as isopropanol. The PSS counterion serves as a dopant that induces holes in the PEDOT chain by electron transfer from the PEDOT. Although PEDOT:PSS is quite stable in air, PEDOT:PSS films are known to react with ITO in a corrosion-type process [73].

Nagamatsu et al. demonstrated the first silicon organic heterojunction (SOH) solar cell using PEDOT:PSS as an electron blocking passivating layer [104]. Their device had a simple structure and can be fabricated by straightforward solution spin coating at <100 °C. The device structure consists of Ag/PEDOT:PSS/n-Si/Al. Under illumination from the PEDOT:PSS side, electrons are prevented from reaching the Ag electrodes by the layer of PEDOT:PSS because of the large LUMO-E_c offset between Si and PEDOT:PSS. This prevents the photo-generated electrons from reaching the Ag electrodes where recombination may occur. On the other hand, the small offset between the HOMO of PEDOT:PSS and E_v of Si facilitates hole extraction. For 1 sun AM1.5 illumination, a PCE of 11.5% was observed for this SOH solar cell [104].

A double heterojunction c-Si solar cell with a hole-selective PEDOT:PSS/Si contact and a higher PCE was reported by Gogolin et al. in 2017 [105]. The device studied by this group has the structure Ag/ITO/a-Si:H(i)/a-Si:H(n)/p-Si(CZ)/PEDOT:PSS/ITO/Ag. The electron-selective contact on the sunward side is based on a SHJ and the a-Si:H(i)/a-Si:H(n) bilayer of the SHJ was deposited onto textured Si to enhance light trapping in the absorber. Since the SHJ is used, the screen-printed Ag top electrodes had to be cured at a lower temperature of 190 °C [105]. Under illumination with a 2 cm × 2 cm shadow mask, the three fabricated devices had a measured PCE of ~16.1% with V_{oc} in the range of 675–680 mV.

The J_{sc} and FF are ~ 31.8 mAcm^{-2} and ~74.3% respectively. The V_{oc} obtained in this work is higher than the V_{oc} = 663 mV for an earlier hybrid PEDOT:PSS c-Si solar cell reported by the same group. Since the SHJ is known to be an excellent passivating contact, the high measured V_{oc} demonstrates that PEDOT:PSS can form a good full area passivating contact with p-Si. This conclusion is supported by additional carrier lifetime measurements [105]. However, the precise passivation mechanism of Si by PEDOT:PSS remains to be identified.

In subsequent work by the same group, Zielke et al. demonstrated a larger (15.6 × 15.6 cm^2) full area hybrid c-Si solar cell with a PEDOT:PSS back contact [106]. A low-temperature metal paste used to metallize the PEDOT:PSS contact layer was found to have no adverse effect on the passivation of the back side of the wafer. The sunward top surface of this cell has a conventional phosphorus diffused homojunction. By using an optimized set-peak firing temperature for the Ag paste of the front electrodes, a high PCE of 20.2% for the champion cell was obtained [106]. Parasitic absorption of incident longer wavelength sunlight was shown to be a main loss mechanism for this device.

5. DHJ c-Si Solar Cells

By using dopant-free passivating contacts for both the front and rear contacts of a c-Si absorber, DHJ or DASH solar cells as originally proposed by Yablonovitch can be fabricated with simpler processing and at lower thermal budget. An early example of this is a Ag/PEDOT:PSS/n-Si/TiO_2/Al/Ag device fabricated by Nagamatsu et al. [107]. The n-Si absorber is a 300 µm FZ wafer. The spin-coated PEDOT:PSS had additional dopants and additives to enhance, respectively, the conductivity and adhesion to n-Si. The TiO_2 back contact was deposited by the modified CVD process mentioned in Section 4.1 at 100 °C. As discussed in Section 4.6, the PEDOT:PSS/Si contact is electron blocking because of a 0.5 eV energy difference between the LUMO of PEDOT:PSS and the E_c of Si. The TiO_2/Si contact, on the other hand, is hole blocking because of a large 2.3 eV offset between the E_v of Si and the E_v of TiO_2 (Figure 10). The DHJ structure reduces the forward-bias dark current compared with a PEDOT:PSS/n-Si/metal device because of minority carrier blockage. Under illumination, the DHJ structure has a PCE of 11.2% which is higher than the single HJ device (10.3%). The difference is mainly due to reduced recombination at the TiO_2/Si back interface and is evidenced by a V_{oc} improvement of 31 mV.

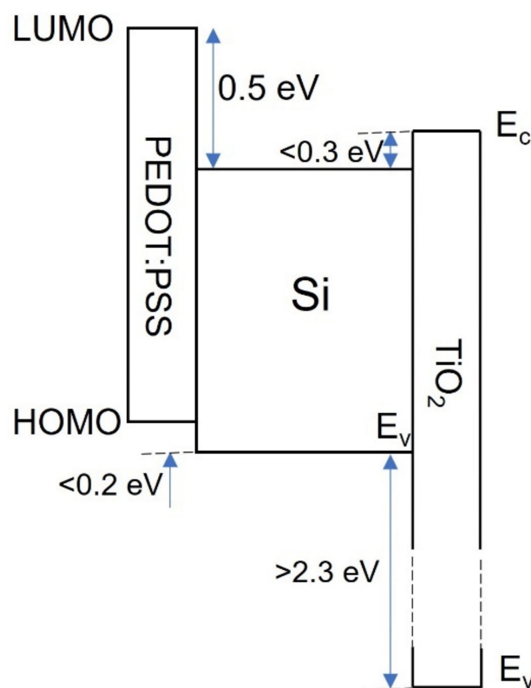

Figure 10. Schematic energy diagram of the PEDOT:PSS/Si/TiO_2 DHJ solar cell.

The acronym DASH was first used for naming a DHJ cell fabricated by Bullock et al. [108]. This n-type cell was textured on both sides of the c-Si wafer by anisotropic wet etching to increase light coupling and trapping. The hole-selective contact consists of a:Si-H(i)/MoO_x while the electron-selective contact is a:Si-H(i)/LiF_x. The fabrication process is straightforward, with just seven processing steps carried out at ambient temperature. The deposition steps include thermal evaporation, sputtering, screen-printing and PECVD. An a-Si:H layer had to be deposited first because the dopant-free passivating layers do not have adequate passivation capability as discussed below. Under illumination, the champion cell with this structure had a V_{oc} of 716 mV, J_{sc} of 37.07 $mAcm^{-2}$, FF of 73.15% and PCE of 19.4%. The efficiency of this device is limited by backside reflection and parasitic series resistance.

Another n-type DASH solar cell with an IBC device structure was fabricated by Wu et al. in 2018 [109]. The SiN_x and MgF_x double antireflection coating on the sunward side of the device were deposited by PECVD and thermal evaporation respectively. For the IBC, MoO_x was used for the hole-selective contact while MgF_x, MgO, LiF_x, Ca and Mg were investigated. It was found that, amongst these five electron-selective contacts, MgF_x resulted in the highest device PCE. The PCE depends strongly on the MgF_x thickness and the interdigitated contacted fraction area (f_{ICA}). For optimized MgF_x thickness f_{ICA}, a high PCE of 22.2% was obtained [109]. One important point to note for this work is that prior to depositing the IBC, a 5 nm layer of PECVD a-Si:H was deposited onto the FZ n-Si wafer to improve passivation.

In 2019, Nayak et al. reported an interesting DASH solar cell with the device structure: Ag/ITO/MoO_x/n-Si/LiF/Al [110]. The Ag, MoO_x, LiF and Al thin films were deposited by thermal evaporation while the ITO was deposited by RF magnetron sputtering. All processing steps could be carried out at ambient temperature because no Si-based auxiliary contact layers were used. Under illumination, this device showed a V_{oc} of 570 mV, J_{sc} of 35.6 $mAcm^{-2}$, FF of 75.02% and PCE of 15.35%. To better understand the cause of the low V_{oc}, capacitance-voltage (C-V) and temperature dependent admittance spectroscopy were performed to characterize the defects at the MoO_x/Si interface. Using the parallel conductance method of Nicollian and Goetzberger, the density of interface defect states D_{it} at the MoO_x/Si interface was found to be of order 10^{12} eV^{-1} cm^2 which is rather high [110]. The D_{it} has the expected negative correlation with the V_{oc} of the fabricated devices; that is, the device with the highest V_{oc} has the lowest D_{it}. A high D_{it} also reduces the built-in potential V_{bi} measured by C-V method. The electrical characterization of this study shows that the passivation of the MoO_x needs to be further improved.

Finally, a high efficiency, thermally stable DASH cell was reported by Bullock et al. in 2018 [111]. This device utilized an improved electron-selective contact comprising two dopant-free passivating films namely, TiO_x and LiF. The device has the structure: ITO/MoO_x/a-Si:H/n-Si/a-Si:H/TiO_x/LiF/Al. The ALD deposited TiO_x has two functions. First, as mentioned earlier, the small conduction band offset between TiO_x and Si facilitates electron extraction from the Si. The second function is to act as a protective layer to prevent intermixing between the a-Si:H and the sub-nanometer thick LiF/Al layer during thermal annealing which can lead to Al induced crystallization of the a-Si:H [111]. Under 1 sun illumination, the device by Bullock et al. showed a champion PCE of 20.7% with V_{oc} of 706 mV, J_{sc} of 38.4 $mAcm^{-2}$ and FF of 76.2% (Figure 11). Significantly, in a damp heat test (85 °C, 85% RH, 1000 h), an unencapsulated device showed a small 3% relative drop in PCE. This demonstrates the thermal robustness of the improved electron-selective contact.

Table 1 summarizes the PV performance and the carrier selective contacts used for recent high efficiency c-Si solar cells reviewed in this article. At present, the best performing c-Si solar cells make use of the SHJ and the POLO (TOPCon) contacts for carrier extraction. For the highest PCE, an IBC structure is necessary. In addition, both SHJ and POLO contacts have demonstrated compatibility with manufacturing processes. Since the dopant-free passivating contacts are still under development, they typically require an auxiliary passivating layer of SiO_x or undoped a-Si:H for adequate passivation. Amongst the DHJ

devices with dopant-free passivating contacts, the highest PCE so far is 22%. This device has the IBC structure and requires a-Si:H to supplement both the MgF_x and MoO_x passivating contacts. The DASH device PCE is, however, much lower if silicon-based passivation layer is not included.

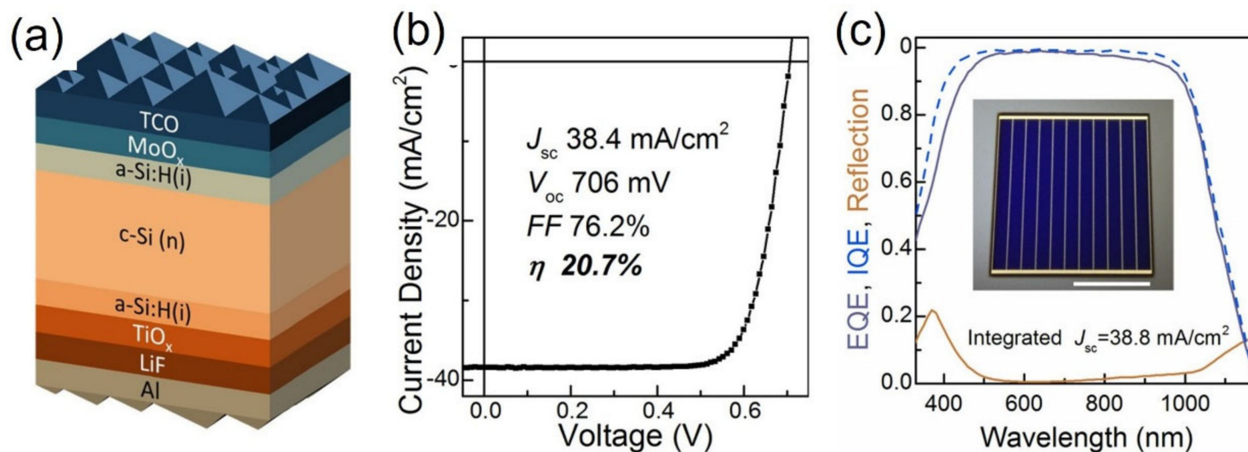

Figure 11. (**a**) Schematic diagram of DASH cell with a−Si:H(i)/MoO_x hole-selective contact and a−Si:H(i)/TiO_x/LiF electron−selective contact; (**b**) current density−voltage characteristics under illumination of champion cell; (**c**) internal, external quantum efficiency and reflection spectra of devices (Reprinted with permission from Ref. [111] ACS Energy Lett. 2018, 3, 508−513. 2018 American Chemical Society).

Table 1. PCE of recent high-performance c-Si solar cells with passivating contacts.

Electron-Selective Contact	Hole-Selective Contact	PCE (%)	Reference
SHJ	SHJ	24.7	[44]
SHJ	SHJ	25.6	[33]
SHJ	SHJ	26.3 [1]	[45]
POLO	p^+ diffusion	21.7	[53]
POLO	POLO	24.4	[56]
POLO	p^+ diffusion	25.7	[57]
POLO	POLO	23.0 [1]	[58]
POLO	POLO	26.1 [1]	[59]
POLO	p^+ diffusion	23.22	[64]
POLO	p^+ diffusion	23.57	[65]
POLO	p^+ diffusion	24.58	[66]
TiO_2	p^+ diffusion	19.8	[79]
SiO_2/TiO_2	p^+ diffusion	21.6	[79]
SiO_2/TiO_2	p^+ diffusion	22.1	[37]
MgO_x	p^+ diffusion	20.0	[82]
LiF_x	p^+ diffusion	20.6	[84]
SHJ	MoO_x	22.5	[86]
Al	PEDOT:PSS	11.7	[104]
SHJ	PEDOT:PSS	16.2	[105]
n^+ diffusion	PEDOT:PSS	20.2	[106]
TiO_2	PEDOT:PSS	11.2	[107]
a-Si:H(i)/LiF_x	a-Si:H(i)/MoO_x	19.42	[108]
a-Si:H/MgF_x	a-Si:H(i)/MoO_x	22.2 [1]	[109]
LiF_x	MoO_x	15.35	[110]
a-Si:H/TiO_x/LiF	a-Si:H/MoO_x	20.7	[111]

[1] IBC structure.

Table 2 below summarizes the four sections on carrier-selective contacts that have been discussed in this article.

Table 2. Section summary.

Section	Section Title	Summary
2	Diffused junction	• Thermal diffusion into c-Si (emitter, BSF) by furnace • High thermal budget • Carrier selection by field effect • c-Si surface not passivated • Emitter concentration Auger limited
3.1	Silicon heterojunction	• PECVD a-Si:H(i), doped a-Si:H • Deposition requires cluster tool • Use highly toxic gases; additional safety equipment mandatory • Low-temperature backend processes • c-Si passivated by a-Si:H • Carrier selectivity due to field effect and asymmetric band offsets in SHJ
3.2	Polysilicon on oxide	• Thermal or wet chemical oxidation • PECVD a-Si:H, n-, p-type doping • Requires thermal annealing for activation and polysilicon formation • High thermal budget; annealing may result in discontinuities in SiO_x • c-Si passivated by ultrathin SiO_x • Current localized at thinned SiO_x or pinholes
4	Dopant-free passivating contacts	• Thermal evaporation, ALD, modified CVD, solution spin coating • Processing at ambient temperature • Wide choice of inorganic and organic thin film materials • Lower PCE than SHJ and POLO if deposited directly onto c-Si
5	DHJ c-Si solar cells	• Carriers selected by asymmetric band offsets ΔE_c, ΔE_v • Needs auxiliary Si based passivation layer for higher efficiency • IBC structure yields the highest PCE

6. Challenges and Outlook

Si based passivating contacts (SHJ, POLO) have enabled c-Si solar cells with the highest PCE to be fabricated. This is due to the reduction in SRH recombination at the carrier extraction contacts. For the emerging dopant-free passivating contacts, the highest PCE reported thus far is 22.2% [109]. Although this is ~4% (absolute) lower than the best SHJ and POLO devices, there are many advantages in using these non-Si passivating contacts. These include a broader choice of thin film materials, deposition using lower cost equipment at ambient conditions, thermal stability and greatly reduced parasitic absorption due to their wide band gap.

Amongst the remaining technical challenges, the main hurdle for the dopant-free passivating contacts is improvement of the c-Si surface passivation so that SiO_2 or a-Si:H(i) passivation layers are no longer required. To achieve this, fundamental studies of the passivation mechanism of the c-Si surface by a given dopant-free contact material and the band offsets (ΔE_c and ΔE_v) with respect to c-Si will need to be conducted [72]. The interfacial electronic structure of c-Si can be probed using photoelectron spectroscopy [112]. This knowledge may result in high efficiency DASH cells.

The environmental stability of DASH solar cells is another critical topic of investigation. Thus far, except for ref. [111], the effect of elevated temperature and humidity on the passivating thin film material are rarely reported. Cell lifetime and degradation mechanisms are, however, crucial to commercial deployment. The TMOs used in DASH cells now

are usually deposited by thermal evaporation. Lower cost solution (sol-gel) deposition processes of MoO_x, V_2O_x and WO_x on c-Si has recently been explored in some detail [113]. However, for the same TMO, the PCE of the solution processed Si heterojunction solar cell is usually lower than cells fabricated by thermal evaporation.

Since the deposition processes for the dopant-free passivating contacts in DASH cells are also used for thin film solar cells and organic photovoltaics, one can anticipate a long-term convergence in the fabrication processes for these devices. This can facilitate the integration of c-Si cells with for example perovskite solar cells into tandem cells [17]. With the reduction in fabrication cost, the market dominance of c-Si cells may become even more entrenched in future.

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