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The Effect of a Dual-Layer Coating for High-Capacity Silicon/Graphite Negative Electrodes on the Electrochemical Performance of Lithium-Ion Batteries

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Abstract: Silicon-based electrodes offer a high theoretical capacity and a low cost, making them a promising option for next-generation lithium-ion batteries. However, their practical use is limited due to significant volume changes during charge/discharge cycles, which negatively impact electrochemical performance. This study proposes a practical method to increase silicon content in lithium-ion batteries with minimal changes to the manufacturing process by using dual-layer electrodes (DLEs). These DLEs are fabricated with two slurries containing silicon and graphite as active materials. Notably, the electrode with the silicon as the outermost layer on top of the graphite layer (Si-on-top) demonstrated a superior initial capacity of 935 mAh/g and retained 70% of its capacity (537 mAh/g) after 100 cycles at 0.5 C. In contrast, a single-layered electrode (SLE) with a silicon-graphite mixture retained only 50.3% of its capacity (370 mAh/g) under the same conditions. These findings suggest that DLEs, particularly with the silicon layer located on top, effectively increase silicon content in the negative electrode while remaining compatible with existing manufacturing processes. This approach offers a realistic strategy for enhancing the performance of lithium-ion batteries without significant process modifications.



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Keywords: lithium-ion battery; silicon/graphite electrode; dual-layer electrode; active material arrangement; electrochemical performance; cycle stability; electrode fabrication process

1. Introduction

Lithium-ion batteries (LIBs) have become indispensable to meet the energy storage requirements of modern society and industry, and have been the main technology enabler driving the widespread adoption of a variety of electronic devices, electric vehicles (EVs), and energy storage systems (ESSs). The advantages of LIBs, including their high energy density, long cycle life, and relatively low self-discharge rates, have propelled their adoption and have sustained a continuous trend of technological advancement and market expansion. In fact, the market for lithium-ion batteries has been expanding at an unprecedented rate. According to recent market analyses, the global market size for LIBs was valued at USD 46.2 billion in 2022, and the LIB industry is projected to reach USD 189.4 billion by 2032, a compound annual growth rate of 15.2% from 2023 to 2032 [1]. Despite their widespread use and numerous advantages, commercialized LIBs still present several challenges, including meeting the growing demand to further increase their energy and power density, decrease their capacity degradation, and lower their cost.

Attempts to overcome the less than satisfactory energy density have generally involved increasing the electrode density by increasing the loading level [2,3]. However, this strategy has limitations. As the electrode density and loading level increase, the flexibility of the electrode decreases [4]. Consequently, the roll-to-roll manufacturing process needs to slow down. Additionally, the increased density and loading level can lead to the destruction of active material and the development of cracks in the electrode components, ultimately

affecting the electrochemical performance adversely [5]. To meet the market demand, the focus has shifted towards the development of new materials with a high capacity. In the case of positive electrodes, lithium nickel cobalt manganese oxide (NCM) has been widely adopted. Since the nickel (Ni) content is the primary contributor to the capacity in NCM positive electrodes, extensive research is currently underway to raise the Ni content of NCM materials (known as high-Ni NCM) [6,7]. Regarding negative electrode materials, silicon (Si) is the most actively researched material to meet these requirements. With a theoretical capacity of 4200 mAh/g, Si can achieve more than ten times the energy density of conventional graphite (Gr), which has a capacity of 372 mAh/g [8,9]. Despite the high capacity of Si, it also undergoes volume changes of up to 300% during the lithiation and delithiation processes. This significant volume change gives rise to the formation of an unstable solid electrolyte interphase (SEI) and pulverization, which leads to structural damage, permanent capacity losses, and low cycling efficiency [10]. Additionally, the low lithium diffusion in and poor electrical conductivity of silicon both limit its rate performance and prevent its capacity from being fully exploited [11]. These issues impose limitations on the extent to which the proportion of Si in negative electrodes can be increased.

Generally known research approaches to address the aforementioned challenges have included the nanonization of silicon [12], coating the silicon surface with carbon or ceramic material [13,14], developing conductive additives [15], and using binders to enhance the rigidity [16]. Liang et al. designed a hydrothermally prepared porous nano-silicon material capable of sustained cycling [12]. Fan et al. improved the cyclability by synthesizing carbon-coated silicon from poly-peri-naphthalene [13]. Dou et al. designed a silicon negative electrode with low volume expansion and high ionic and electrical conductivity by applying a hybrid coating consisting of carbon and titanium oxide [14]. Tsai et al. employed long-length carbon nanotubes as conductive materials to stabilize the cycling performance of high-energy density LIBs [15]. Parikh et al. investigated the use of poly(acrylic acid) as a binder to improve the capacity retention of the silicon negative electrode [16]. Although these efforts have yielded positive outcomes, these conventional approaches require substantial changes to current manufacturing processes, which make large-scale production challenging. Consequently, a novel type of electrode, the dual-layer electrode (DLE), has emerged with the aim of enhancing electrochemical performance while keeping changes to the existing manufacturing processes to a minimum. The DLE is composed of two separate layers, each of which is fabricated using two separately prepared slurries. The advantage of this design is that slurries with different compositions in terms of the binders, solid contents, and active materials can all be used to fabricate a DLE.

Prior studies of DLEs have targeted specific goals and demonstrated notable results. For instance, Chu et al. designed a two-layered positive electrode with high-energy active materials to increase the discharge capacity at high C-rates [17]. Imachi et al. designed a two-layered positive electrode, with the upper layer containing a high-energy active material, and the lower layer comprising a safety active material [18,19]. Zhang et al. developed a flexible silicon/carbon two-layered negative electrode using microelectronic printing technology to markedly improve the stability and performance of LIBs by addressing the conductivity and volume expansion issues presented by Si [20]. Liu et al. mitigated the degradation of the battery performance due to binder migration by changing the content of the binder used in the upper and lower layers [21]. Nonetheless, studies on the order in which the different layers are arranged on the DLE to investigate the effect of the location of the active material on the negative electrode have not yet been reported.

In this study, we fabricated two DLEs and investigated the dependence of the electrochemical performance on the location of the silicon layer in the electrodes in comparison to electrodes without the dual layer (single-layered electrodes (SLEs)). This enabled the extent to which the position of the silicon-containing layer affected the electrochemical performance to be confirmed. Particularly, the capacity retention of the cell operated with the DLE with the silicon located in the top layer (Si-on-top DLE) was 70% after 100 cycles at 0.5 C, which exceeded that of the SLE cell by 20%. In addition, the silicon-on-top DLE

also had the lowest charge transfer resistance (41.8Ω) and the highest lithium-ion diffusion coefficient ($2.02 \times 10^{-14} \text{ cm}^2/\text{s}$) in the 100% state of charge (SOC), which indicated improved ionic and electronic transport. Based thereupon, the use of a DLE can be considered a promising practical approach to enhance the electrochemical performance of high-content silicon electrodes, an approach that obviates the need for substantial modifications to the battery manufacturing process.

2. Materials and Methods

2.1. Materials

A Si alloy with a capacity of 1250 mAh/g and a D50 diameter of $2.46 \mu\text{m}$ was obtained from MK Electron (Yongin, Republic of Korea), artificial graphite with a capacity of 350 mAh/g and a D50 diameter of $23.6 \mu\text{m}$ was purchased from Showa Denko (SCMGTM-BH, Tokyo, Japan), Super P was purchased from IMERYS (SUPER P LI, Paris, France), carboxymethyl cellulose (CMC) was obtained from GL Chem (MicellCMC[®] GB-S01, Chungju, Republic of Korea), styrene-butadiene rubber (SBR) was purchased from Zeon (BM-451B, Tokyo, Japan), and the separator was purchased from Celgard (Celgard[®] 2400 monolayer, Tokyo, Japan).

2.2. Construction of Dual-Layer Electrode

The slurry that was prepared contained the active material, binder, and conductive material in the weight ratio of 80:10:10. The reference electrode contained silicon and graphite as the active materials in the weight ratio of 1:1 and the DLE contained either silicon or graphite as the active material. CMC and SBR in a weight ratio of 2:3 were added as the binder. Each of the slurries contained Super P as the conductive material. For the SLE, the prepared slurry was applied to $10 \mu\text{m}$ thick copper foil with an applicator at a loading level of $3 \text{ mg}/\text{cm}^2$, and for the DLE, the silicon and graphite layers, respectively, were each applied to copper foil at a loading level of $1.5 \text{ mg}/\text{cm}^2$ for a total loading level of $3 \text{ mg}/\text{cm}^2$ and a loading capacity of 3.07 mAh for each electrode. The total electrode density was set to $1.5 \text{ g}/\text{cm}^3$.

2.3. Coin Cell Assembly

The prepared electrodes (diameter: 16 mm) were assembled into half-cells using a CR-2032 coin-type cell kit. A $25 \mu\text{m}$ thick separator was used and a 1 mm thick lithium metal sheet was used as the counter electrode. The electrolyte solution had the following composition: LiPF_6 (1M) solution in ethylene carbonate (EC), ethyl methyl carbonate (EMC), and fluoroethylene carbonate (FEC) in the ratio of 25: 70: 5 ($v/v/v$), to which vinylene carbonate (VC) 0.5 wt.% was added. The assembly process was carried out in a glove box under an argon atmosphere.

2.4. Electrochemical Analysis

Formation cycles were initially performed. The cells were operated for three cycles with lithiation at the rate of 0.1 C in constant current-constant voltage mode (CC-CV with a current cut-off limit of 0.005 C) and delithiation at 0.1 C in the voltage range 0.01–3.0 V to form stable SEI layers. Electrochemical impedance spectroscopy (EIS) measurements were conducted by using a potentiostat (SP-150e, BioLogic, Seyssinet-Pariset, France) in the fully delithiated state before formation and in the fully lithiated state after the formation process, followed by a one-hour rest period to reach equilibrium after full lithiation. A frequency range of 100 kHz to 100 mHz (with readings recorded at 6 points per decade) was applied with a 10 mV amplitude.

Equation (1) expresses the real part of the impedance (Z_{real}) in terms of the bulk resistance (R_b), charge transfer resistance (R_{ct}), and Warburg impedance (Z_W). In the high-frequency range, the values of R_{ct} and Z_W converge to zero, allowing the value of R_b to be determined [22]. In the mid-frequency range, the Z_W value can be still ignored, which enables the calculation of the R_{ct} value using the previously obtained R_b value. In the

low-frequency range, the values of R_b and R_{ct} are negligibly small compared to the Z_W value, thus allowing the Z_W value to be extracted.

$$Z_{real} = R_b + R_{ct} + Z_W \quad (1)$$

Then, using the frequency value at a specific point, it is possible to calculate the value of the double-layer capacitance (C_{dl}) by Equation (2).

$$C_{dl} = \frac{1}{2\pi f R_{ct}} \quad (2)$$

Furthermore, it is possible to calculate the Warburg coefficient (σ) by using Z_W in Equation (3), where ω is the angular frequency.

$$Z_W = \sigma \left(\frac{1-j}{\sqrt{\omega}} \right) \quad (3)$$

By using σ , it is possible to derive the Li-ion diffusion coefficient (D_{Li}) using Equation (4), where R is the gas constant (8.314 J/mol); T is absolute temperature (298 K); A is the surface area of the electrode (1.538 cm²); n is number of electrons ($n = 2.38$, Si: 3.75, Gr: 1); F is the Faraday constant (96,845 C/mol); and C is the Li-ion concentration (1 mol/L) [22].

$$D_{Li} = \frac{R^2 T^2}{2A^2 n^4 F^4 C^2 \sigma^2} \quad (4)$$

All the calculated results are summarized in the tables.

Cyclability tests were performed at a current rate of 0.5 C in CC-CV mode for lithiation and in CC mode for delithiation, with a current cut-off rate of 0.005 C in the voltage range of 0.01–3 V for 100 cycles. The rate capability was measured at various current levels to assess the kinetics of the fabricated electrodes. Lithiation was carried out in CC-CV mode at the rates 0.2, 0.33, 0.5, 1, 2, 3, and 5 C in CC mode (current limit: 0.005 C) at the constant voltage of 0.01 V. Then, delithiation was carried out in CC mode at the same current rate with lithiation to the voltage cut-off limit of 3.0 V. In addition, the delithiation step at each C-rate was followed by delithiation at 0.2 C to ensure full delithiation. Each lithiation and delithiation step was followed by a 30 min rest period. Five cycles were used at each C-rate to obtain regular capacities.

2.5. Characterizations

Scanning electron microscopy (SEM) (SU8230, Hitachi, Japan) and energy-dispersive X-ray spectroscopy (EDX) (Ultim[®] Max, Oxford, UK) were used to investigate the morphology of the prepared samples. The interfacial resistance between the current collector and the electrode material was probed by an electrode resistance measurement system (RM2610, HIOKI, Nagano, Japan). The galvanostatic charge/discharge (GCD) curves were recorded and the cycling performance of the assembled cells was tested on a battery testing system (NEWARE, MIHW-200-160CH, Shenzhen, China).

3. Results and Discussion

Figure 1 shows a schematic illustration of the structural layer arrangements of the SLE and DLEs. The intended samples were fabricated by preparing three distinct slurries. The weight ratio of the active material, conductive material, and binder was maintained constant at 80:10:10 for all of these slurries, but the composition the active material of the respective slurries was designed to be different and comprised a mixture of silicon and graphite, silicon alone, and graphite alone, respectively. In the case of the mixed slurry, the ratio of silicon to graphite was 1:1 by weight. The final solid content of each slurry was equal at 40 wt.%. The electrodes were prepared by applying a slurry of the bottom layer and allowing this layer to completely dry in air under ambient conditions, before the

top layer was applied to cover the bottom layer. The loading level of the three prepared electrodes was set to 3 g/cm^2 . The DLE consisted of two separate layers with different active materials, Si and graphite, with a 1.5 g/cm^2 loading level. As the area of each electrode was 1.54 cm^2 , the theoretical loading capacity of the electrodes was designed as 3.07 mAh . The completely dried electrodes were then pressed by roll press to comply with the density requirement of 1.5 g/cc .

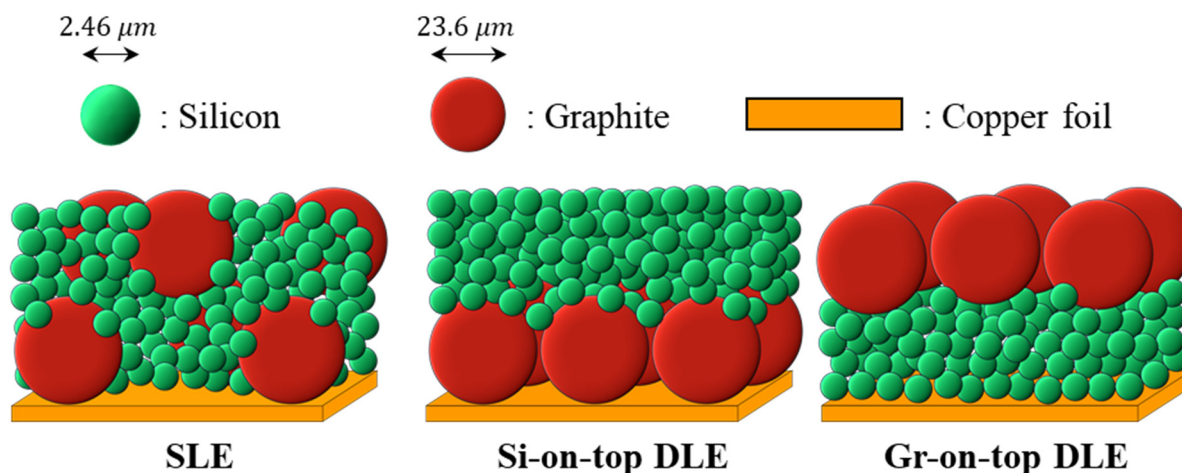


Figure 1. Schematic illustration of SLE and DLEs.

Figure 2 presents SEM images and EDX results of the electrode samples. The top view of each electrode [Figure 2a–c] shows the different surface distributions according to the arrangement of the active materials. The samples that were used to acquire the cross-sectional SEM images [Figure 2d–f] were subjected to a surface polishing process using ion milling to reveal the distribution of the materials in terms of the layers. Comparing Figure 2d–f, it is evident that the distinct layers of silicon and graphite are satisfactorily deposited. To confirm whether the materials are either mixed or separated as intended, EDX mappings of the elements C, Si, and Cu, corresponding to the samples in Figure 2d–f, were acquired and are displayed in Figure 2g–i. The SEM and EDX results reveal that, although we aimed to create distinct layers, the pressing process caused some smaller silicon particles to merge into the graphite regions, as observed in Figure 2e,h. In contrast, the larger graphite particles did not merge into the silicon regions, which is why Figure 2f,g show a more distinct separation. The SEM and EDX results confirm that the three different electrodes were fabricated as intended with either SLE or DLE structures.

The prepared electrodes were assembled in a 2032 coin half-cell for electrochemical analysis. At first, the assembled cells were operated for three cycles at the 0.1 C (0.307 mAh) rate within the voltage window of $0.01\text{--}3.0 \text{ V}$ to allow the SEI to form. Figure 3a shows the voltage profiles of the first cycles of the SLE, Si-on-top DLE, and Gr-on-top DLE cells. The SLE delivered gravimetric delithiation and lithiation capacities of 846 and 920 mAh/g , corresponding to a Coulombic efficiency (CE) of 92% . Similar CEs of 92.2% and 91.9% were obtained for the Si-on-top DLE at 935 and 1014 mAh/g , and the Gr-on-top DLE at 815 and 887 mAh/g . Compared to the SLE and Gr-on-top DLE, the capacity of the Si-on-top DLE was 8% higher and the Coulombic efficiency increased by 0.2% .

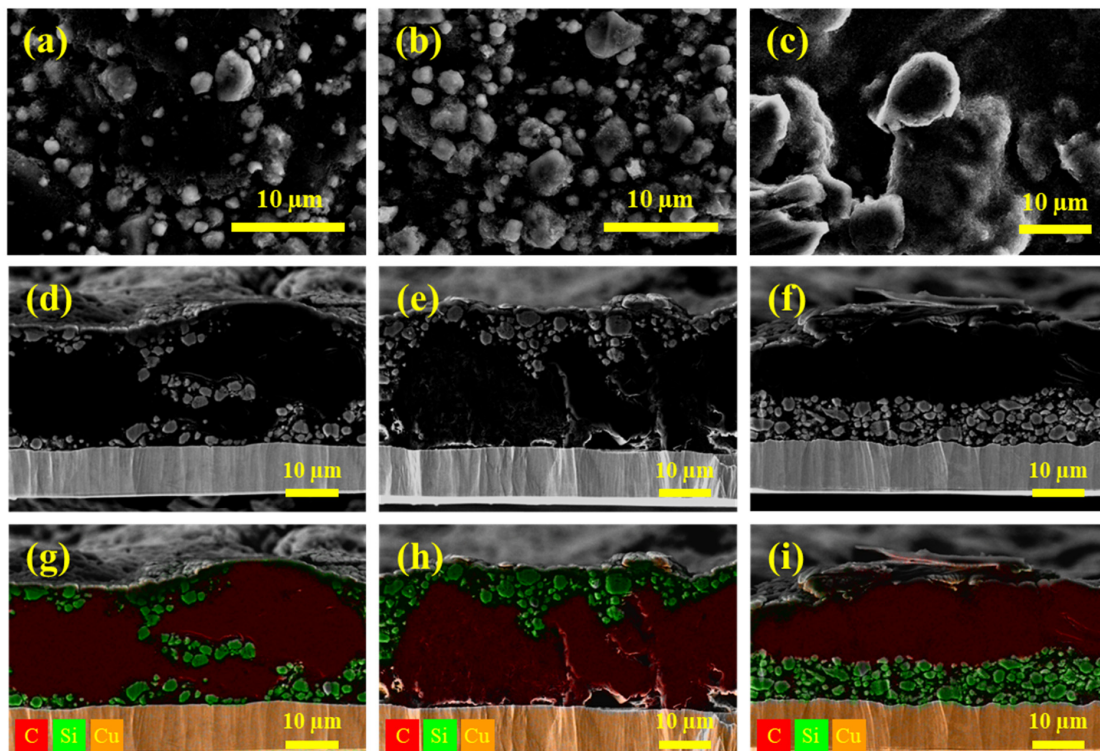


Figure 2. The surface (a–c) and cross-sectional (d–f) SEM images and EDX elemental mappings (g–i) of carbon (red), silicon (green), and copper (orange) of the SLE (a,d,g), Si-on-top DLE (b,e,h), and Gr-on-top DLE (c,f,i).

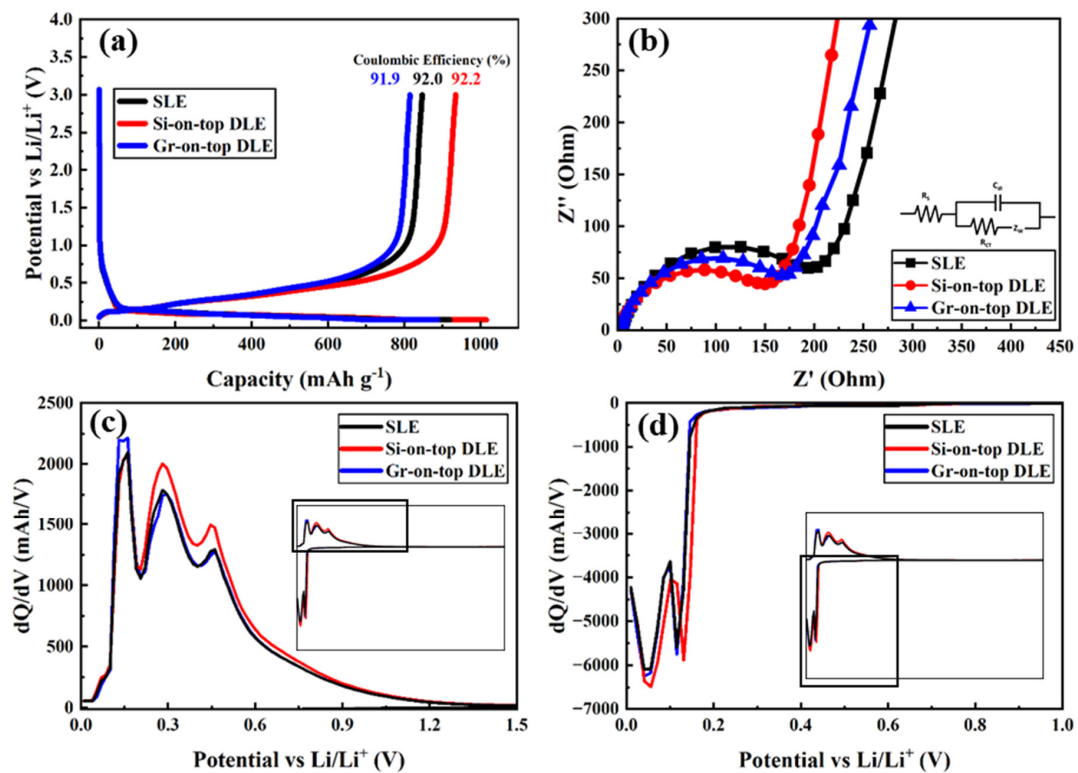


Figure 3. (a) Initial charge/discharge profile, (b) EIS result before formation process of SLE and DLEs (inset: equivalent circuit model). Magnified dQ/dV plot of (c) charging and (d) discharging process of initial cycle (inset: full plot).

The initial capacity and CE of the different cells were measured using electrochemical impedance spectroscopy (EIS) before the formation process. The electrochemical impedance spectra were recorded at the open circuit voltage in the frequency range from 100 kHz to 100 mHz with a perturbation amplitude of 10 mV. Figure 3b shows typical Nyquist plots of the electrodes used in Figure 3a. The EIS data reveal distinct characteristics based on the measured parameters: R_b , R_{ct} , C_{dl} , Z_W , and D_{Li} , the values of which appear in Table 1. Lower values of R_b typically indicate superior conductivity of the electrode material, which facilitates easier electron flow [23]. Among the measured values, the SLE had the highest resistance of 4.90 Ω , which was twice as high as that of the DLE. The Si-on-top DLE demonstrated the most favorable electrochemical characteristics with the lowest R_{ct} of 86.1 Ω . This indicates that this electrode has the most efficient charge transfer, a property that is essential for limiting polarization losses during battery operation and enhancing the overall battery performance, including the initial capacity increase [24]. C_{dl} provides insights into the ability of the electrode surface to store charge [25]. The Gr-on-top DLE had the highest double-layer capacitance of 11.8 μF , which suggests a larger electrochemically active surface area, and which enhances the ability of the battery to store and release energy efficiently [25,26]. The Si-on-top DLE had the next-highest C_{dl} value and the SLE had the lowest value. Z_W is an indicator of the ion diffusion resistance [24,27]. The value of 464 Ω for the Si-on-top DLE indicates that this electrode had the lowest ion diffusion resistance, which allows for faster Li-ion transport within the electrode. Finally, D_{Li} highlights the differences in ion mobility across a sample [27,28]. A higher D_{Li} such as the $1.39 \times 10^{-18} \text{ cm}^2/\text{s}$ of the Si-on-top DLE reflects superior ion transport capabilities, which can enhance the electrochemical performance of the battery by reducing the ionic resistance [28]. The differences in the initial charge/discharge profiles of the samples may have resulted from electrode polarization, including charge transfer polarization (related to C_{dl}) and concentration polarization (related to D_{Li}), both of which affect the overall electrochemical reactions and performance [29]. Taken together, the initial EIS data show that the Si-on-top DLE had relatively low resistance and high ion mobility, indicating that this electrode outperformed the other electrodes in the initial stages.

Table 1. The values calculated from the initial EIS results before the formation process.

	R_b (Ω)	R_{ct} (Ω)	C_{dl} (μF)	Z'_W (Ω)	D_{Li} (cm^2/s)
SLE	4.90	120	9.33	545	1.01×10^{-18}
Si-on-top DLE	2.35	86.1	10.2	464	1.39×10^{-18}
Gr-on-top DLE	2.63	96.4	11.8	502	1.19×10^{-18}

Figure 3c,d presents the differential capacity plots (dQ/dV) for the initial charge and discharge process of the SLE, Si-on-top DLE, and Gr-on-top DLE. The differential capacity plots highlight the advantages of the Si-on-top DLE over the SLE and Gr-on-top DLE. The sharper peaks and reduced hysteresis of the Si-on-top DLE suggest more efficient ionic and electronic transport, which results in superior capacity utilization and cycling stability [30,31]. The clear differentiation in the peaks implies more effective management of the repeated electrochemical reaction of Si, which is crucial for maintaining electrode integrity over repeated cycles [32–34]. The SLE, despite benefiting from the combined capacity contributions of silicon and graphite, is negatively impacted by higher polarization and less distinct electrochemical processes to lower its overall efficiency [35]. In contrast, the Gr-on-top DLE delivers moderate performance, with the stability of graphite partially offsetting the challenges presented by silicon, yet not optimizing its high-capacity potential. These findings demonstrate that arranging the layers such that silicon is the top layer of the DLE enhances the electrochemical performance by improving the kinetic conditions for lithium-ion intercalation and minimizing the adverse effects of volumetric changes during cycling [36]. This highlights the importance of the order in which layers of materials are arranged for optimizing the performance of high energy density lithium-ion batteries.

Figure 4 shows the effect of the DLE on the cycling performance evaluated at the 0.5 C (1.50 mAh) current rate within the voltage window of 0.01–3.0 V with the current cut-off limit of 0.005 C. After the first cycle, the capacity of the SLE was 735 mAh/g and this value decreased to 370 mAh/g at the 100th cycle, which corresponds to a capacity retention of 50.3%. This is similar to the cycling efficiency of 55.9% of the Gr-on-top DLE with capacities of 728 and 407 mAh/g at the first and 100th cycle, respectively. In comparison, the retention of the Si-on-top DLE was significant at 70.0% with capacities of 767 mAh/g and 537 mAh/g at the first and 100th cycles, respectively. Compared to the SLE, the presence of silicon on the outer surface enhanced the capacity retention rate by about 20%. The enhanced capacity retention of the Si-on-top DLE is attributed to several key mechanisms. First, when silicon is located in the top layer, it facilitates more efficient formation of the SEI layer. This stable SEI layer reduces the degradation caused by volume expansion and contraction, maintaining the electrode's integrity and thereby improving capacity retention. Second, silicon on the top layer provides a structural advantage by isolating the bulk of volume changes, minimizing internal stress propagation, and enhancing overall structural stability. Third, the Si-on-top DLE exhibits lower R_{ct} and higher D_{Li} compared to SLE, allowing electrochemical reactions to proceed more efficiently, maintaining active material functionality, and reducing capacity loss over cycles. The experimental data from EIS and charge/discharge profiles support these findings, indicating that the Si-on-top DLE undergoes less degradation during cycling, thereby preserving capacity more effectively. The reason for the difference in capacity retention was determined by referring to the charge/discharge profile at certain cycles, as shown in Figure 4b–d.

A comparison of Figure 4b–d revealed the most noticeable difference in the profile of the 100th cycle (magenta) of the SLE. Higher initial voltage during delithiation is known to indicate an increase in the overpotential [37,38]. This reflects that higher energy is required to initiate reactions and suggests increased polarization [37]. This may be related to electrode degradation caused by the collapse of the SEI layer due to volume expansion during repeated charge/discharge cycles [38,39]. The large amount of noise observed in the voltage plateau near 0.8 V is linked to side reactions resulting from the collapse of the SEI layer, indicating structural damage that is also evidenced by capacity fading [40]. Capacity fading during cycling can be attributed to several factors, including collapse and growth of the SEI layer, loss of active material, and increased internal resistance [39,41,42]. To gather evidence of electrode degradation, the electrochemical impedance spectra were recorded after the formation process. The EIS results are shown in Figure 4e and the measured values appear in Table 2.

Table 2. The values calculated on the basis of the initial EIS results at SOC 100.

	R_b (Ω)	R_{ct} (Ω)	C_{dl} (μF)	Z'_w (Ω)	D_{Li} (cm^2/s)
SLE	6.19	48.0	18.3	10.4	2.78×10^{-15}
Si-on-top DLE	4.89	41.8	18.1	3.85	2.02×10^{-14}
Gr-on-top DLE	3.63	50.8	17.3	7.95	4.75×10^{-15}

By referring to the parameter values in Tables 1 and 2, it is possible to infer the reasons for the variation in electrode degradation between the electrodes. The low R_{ct} and Z_w and high D_{Li} values with silicon as the top layer imply efficient SEI layer formation and an appropriate change in C_{dl} , which suggests structural stability [43–45]. On the other hand, the higher R_{ct} and Z_w and lower D_{Li} values of the SLE indicate inefficient SEI layer formation and structural instability, which leads to faster degradation during cycling [41]. The moderate R_{ct} , Z_w , and D_{Li} values of the Gr-on-top DLE suggest that, although the use of graphite as the outermost layer provides some initial stability, the arrangement is prone to structural issues due to the underlying volume expansion of Si, which can lead to degradation patterns similar to those observed for the SLE. Based on the results of the cycling test and EIS analysis, the Si-on-top DLE demonstrated a significant improvement in

capacity retention by maintaining 70.0% after 100 cycles. This is in contrast to the SLE and Gr-on-top DLE, which exhibited lower retention rates (50% and 56%, respectively). The enhanced performance of the Si-on-top DLE is attributed to the efficient formation of the SEI layer and greater structural stability, as evidenced by lower charge transfer resistance and higher lithium-ion diffusion. Conversely, the SLE and Gr-on-top DLE showed signs of electrode degradation, with increased overpotential and SEI layer instability that ultimately lead to capacity fading. These differences were validated through EIS and corroborated by the observed charge/discharge profiles.

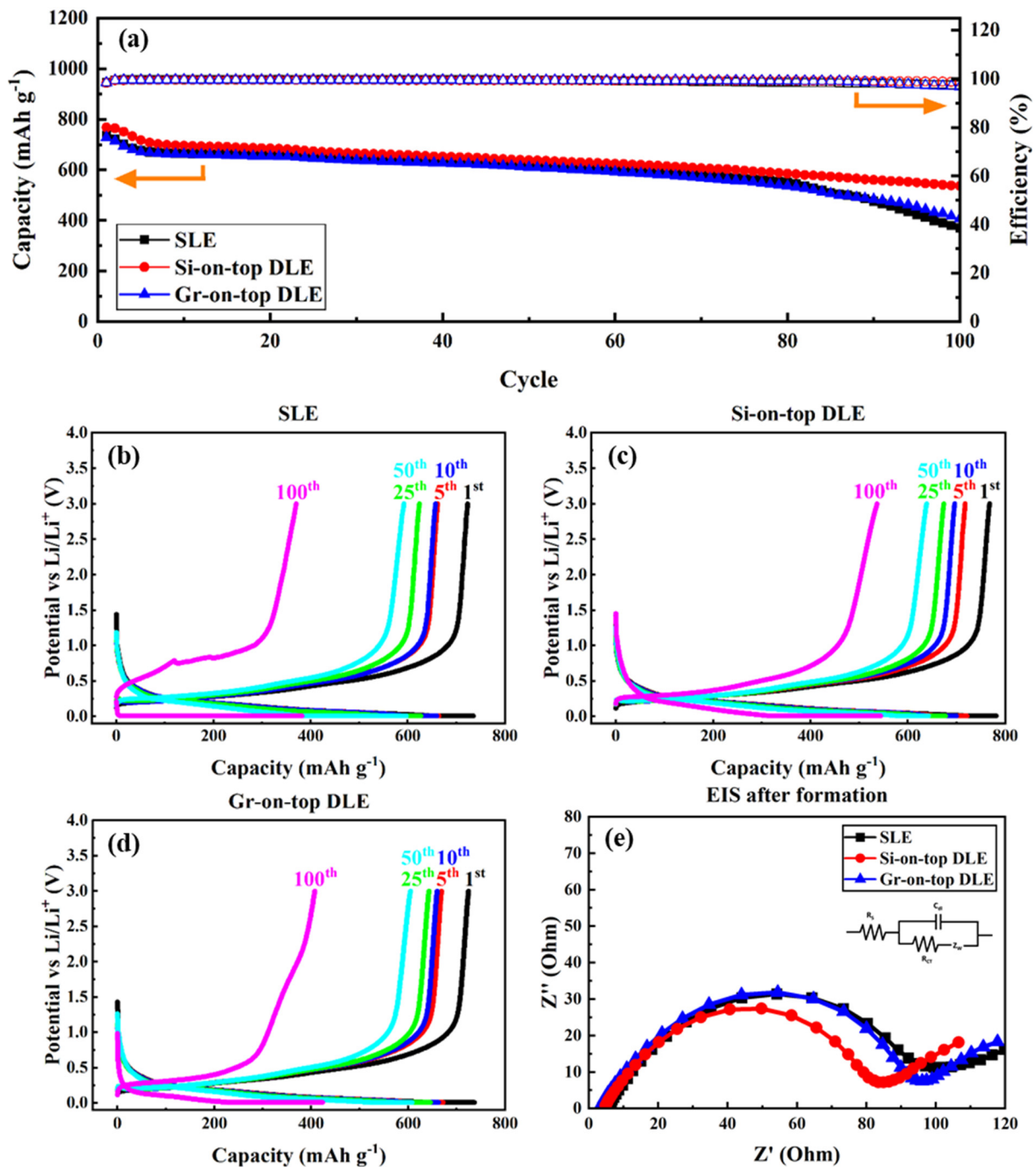


Figure 4. (a) The cycling performance at 0.5 C for 100 cycles, (b–d) the charge/–discharge profile at the 1st, 5th, 10th, 25th, 50th, and 100th cycles of the SLE, Si-on-top DLE, and Gr-on-top DLE and (e) the results of the EIS analysis after the formation process.

A rate test was conducted to explore the effect of applying different current rates, ranging from 0.2 C to 5 C, with an additional five cycles at 0.2 C at the end to observe recovery. For the rates higher than 0.5 C, additional delithiation processes at 0.2 C were introduced in each cycle to ensure thorough delithiation. The discharge capacity results are shown in Figure 5a. The charge/discharge profiles of the last cycle of the cells at each rate are shown in Figure 5b–d. Although no significant differences were observed between the samples at most rate values, the Gr-on-top DLE exhibited a noticeable capacity fall at 5 C. The capacity drop and the charge/discharge efficiency were both noticeably lower for the Gr-on-top DLE. Upon examining the charge capacity, it was found that the Gr-on-top DLE had a lower charge capacity compared to the other samples. This could possibly be explained by considering that, at high rates, electrons and lithium ions are unable to penetrate the silicon layer, which provides most of the capacity, and instead are inserted into the graphite layer [35,46,47]. This suggests that the rate at which lithium ions are inserted into the graphite layer is significantly faster than the rate at which they intercalate into the silicon layer through the graphite.

To validate this hypothesis, the electrode resistance values were measured, as shown in Figure 5e. The results indicate that the Gr-on-top DLE exhibited the highest resistance, suggesting that lithium ions have difficulty penetrating deeply and that electrons find it difficult to reach the surface [48,49]. Although this may not significantly impact performance at low C-rates, substantial changes occur at higher rates. According to the fundamental mechanism of lithium intercalation, lithium initially intercalates at the electrode surface and then diffuses deeper through continuous reactions within the electrode [50–52]. Unfortunately, during this process, the active material undergoes volumetric expansion to obstruct the pathways for both electron and lithium-ion diffusion [46,48,53]. To fully leverage the potential of the electrode, smooth ionic and electronic transport is essential, but the high interface resistance of the Gr-on-top DLE significantly increases the ohmic and concentration polarization to prevent its full utilization under the high-rate conditions at which rapid lithium diffusion is crucial [54].

The degree of electron transport and Li-ion diffusion was therefore investigated by analyzing the tortuosity [55]. The tortuosity (τ) is an indicator of the inefficiency of the pathway along which ions or electrons travel through the electrode, expressed as the ratio of the actual path to the linear distance as in Equation (4) [56].

$$\tau = \frac{L_{actual}}{L_{straight}} \quad (5)$$

where $L_{straight}$ is the distance on a straight line, which is mostly affected by the thickness of the electrode and separator, and L_{actual} is the pathway along which or the distance ions or electrons are moving, which is affected by the interface resistance, surface resistance, Li-ion diffusivity, and Warburg impedance [55–57]. By positioning the silicon layer, with its high capacity versus that of the graphite, closer to the Li metal counter electrode, the effective ion transport pathways are shortened to decrease the tortuosity [57]. Lower tortuosity facilitates more direct and efficient Li-ion diffusion and minimizes the resistance encountered by ions as they travel through the electrode [58]. This structural arrangement not only decreases the charge transfer resistance but also enhances the overall ion mobility, to ultimately improve the initial capacity and the electrochemical performance [59]. Consequently, the Si-on-top DLE configuration outperforms the SLE and Gr-on-top DLE, as the lower tortuosity allows for more efficient utilization of the high-capacity silicon material [55–60]. The EIS data support these findings by showing that the Si-on-top configuration exhibits lower resistance and higher diffusion coefficients, thereby confirming its superior performance.

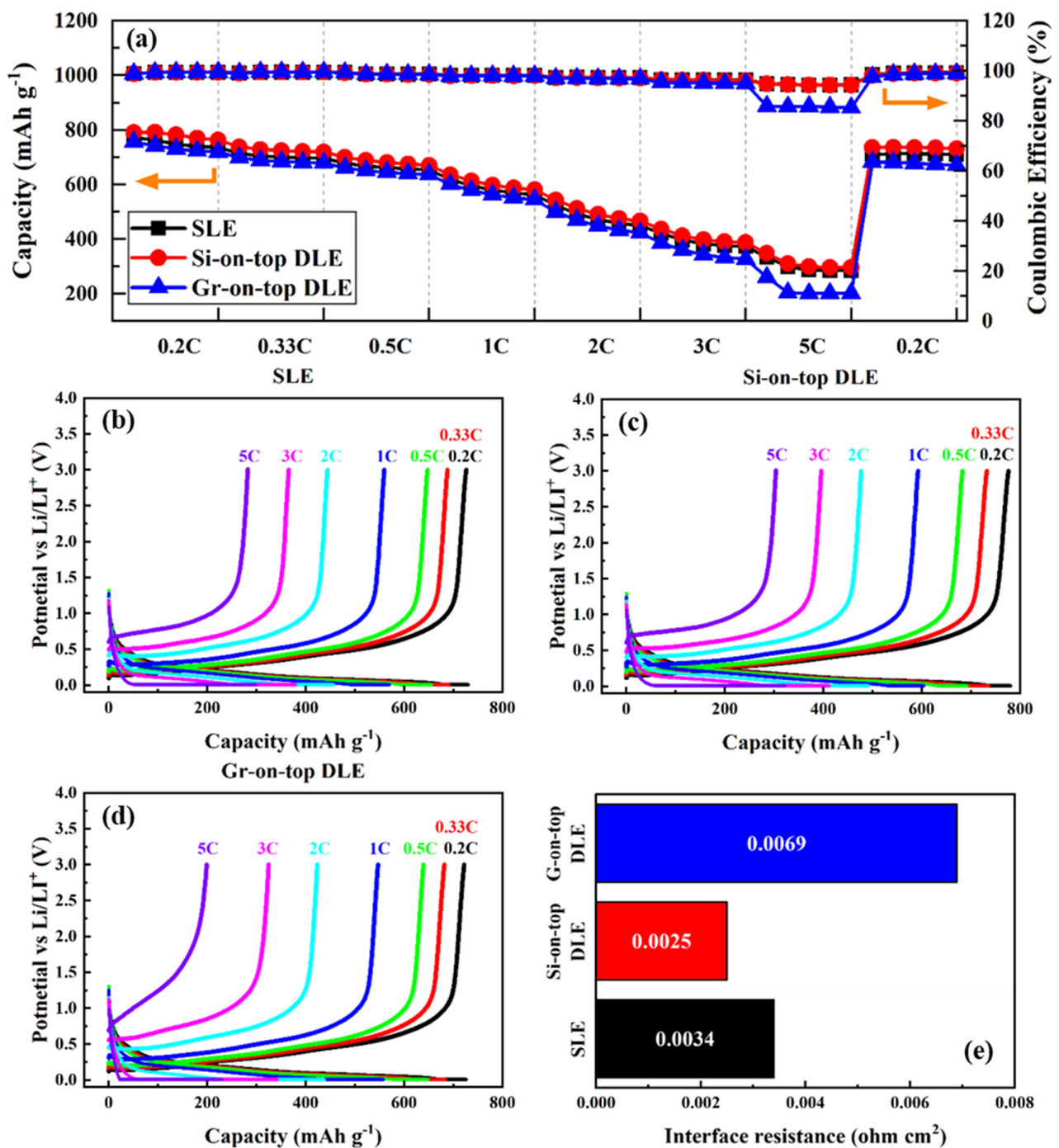


Figure 5. (a) Rate capability of each electrode at various current rates (0.2, 0.33, 0.5, 1, 2, 3, and 5 C), (b–d) charge/–discharge profile at last cycle of each C–rate of SLE, Si-on-top DLE and Gr-on-top DLE, and (e) interface resistance.

The overall comparison of the functional performance parameters including initial capacity, initial CE, 100th cycle capacity, 100th cycle capacity retention and interface resistance is organized in Table 3.

Table 3. Comparison of functional performance parameters.

	Initial Capacity (mAh/g)	Initial CE (%)	100th Cycle Capacity (mAh/g)	100th Cycle Capacity Retention (%)	Interface Resistance ($\Omega \text{ cm}^2$)
SLE	846	92.0	370	50.3	0.0034
Si-on-top DLE	935	92.2	537	70.0	0.0025
Gr-on-top DLE	815	91.9	407	55.9	0.0069

4. Conclusions

In this study, we demonstrated that, by strategically confining the active materials to layers that can be applied to the electrode in the desired order, the dual-layer electrode (DLE) design improves the electrochemical performance of lithium-ion batteries. The confinement of silicon and graphite to distinct layers of a dual-layer structure on the electrode surface enabled us to enhance stability and efficiency compared to conventional mixed-material single-layered electrodes (SLEs). The silicon-on-top DLE especially yielded outstanding results, with an initial capacity of 935 mAh/g and 70% capacity retention after 100 cycles at 0.5 C. This stands in stark contrast to the SLE, for which the retention was only 50.3% under the same conditions. The silicon-on-top DLE also had the lowest charge transfer resistance (41.8 Ω) and the highest lithium-ion diffusion coefficient ($2.02 \times 10^{-14} \text{ cm}^2/\text{s}$), indicative of improved ionic and electronic transport. These improvements are attributed to the reduced tortuosity and enhanced kinetics facilitated by the dual-layer structure, which mitigates the challenges associated with the volumetric expansion of silicon. Our findings underscore the potential of using the dual-layer approach, particularly by positioning the silicon layer on top, to develop high-performance batteries with increased energy density and longevity, while minimizing the need for extensive changes to current manufacturing processes. This innovative design strategy offers a practical and scalable solution to meet the increasing demands for efficient energy storage in modern applications.

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