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Neuron Circuit Based on a Split-gate Transistor with Nonvolatile Memory for Homeostatic Functions of Biological Neurons

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Abstract: To mimic the homeostatic functionality of biological neurons, a split-gate field-effect transistor (S-G FET) with a charge trap layer is proposed within a neuron circuit. By adjusting the number of charges trapped in the Si_3N_4 layer, the threshold voltage (V_{th}) of the S-G FET changes. To prevent degradation of the gate dielectric due to program/erase pulses, the gates for read operation and V_{th} control were separated through the fin structure. A circuit that modulates the width and amplitude of the pulse was constructed to generate a Program/Erase pulse for the S-G FET as the output pulse of the neuron circuit. By adjusting the V_{th} of the neuron circuit, the firing rate can be lowered by increasing the V_{th} of the neuron circuit with a high firing rate. To verify the performance of the neural network based on S-G FET, a simulation of online unsupervised learning and classification in a 2-layer SNN is performed. The results show that the recognition rate was improved by 8% by increasing the threshold of the neuron circuit fired.

Keywords: neuron circuit; homeostasis functionality; nonvolatile memory; charge trap layer

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1. Introduction

Recently, artificial neural networks (ANNs), inspired by the brain, have been actively researched and developed [1]. Particular attention has been paid to spiking neural networks (SNNs) that utilize biological spike timing–dependent plasticity (STDP) rules to function as event-driven systems for unsupervised learning [2–10]. Since such SNNs pursue a more bio-plausible direction than other ANNs do, it is necessary to explore the signal transmission mechanisms of biological neurons and synapses to gain a deeper understanding of these SNNs. Figure 1a illustrates the neurons and synapses, and we focus on explaining the membrane potential and neurotransmission of neurons. Neurons maintain the membrane potential by consuming adenosine triphosphate, and the membrane potential increases when cations are injected into the membrane due to stimuli pro-vided as dendrites. At this point, if the membrane potential exceeds a specific threshold value, the neuron will be depolarized. Then, the membrane potential reaches the action potential, following which the neuron is repolarized and the membrane potential restored to its initial value. The electrical spikes generated in this process are transmitted to the axon of the neuron in an electrical form and to the post-synaptic neuron in the form of a neurotransmitter through the synapse. However, according to rate-based learning rules such as SRDP and BCM [11–14], synapses cannot simply transmit signals between two neurons; rather, they can modulate the strength of the transmitted signal by increasing the synaptic efficiency when receiving high-frequency stimulation and reducing it when receiving low-frequency stimulation. These changes in synaptic strength can be explained primarily by activity-dependent plasticity, such as long-term potentiation and long-term depression, and are known to be closely related to the functions per-formed by the brain, such as learning, memory, and cognition. When synaptic strength changes only due to activity, the neural activity can be induced in the direction of runaway excitation or

sequences. In response, neurons are known to perform homeostatic regulation to stabilize natural activity and maintain their average firing rate within a narrow range. Figure 1b shows the change of AMPA receptor's number at the post-synaptic surface induced by neural activity. AMPA receptor's numbers at the postsynaptic surface are accordingly scaled up- or downwardly in response to activity deprivation or overexcitation, respectively. In this process, the firing rate of neurons is maintained in a narrow range [15–18].

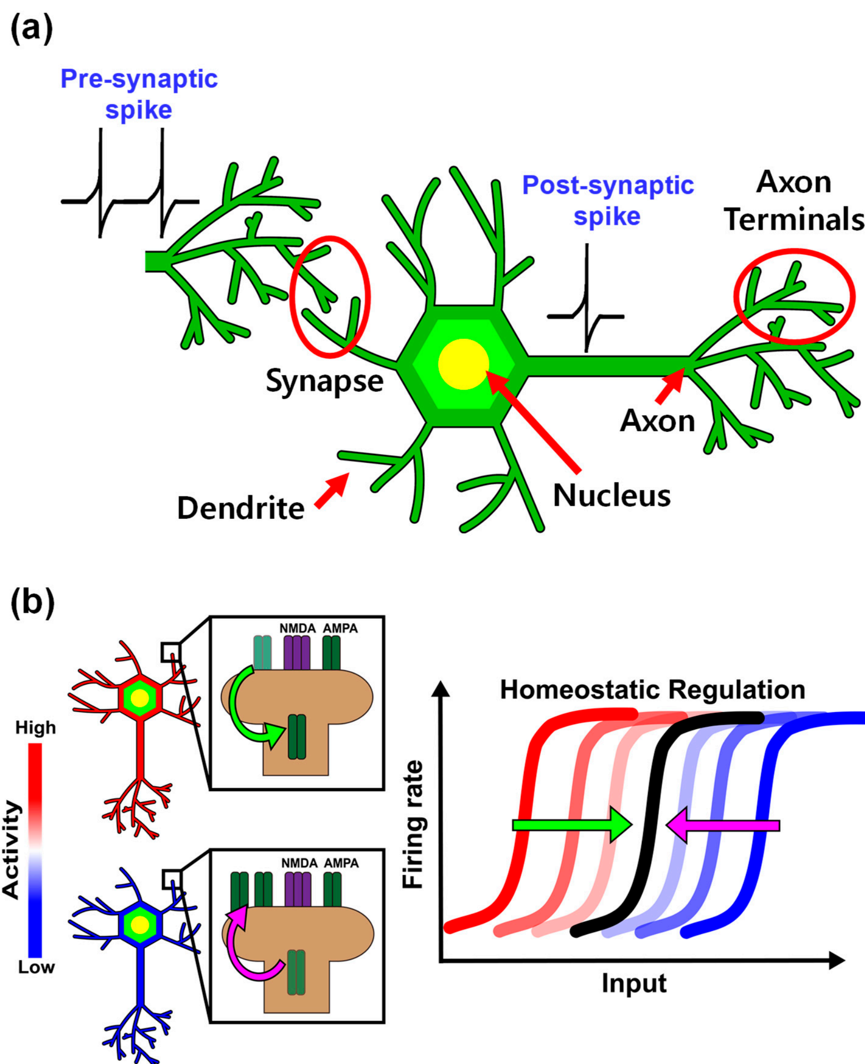


Figure 1. (**a**) Simple diagram of a biological neuron and synapse. The neuron is composed of a nucleus, dendrite, axon, and axon terminals. Synapse is a connection between pre-synaptic neurons and post-synaptic neurons. (**b**) A model of homeostatic regulation which stabilizes firing rate of neurons by synapse scaling.

Recently, research has focused on integrating neuromorphic systems and hard-ware-based neural networks with various emerging memory devices to enable energy-efficient operation of artificial intelligence algorithms [9,10,19–43]. For instance, on-chip learning can reduce power consumption and compensate for the degradation caused by device variation [44–49]. Similar to biological neurons, STDP-based neural networks re-quire a homeostasis functionality that controls the firing rate of the output neurons to achieve more accurate pattern recognition. The homeostasis functionality in biological neurons involves reducing the fire rate of dominant (high firing rate) neurons and increasing that of weak (low firing rate) neurons. Various studies have attempted to implement the homeostasis functionality in hardware and software neural systems [50–56]. To mimic the

homeostasis function, each neuron needs peripheral circuits composed of conventional complementary metal-oxide-semiconductors (CMOSs) and capacitors. However, if all neuron circuits have at least one large capacitor, the hardware footprint of the neural system can become excessive. In addition, when synaptic weights are updated in SNNs, the value controlling the firing frequency of each neuron circuit is also updated and stored in the peripheral circuits. Due to the volatile memory functionality in peripheral circuits, maintaining the values for the homeostasis functionality in the system is impossible without a supply voltage.

In this paper a split-gate field-effect transistor (S-G FET) with a charge-storage layer is proposed to mimic the homeostasis functionality. The S-G FET is used to compare the membrane potential (V_{mem}) with the threshold voltage (V_{th}) for the fire function in the neuron circuit. By using the fin structure in the S-G FET with independent double gates, it was possible to implement a stable operation of neuron circuit by distinguishing between the gate for implementing homeostatic function through P/E and the gate for reading synaptic signals. The V_{th} of each neuron circuit can be updated selectively using the S-G FET, which has two independent gates. The homeostasis functionality can be achieved by controlling the threshold of the neuron circuit using the program/erase operation in the charge-trap layer. Employing a nonvolatile memory functionality for the charge storage layer can maintain the optimized V_{th} of the neuron circuit. A two-layer SNN based on biological STDP learning rules was simulated with the S-G FET to demonstrate the improved pattern-recognition accuracy on MINST datasets.

2. Materials and Methods

The S-G FET was fabricated on a 6-inch Si wafer using conventional CMOS technology. Figure 2a–h shows the fabrication steps for integrating the S-G FET, n-type FET, p-type FET, and memory devices. First, a sacrificial SiO_2 layer is deposited on the wafer and patterned to obtain the single-gate FETs, and a nitride layer is then deposited. Subsequently, a 250 nm poly-Si layer is deposited and patterned to enable the formation of the Si_3N_4 spacers. Next, a 35 nm (fin width = 35 nm) Si_3N_4 layer is deposited and etched again, causing the Si_3N_4 spacers to be formed on the sidewalls of the patterned poly-Si layer (Figure 2a). The poly-Si layer is selectively removed using a solution of HNO_3 and HF (Figure 2b), and the Si substrate is etched to a depth of 80 nm (fin height = 80 nm) with the Si_3N_4 spacers as a hard mask (Figure 2c). Then, a thin SiO_2 film is again deposited as a barrier layer for SF_6 dry etching, followed by the deposition of a poly-Si layer (Figure 2d). The poly-Si spacers are selectively removed using a mask in the regions of bulk-fin FETs, followed by anisotropic etching of SiO_2 (Figure 2e). Thereafter, isotropic Si etching using SF_6 gas is performed by controlling the etching thickness (Figure 2f). Si fins without the SiO_2/poly-Si sidewalls are separated from the Si substrate, as shown on the left in Figure 2g. Notably, both ends of the separated fins are connected to the substrate, as shown on the right in Figure 2g. By wet-etching SiO_2 in a buffered hydrogen fluoride solution, the Si_3N_4 spacers on the sacrificial SiO_2 are removed. The gap between the Si fins is filled with SiO_2 via a high-density plasma chemical vapor deposition process (Figure 2h). After the SiO_2 is etched up to a certain thickness (until the top of the Si fins), boron and phosphorus ions are implanted for the field and channel doping of the n-type and p-type FETs, respectively. Then, the $SiO_2/Si_3N_4/SiO_2$ (2/4.2/9 nm) gate dielectric layer, which is called the O/N/O layer, is deposited for a memory function, and a SiO_2 film (10 nm) is deposited as the gate dielectric layer of the conventional MOSFET, respectively. (Figure 2i). Then, an n^+-doped poly-Si layer is deposited as a gate material. To form the independent split gates using the Si_3N_4 spacers, the wafer is coated with a diluted photoresist (PR); a thin PR layer is then formed only on the top of the Si_3N_4 spacers (Figure 2j). By etching the PR up to a specific thickness, only the n^+-doped poly-Si on the Si_3N_4 spacers is exposed (Figure 2k). The exposed n^+-doped poly-Si is then etched to form the independent split gates. The remaining PR is removed, followed by the patterning of the n^+-doped poly-Si for the gates. Subsequently, the Si_3N_4 spacer is striped (Figure 2l). After boron and arsenic ions are

implanted for the source/drain regions of the n-type and p-type FETs, respectively, rapid thermal annealing is conducted at a temperature of 1050 °C (5 s) to activate the ions. Then, an interlayer dielectric is deposited, and the contact holes and metal are patterned.

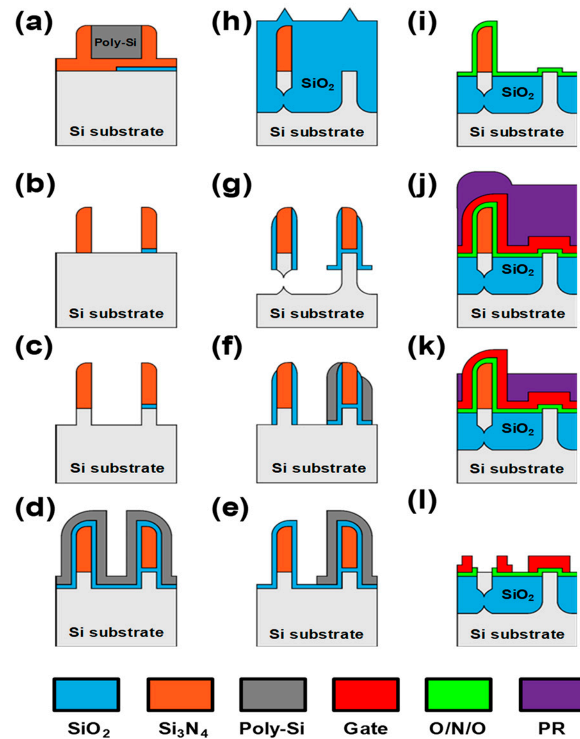


Figure 2. (**a**–**l**) Steps for integration of the fabricated S-G FET, n-type FET, p-type FET, and memory devices on the same wafer.

Figure 3a,b show a 3D schematic view and a cross-sectional transmission electron microscopy (TEM) image, respectively, of the fabricated S-G FET with a floating fin body. The split gates (G1 and G2) are n+ doped poly-Si, and the thickness of the gate oxide (SiO_2) is 9 nm for the conventional CMOSFET. The thicknesses of the tunneling layer, charge-trap layer, and blocking layer are 2 nm, 4.2 nm, and 9 nm, respectively, consisting of the $SiO_2/Si_3N_4/SiO_2$ stack to provide the nonvolatile memory for the homeostatic function. The width (W_{fin}) and height (H_{fin}) of the floating fin body are 35 nm and 80 nm, respectively. The split gates on both sides of the floating fin body can be used to modulate the threshold voltage (V_{th}) of the S-G FET, thereby enabling neuron circuits to be controlled using the S-G FET. The doping concentrations of the n-type channel, p-type channel, source region, and drain region are 1×10^{18} cm^{-3}, 1×10^{18} cm^{-3}, 2×10^{20} cm^{-3}, and 2×10^{20} cm^{-3}, respectively.

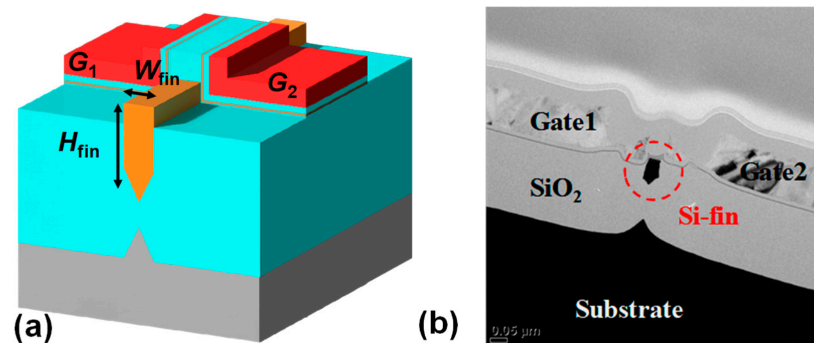


Figure 3. (**a**) 3D schematic view and (**b**) cross-sectional TEM image of the fabricated S-G FET.

3. Results and Discussion

3.1. Basic Device Characteristics

Figure 4 shows the I_D-V_G characteristics of CMOSs and S-G FET, respectively. The entire measurement process was conducted using the Keysight B1500A parameter analyzer with 10ms intervals. Figure 4a shows the measured I_D–V_G curves of the n-type and p-type FETs fabricated on the same wafer. The gate width (W) and length (L) of the conventional CMOSs are 35 nm and 1 μm, respectively. The subthreshold swings (SS) of of conventional n-type MOSFET and p-type MOSFET are 70 mV/decade and 160 mV/decade at V_D = 0.1 V, respectively. The conventional CMOSs are used for the neuron circuits, self-controller (including a pulse generator for the program/erase operation of synaptic devices and the S-G FET), and connecting parts (current mirror and switch circuits) between the synaptic array and neuron circuit. Figure 4b shows the measured I_D–V_{G1} curves of the S-G FET for V_{G2} values between −2 V and 2 V. The solid and hollow symbols represent the transfer curves at V_D values of 0.1 V and 1 V, respectively. For both sets of curves, the I_D values are almost identical at the same V_{G1} due to the low drain-induced barrier lowering of the fabricated S-G FET. As the gate voltage applied to G2 decreases from positive to negative, the potential in the channel region increases, and the electron energy barrier from the source region to the channel region increases as well. This results in an increase in the V_{th} of the S-G FET. Since the channel region between the split gates is fully depleted as 35 nm, the $\triangle V_{th}$ of the S-G FET is almost linearly related to $\triangle V_{G2}$ [20]. In previous studies, neuron circuits were designed as homeostatic circuits consisting of current mirrors and a single capacitor, to mimic the biological homeostatic function. However, since this involves storing the homeostatic data of neurons in capacitors to control the V_{th} of each neuron, a risk of data loss exists due to the volatile memory characteristics of the capacitors. Additionally, the large size of such capacitors (with a 1 pF capacitor occupying 100 μm^2 at a SiO_2 thickness of 10 nm) causes the neuron circuit array to occupy a significant area. As described below, however, utilizing the nonvolatile memory characteristics of the charge-trap layer allows for implementing the homeostatic function of biological neurons at a high density as well as permanent storage of homeostatic data.

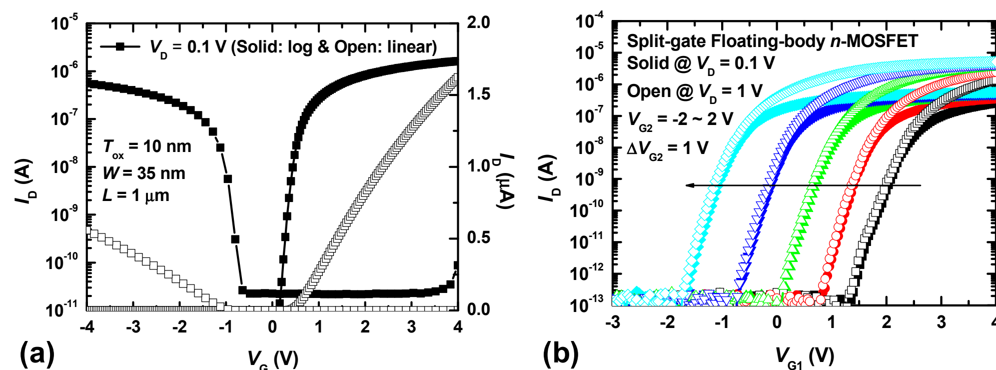


Figure 4. (**a**) The measured I_D-V_G curves of the n-type FET and p-type FET, fabricated on the same wafer with the S-G FET. (**b**) The measured I_D-V_{G1} curves of the S-G FET as a parameter of different V_{G2} from −2 V to 2 V, respectively. The solid and open symbols represent transfer curves at V_D of 0.1 V and 1 V, respectively.

When the S-G FET with the two independent gates (G1 and G2) is used in a neuron circuit, one gate (G1) reads input signals from a synaptic array, while the other gate (G2) modulates the V_{th} of the S-G FET through the amount of charge in the charge-trap layer via program/erase operations. The program/erase operations are executed in the tunneling layer through the Fowler–Nordheim (FN) tunneling mechanism when high positive/negative voltages are biased across the gate dielectric layers. Figure 5a shows the measured I_D–V_{G1} curves of the S-G FET with the number of program pulses applied to G2. When a positive pulse (V_{PGM} of 7 V, t_{PGM} of 100 μs) is applied to G2 for the program

operation, electrons accumulate in the charge-trap layer adjacent to G2; this has the same effect as applying a negative voltage to G2, resulting in an increase in the V_{th} of the S-G FET. By contrast, when a negative pulse (V_{ERS} of −7.5 V, t_{ERS} of 100 μs) is applied to G2 for the erase operation, the accumulated electrons are de-trapped, resulting in a decrease in the V_{th} of the S-G FET. Figure 5b shows the measured V_{th} changes in I_D–V_{G1} curves of the S-G FET with the number of program/erase pulses applied to G2; V_{th} is measured at an I_D of 10 nA. As the number of program pulses applied to G2 increases, V_{th} increases from 0.6 V to 0.83 V at 50 pulses. Conversely, when the erase pulses are applied to G2, V_{th} gradually decreases and returns to its initial value of 0.6 V when more than 50 pulses are applied. V_{th}s in program and erase states were measured at room temperature with the terminals open. As a result, The V_{th}s of the S-G FET in both states are maintained well over 10^4 s (< V_{th} changes of 10%), as shown in Figure 5c. The V_{th} values of the S-G FET in both the program and erase states are maintained for well over 10^4 s (V_{th} variation < 10%), as shown in Figure 5c; the nonvolatile memory function enables the optimized V_{th} of the S-G FET to be maintained. If the S-G FET is used to determine the threshold of one neuron circuit during the learning process of an SNN, the threshold of all other neuron circuits can be optimized through the PGM/ERS operation. Moreover, G1 and G2 being independent gates allows for the thresholds of all neuron circuits to be updated selectively. No change in the SS is observed until 10^4 program/erase cycles have been executed. However, beyond 10^5 cycles, the tunneling layer on G2 becomes degraded, resulting in an increase in the SS corresponding to the V_{G2} of the S-G FET. Notably, since the program/erase pulses are applied to G2, the gate dielectric of G1 does not degrade, even after more than 10^5 program/erase cycles, as seen in Figure 5d. In addition, |7 V| program/erase pulses are applied to G2 of the S-G FET to modulate the threshold value of the neuron circuit only during the learning process. After learning, only small signal (synaptic signals, membrane potential) are applied to G1 of the S-G FET for the classification and pattern recognition. Therefore, when implementing biological homeostasis functions using nonvolatile memory characteristics, signals transmitted from the synaptic array can be reliably read.

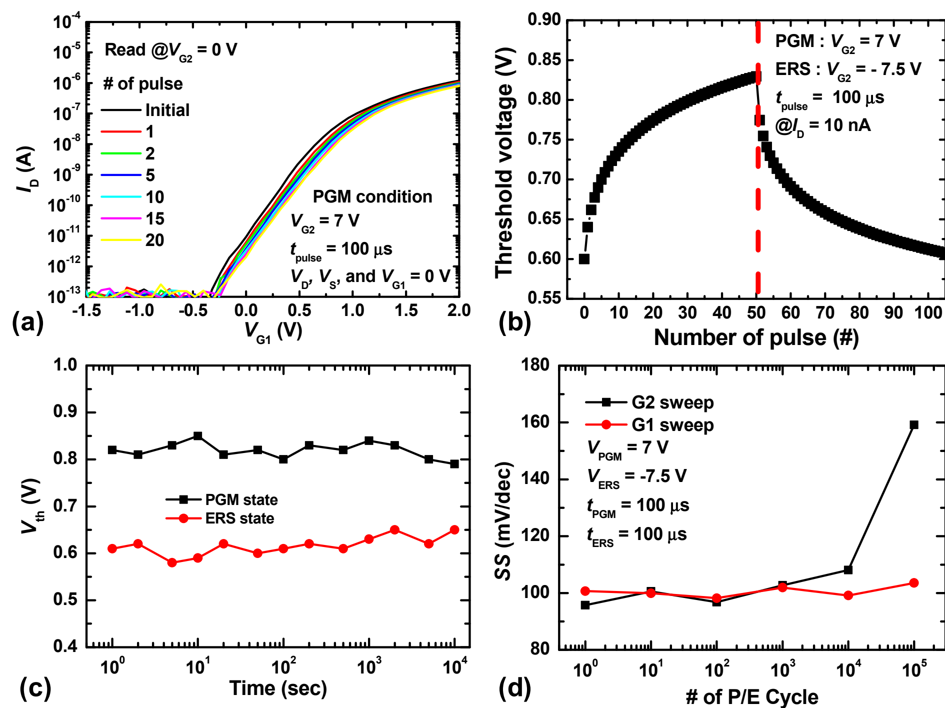


Figure 5. (**a**) I_D-V_{G1} curves of the S-G FET as a function of the number of pulses applied to G2. (**b**) V_{th} variation in I_D-V_{G1} curves of the S-G FET with the number of program/erase pulses applied to G2 at an I_D of 10 nA. (**c**) Retention characteristics (V_{th} change) of the S-G FET over time. (**d**) *SS* variation in the G1 and G2 DC sweep of the S-G FET with the number of program/erase cycles applied to G2.

3.2. A Neuron Circuit Using the S-G FET

Figure 6a shows a schematic of an integrate-and-fire (IF) neuron circuit integrated with the S-G FET. The S-G FET is designed using a Sentaurus TCAD simulation, and the modulation of the V_{th} in the charge trap layer (Si_3N_4) of the S-G FET was performed through the program and erased operations via the Fowler-Nordheim (FN) tunneling model. When determining carrier mobility, the velocity saturation model, doping dependence model, and Lombardi surface mobility model were used. The old Slotboom model was used to calculate bandgap narrowing due to doping. The simulation of the neuron circuit with the S-G FET was conducted using the mixed mode provided in the Sentaurus TCAD simulation. The parameters of the CMOS and capacitors are as follows: L = 0.5 μm, W = 0.1 μm, C_{mem} = 0.5 pF, C_{reset} = 0.05 pF. The supply voltage (V_{DD}) is 1.0 V. C_{mem} is used for the integrate function, while the S-G FET compares the membrane potential (V_{mem}) with V_{th}. When V_{mem} exceeds the V_{th} of the S-G FET due to the charge stored in C_{mem}, the S-G FET triggers the fire function, and the state of Node 1 (N1) changes from high to low. Then, the output node (V_{out}) of INV1 changes from a low to a high state, and the charges accumulated on C_{mem} are drained through M_{reset}. Finally, the neuron circuit resets to the initial state via a feedback signal. At this point, M1 and M2 temporarily enhance the pull-down operation, whereby the S-G FET is activated and lowers the voltage at N1. M4 is intended to prevent the drain current from flowing through the S-G FET when V_{PGM} (positive voltage) is applied to G2 for the program operation. Figure 6b demonstrates the IF operation of the neuron circuit using the S-G FET during the learning process. Through this operation, the output signal is transmitted to the expended pulse generator and voltage shifter, where it can be modulated to the desired pulses for the program operation. When a program pulse (V_{PGM} of 7 V, t_{PGM} of 100 μs) is applied to G2, 0 V is simultaneously applied to the M4 gate to perform the program operation through FN tunneling. The neuron circuit performs the IF operation at a higher V_{mem} from 0.56 V, as shown in Figure 6b. Through the program operation of the S-G FET, V_{th}s of the neuron circuit are increased. Each of the V_{th}s of the neuron circuit after the program operation was 0.558 V, 0.60 V, 0.618 V, 0.637 V, 0.66 V, 0.675 V, and 0.71 V. Consequently, the firing rate of the neuron circuit also linearly decreases as 1902 Hz, 1754 Hz, 1694 Hz, 1639 Hz, 1587 Hz, 1538 Hz, and 1449 Hz. Raising the threshold of frequently firing neuron circuits allows other neurons a greater chance of firing.

An output spike of 1 V and 2 μs generated by the neuron circuit is insufficient for the program/erase operations required to inject charge into the charge-trap layer for implementing homeostatic functions. Hence, to generate the required program/erase pulses, an extended pulse generator and a voltage level shifter are designed (Figure 7a) [57]. The extended pulse generator consists of a NOR gate and buffer invertors to extend the width of the pulse, while the voltage level shifter comprises an inverter and differential amplifier to raise the output signal of the neuron to the V_{PGM} level. In Figure 7a, the parameters of the CMOS, excluding M5, M6, and M7, are as follows: L = 0.5 μm, W = 0.1 μm, C_1 = 1 pF, V_{DD1} = 1 V, and V_{DD2} = 7 V. M5 is designed with L = 2 μm and W = 0.1 μm to slowly pull up the V_2 node; the width of the extended pulse is determined by M5 and the capacitor C_1. Standard CMOS devices are unsuitable for handling high supply voltage about 7 V, in the case of M6 to M9 for high voltage, the simulation was conducted by setting it as a device with lightly doped drain (LDD) which is doping concentration of 1×10^{19} cm^{-3} [58,59]. M6 and M7 are designed with L = 5 um and W = 0.1 um to ensure an output voltage of 0 V in the off state, even when the applied V_{DD2} has a high value of 7 V or more. A high supply voltage is applied to the gates of M6 and M9, generating 7 V, which can cause damage or degradation to the gate oxide. To ensure the stable operation of the circuit, it is necessary to improve the quality and increase the thickness of the CMOS gate oxide through fabrication.

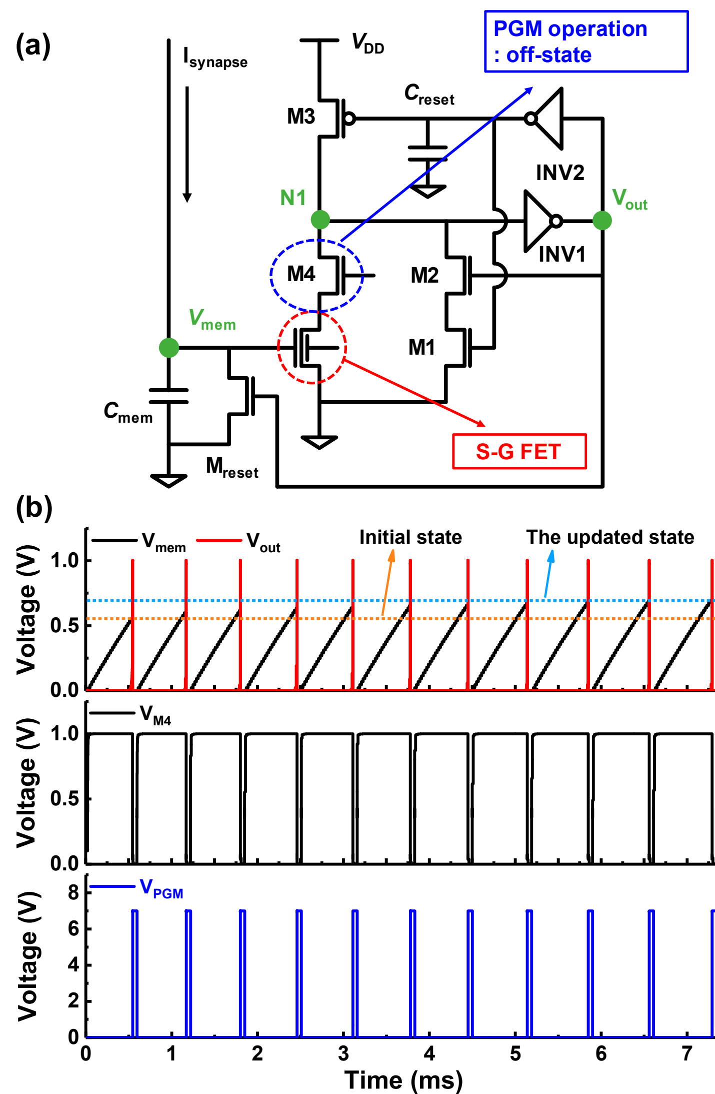
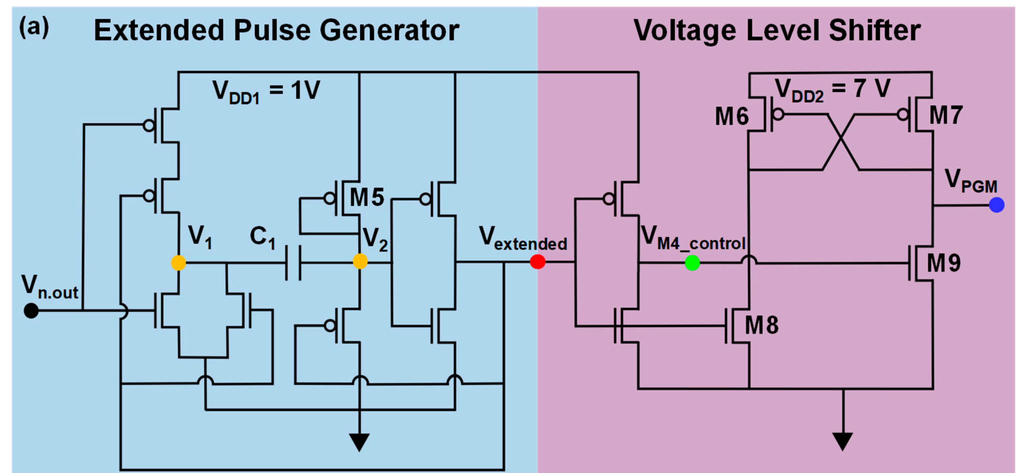


Figure 6. (**a**) Schematic of IF neuron circuit integrated with S-G FET. (**b**) Simulated operational characteristics demonstrating the increase in the neuron circuit threshold during the learning process.

When the output spike is transmitted to the $V_{n.out}$ node, the NOR gate lowers V_1 from 1 V to 0 V. Since V_2 is coupled to V_1 by C_1, V_2 is also set to the low state. Consequently, $V_{extended}$ is raised to the high state by the inverter. Even though $V_{n.out}$ changes from 1 V to 0 V after 2 µs (t_{spike} = 2 µs), V_1 remains 0 V because $V_{extended}$, another input voltage to the NOR gate, is 1 V. However, when V_2 is 0 V, M5 is activated, which causes V_2 to increase gradually from 0 V to 1 V. As shown in Figure 7b, when V_2 is close to 1 V after 50 µs, $V_{extended}$ decreases from 1 V to 0 V. Since all the input voltages and the output voltage of the NOR gate become 0 V, both V_1 and V_2 return to the initial value of 1 V. Thus, the extended pulse generator allows for extending the output spike of the neuron circuit to the time required for the program operation, and the extension duration is determined by the capacitance of C_1 and the current at M5. Next, the process of modulating the amplitude of the extended pulse from 1 V to 7 V is described. The output voltage of the extended pulse generator is transmitted to the input node of the voltage level shifter and the gate of M8. When $V_{extended}$ is raised, M8 is activated, and the inverter deactivates M9. Thus, M7 is activated, and a V_{DD2} of 7 V is applied as the output voltage of the voltage level shifter, which is used as the V_{PGM} for the program operation of the synaptic devices and the S-G FET. Conversely, lowering $V_{extended}$ deactivates M8, causes the inverter to activate M9, and returns all nodes to their initial condition, as shown in Figure 7b.



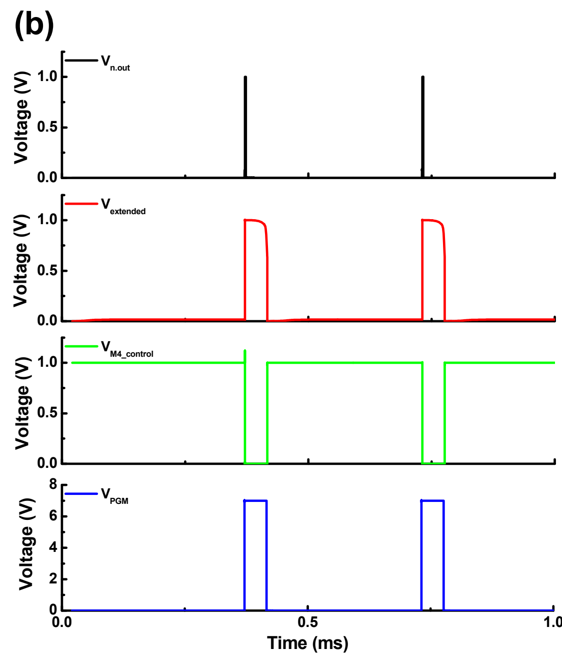


Figure 7. (**a**) Basic configuration circuit including extended pulse generation and voltage level shifter for program/erase operations. (**b**) Simulated *V*–*t* plots for modulation of V_{PGM} pulse from the output pulse of the neuron circuit using the basic configuration circuit.

3.3. Pattern Recognition in SNN with Homeostasis Function

To verify the performance of a neural network based on the S-G FET, online unsupervised learning and classification were performed on in SNNs using MNIST data set with a Python simulator as shown in Figure 8a. The MNIST dataset is represented by 28 × 28 pixels, and 60,000 training and 10,000 test images of MNIST dataset are used for training and verification. The simulated SNN consists of a 784-input neuron layer and a 50–500 output neuron layer. To analyze the change in recognition rate according to the number of output neurons, the output neurons were set from 50 to 500. The synapse array for training the SNN used TFT (Thin Film Transistor) type NOR flash memory, and the memory characteristics for training used a simplified STDP, as shown in Figure 8b [60]. When V_{pre} and V_{post} are applied to the gate and source of each TFT synaptic device, respectively, program (LTD) and erase operations (LTP) in the charge storage layer are performed due to the potential difference (V_{pre}–V_{post}) between the gate and source [60]. Figure 8c shows a block diagram of the proposed system, consisting of a synapse array, neuron circuits, and a common controller (including switch circuits, the extended pulse

generator, and the voltage level shifter). To ensure that other neurons have the opportunity to fire, the thresholds of frequently fired neurons were increased by applying V_{PGM_SGFET} whenever a neuron fired and transmitted an output signal. To accelerate the learning, the thresholds of all neuron circuits were reduced by periodically applying V_{ERS_SGFET} to all the neuron circuits. As described earlier, this operation can imitate the homeostasis functionality for controlling the firing rate of neuron circuits. The initial voltage threshold of each neuron in the proposed neural network is 0.7 V, and Figure 8d,e show the optimized V_{th} of the output neurons and the recognition rate of the proposed system, respectively, for a given MNIST dataset. The recognition rate is an average of 10 runs. The type of MNIST digits can be distinguished better by increasing the number of output neurons in a neural computing system, which leads to highly accurate pattern recognition [20]. The maximum accuracy of the SNN based on the proposed homeostasis functionality reached 91.84% with 200 output neurons. The proposed SNN achieved about an 8% higher recognition rate than an SNN without the homeostasis function. In addition, although the conductance fluctuation of synaptic devices is large ($\sigma/\mu > 0.5$), as shown in Figure 8f, the degradation of the recognition rate was observed to be low (~3%) in the proposed system due to the homeostasis function. However, the recognition rate without the homeostasis functionality was severely compromised as the fluctuation of the synaptic devices increased.

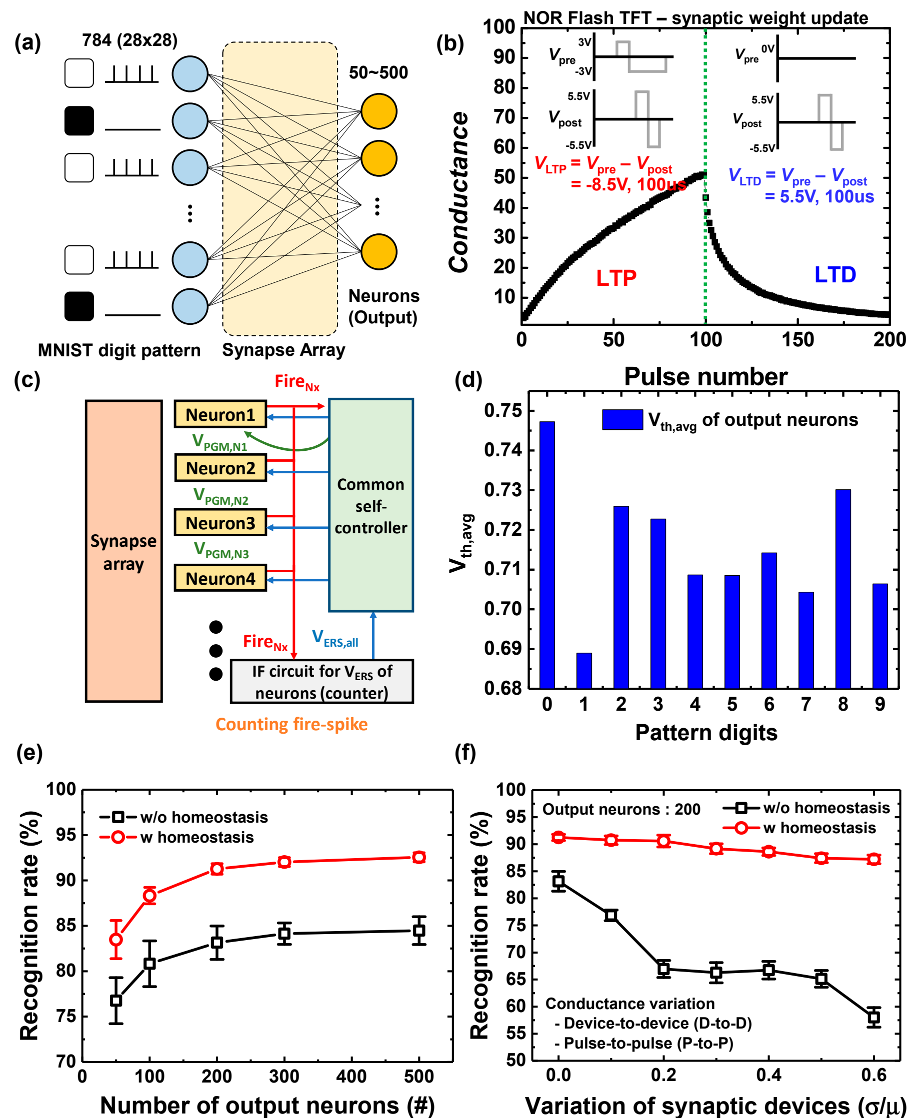


Figure 8. (**a**) A diagram of a fully connected neural network with a synapse array and neurons. (**b**) Synaptic weight updates (LTP/LTD) and operation scheme of a TFT memory device [60] (**c**) A block

diagram of the neuromorphic system consisting of a synapse array, neurons, and a common controller. (**d**) The optimized threshold voltages of output neurons with the input patterns. (**e**) Comparison of the pattern recognition accuracy in STDP based SNN system with/without homeostasis functionality. (**f**) The degradation of the recognition rate with increasing conductance variation (σ/μ) of the synaptic devices.

4. Conclusions

A S-G FET was designed and fabricated in this study to control the threshold of neuron circuits for spiking neural networks. The V_{th} variation of the S-G FET was verified experimentally by applying a V_{PGM} of 7 V and V_{ERS} of −7.5 V to the G2 gate. Even after more than 10^5 program/erase cycles, the gate dielectrics of G1 did not degrade; thus, no change in the SS of G1 was observed. In neuron circuits with the homeostatic function, the recognition rate was improved by 8% by increasing the firing threshold of the circuits. Furthermore, the nonvolatile memory functionality of the charge storage layer in the S-G FET could maintain the thresholds (for over 10^4 s) of the neuron circuits optimized during the SNN's learning process. The proposed homeostatic neuron functionality yielded a high classification accuracy for the MNIST dataset, despite large fluctuations in the synaptic devices in the two-layer SNN.

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