Technical Note

Methods to Create Novel La$_{2-x}$Sr$_x$CuO$_4$ Devices with Multiple Atomically Sharp Interfaces

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Abstract: We present methods to create devices that utilize the high-temperature superconductor La$_{2-x}$Sr$_x$CuO$_4$ grown by atomic layer-by-layer molecular beam epitaxy (ALL-MBE). The ALL-MBE synthesis technique provides atomically precise interfaces necessary for the tunnel junctions, Josephson junctions, and dyon detection devices that will be considered. A series of microfabrication processing steps using established techniques are given for each device, and their details are discussed. These procedures are easily extended to generate more complex designs and could be suitable for a wider variety of materials.

Keywords: superconductivity; cuprates; microfabrication

1. Introduction

The copper oxide materials that superconduct at high critical temperatures (T_c) also display a wealth of other electronic behaviors. In addition to superconductivity [1–6], antiferromagnetic ordering [7–9], spin density wave [10–16], charge density wave [10,14,17–28], Fermi liquid [29–32], strange metal [33–40], and nematic [41–53] behaviors have all been claimed to be observed, depending on the temperature, T, and the doping, x, of the material. While each of these electronic states is interesting in its own right, novel physics and devices can be created when high-T_c cuprate materials of one doping are combined with other cuprates of different doping or even with other non-cuprate materials. Interfaces between differing complex oxides are well known for displaying behaviors that are not observed in their constituent materials [54–58], and cuprates are no exception [59–63]. Heterostructure engineering is also a proposed means for raising T_c, possibly to room temperature [64–66].

An obvious way to create these combinations of cuprates is to use the crystal structure of the component materials to our advantage. The high-T_c cuprates naturally order into a layered perovskite structure with stacks of oxide layers. A deposition method that grows thin films in a layer-by-layer fashion is a perfect match for these systems, as specific blocks of materials can be grown on top of one another in a controlled way to create an engineered heterostructure. One such technique, atomic layer-by-layer molecular beam epitaxy (ALL-MBE), provides this capability and has the added benefit that since the films grow epitaxially, the interfaces between different layers can be essentially perfect [67–69].

Atomic layer-by-layer growth of cuprate heterostructures by molecular beam epitaxy has already generated several exciting results [70]. Devices made with trilayer sandwich-type junctions, using optimally doped La$_{2-x}$Sr$_x$CuO$_4$ (LSCO) for the top and bottom layers and insulating La$_2$CuO$_4$ (LCO) for the middle layers, have demonstrated that the electronic states in the two materials do not overlap [71]. While mutual inductance measurements showed that the optimally doped layers were superconducting, no supercurrent could be

passed across the insulating barrier, even when it was made as thin as one unit cell [71]. This could be explained if the insulating LCO were poisoning several unit cells of the LSCO above and below it, effectively increasing the barrier width for Cooper pair tunneling. However, the inverse heterostructure, with insulating top and bottom layers and a one-unit-cell thick optimally doped middle layer, remained superconducting in mutual inductance measurements [71]. The two phases must separate sharply when optimally doped LSCO and insulating LCO are involved.

This paradigm has been found to not necessarily hold once the doping of one of these two constituent materials is changed. When the superconductor–insulator–superconductor (S-I-S) heterostructure described above is annealed to drive oxygen into the LCO, converting it to $La_2CuO_{4+\delta}$, the barrier is no longer insulating and acts as a metal, even superconducting at some critical temperatures $T_c' < T_c$. When measured at a temperature in the range $T_c' < T < T_c$, so that the $La_2CuO_{4+\delta}$ is in the normal state (N), the device becomes an S-N-S junction that is shown to carry a supercurrent [72]. Unlike S-N-S junctions made from traditional low-T_c materials, the barrier thickness can be very large while maintaining supercurrent, up to two orders of magnitude larger than the c-axis coherence length in LSCO [6]. As it has come to be known, this Giant Proximity Effect points to the fact that the normal state in the high-T_c cuprates is unique.

Another interesting observation can be made at the interface of LCO-LSCO structures when the LCO remains insulating, but the doping of the LSCO is allowed to vary. When the LSCO is so overdoped that it no longer superconducts on its own, if LCO is subsequently grown on top, high-T_c superconductivity is still observed in the overall bilayer structure [59]. In such LSCO/LCO bilayers, T_c varies very little with the LSCO doping [60], with the only substantial difference depending on whether the metallic layer is grown before the insulator or the other way around [61]. Further experiments have proven that high-T_c superconductivity exists in a single copper-oxide plane near the interface [62]. The phenomenon can be attributed to the spillover of charge carriers from the metallic side of the interface to the insulating side [63].

While much has already been achieved, the relevance of cuprate devices with multiple interfaces to current research continues to persist. In what follows, we will discuss how we fabricate specific devices of interest and present some results obtained with these structures. We will begin with some well-established work that we have done making tunnel junctions, explain our current efforts to make c-axis Josephson junctions, and finally give a forward-looking discussion of a proposed dyon detection device.

2. Tunnel Junctions

2.1. Tunnel Junction Fabrication

The method for making tunnel junctions begins with trilayers grown by the ALL-MBE technique. Our atomic fluxes are produced by Knudsen cells, all aimed at one central point where the 10 mm × 10 mm × 1 mm single crystal substrates we grow on are held. The substrates are maintained at a temperature that allows sufficient thermal energy for the incoming atoms to move laterally on the surface of the growing film and find their place within the developing crystal structure but not enough thermal energy that diffusion of atoms throughout the thickness of the film takes place. Oxygen is the only element not deposited in this way and is instead introduced into the film during the growth using pure distilled ozone, a powerful oxidizer. Reflection high energy electron diffraction (RHEED) monitors the crystal structure during growth, providing the real-time feedback the MBE operator uses to steer the growth. Low deposition rates and computer-controlled shuttering of the cells provide fine control over the entire process to better than 1%. This precise control over the stoichiometry of each layer enables the atomic layer-by-layer growth mode necessary for producing heterostructures with sharp interfaces between specifically designed blocks of materials.

The substrates used in this work are single-crystal LaSrAlO$_4$ (LSAO) with a (001) orientation. The a-axis lattice constant of LSAO is very close to the *a*- and *b*-axis lattice constants of LSCO, which coerces the cuprate layers to grow tetragonally along the *c*-axis. At the beginning of each film growth, a thin (0.5—1.0 unit cell) buffer layer of overdoped LSCO is first deposited to initiate good growth. The upper and lower sections of the subsequently deposited trilayers are composed of LSCO, with the middle barrier layer being made from LCO, similar to Ref. [71]. One difference between that study and more recent work [73,74] is that many different junctions with an assortment of strontium contents that range from slightly undoped ($x = 0.10$) to optimal doping ($x = 0.16$) have been made. Additionally, different barrier thicknesses down to 0.5 unit cells have been tested. The last step of each growth is to cap the trilayers, in situ, with a thin layer of gold to protect the surface from the atmosphere.

The first step when making these junctions is to define the overall shape of the bottom electrodes. Since we are making *c*-axis junctions, we cannot easily contact the bottom of the junction as it is anchored to the substrate. Instead, part of the bottom layer of the trilayer serves as one pair of our current and voltage electrodes. The photolithography mask pattern is shown in Figure 1a. After creating this geometry in photoresist on the surface of the trilayer, the pattern is transferred into the film by argon ion milling with a 500 V beam voltage and 2.5 mA/cm^2 ion beam current density.
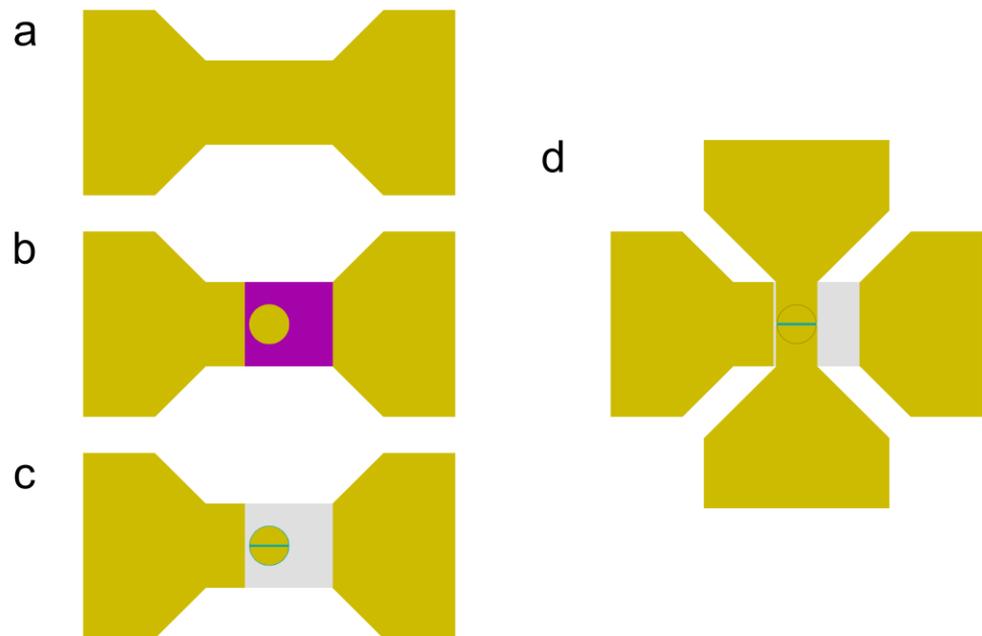

Figure 1. Fabrication scheme for creating high-T_c cuprate tunnel junctions. Gold color represents gold, magenta is the bottom LSCO layer, cyan is the top LSCO layer, and grey is the Al$_2$O$_3$ insulation. Pictures show the top view of the device after each step. (**a**) Overall bottom electrode shape after the first ion milling step. (**b**) Creation of bottom electrodes and mesa structure. (**c**) Insulating layer deposited over bottom electrodes. (**d**) Gold contacts with the top of the mesa.

Once the bottom electrode geometry is defined, we thin those areas that serve as the electrodes while maintaining the trilayer structure of the junction. A round mesa is patterned for the junction area while the trilayer outside of the mesa is thinned by ion milling through the top and middle layers, leaving as much of the bottom layer as possible (Figure 1b). Using a reduced beam voltage and current density so that the etch rate is slower helps with this. Additionally, the thickness of the "dead layer" resulting from ion milling damage can be minimized. The bonding pad areas are not etched, so the pads are thicker and more robust.

Contacts to the top of the mesa are made with gold, but before we can do that, the area around the mesa must be insulated so that the gold does not short the top and bottom of the junction. A double-layer resist process and the mask shown in Figure 1c is used to expose the entire bottom electrode and sides of the mesa and define vias on the top. The exposed in situ gold is removed by wet etching, and then Al_2O_3 is deposited by e-beam evaporation and liftoff. The Al_2O_3 thickness should be at least the same as the depth that was etched through while making the bottom electrode. A subsequent double-layer resist photolithography process, evaporation of gold, and liftoff define the top electrodes and bonding pads (Figure 1d). Typical gold thickness is 100–200 nm, much larger than the Al_2O_3 thickness to cover the Al_2O_3 step sufficiently. While the images shown in Figure 1 only illustrate the creation of one device, in practice, the actual lithography mask contains many copies (of the order 100) of each design with various mesa diameters.

2.2. Tunnel Junction Results

Representative electrical transport data for a high-T_c tunnel junction are shown in Figure 2. Based on the previous measurements in Ref. [71], we expected that we should not observe any supercurrent tunneling across these junctions, which was indeed confirmed in the current–voltage, $I(V)$, measurements. The differential conductance shows a dip near zero bias but does not go to zero, even at the lowest temperatures. At biases outside this pseudogap, the $I(V)$ is non-linear, as observed in other tunneling experiments involving the high-T_c cuprates [73–77].
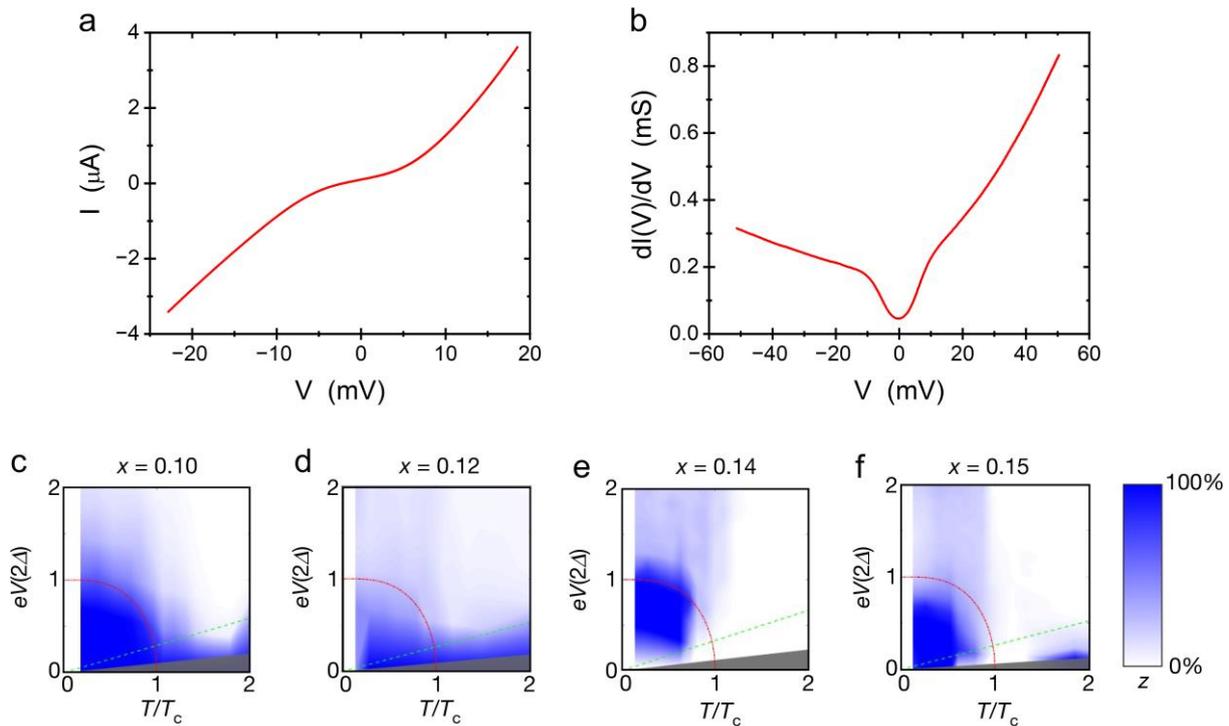

Figure 2. Transport data for tunnel junctions. (**a**) Representative current–voltage and (**b**) differential conductance curves. (**c**–**f**) Fraction of tunneling from paired carriers determined from shot noise measurements as a function of temperature and voltage for samples with differently doped top and bottom electrodes. Adapted from Ref. [73].

Novel results came from shot-noise measurements with these junctions that were used to determine the charge of carriers in the electrodes [73]. At temperatures far above T_c, the noise power spectral density followed the expected $2eI\coth(eV/2k_BT)$ dependence for single electron tunneling. However, as the temperature approached T_c, excess noise was detected, which was attributed to pair tunneling. Fits to the combined function $(1 - z) \times 2eI\coth(eV/2k_BT) + z \times 4eI\coth(eV/k_BT)$ that uses the fraction of pair tunneling,

z, as a fitting parameter, quantified this excess noise. Not only was pair tunneling observed above T_c, but also below T_c for voltages outside the gap, $V > \Delta$. This was true of all doping levels used for the upper and lower electrodes ($x = 0.10$–0.15).

3. Josephson Junctions

3.1. Josephson Junction Fabrication

Junctions based on an LCO barrier are unsuitable for fabricating *c*-axis high-T_c superconductor S-I-S Josephson junctions. The focus of our current research in this area is the exploration of different non-cuprate complex oxides that could provide a suitable barrier that would allow coherent tunneling and the observation of the Josephson effect. In this work, we have made a few improvements to the previous device geometry [78].

The first is to prepare the sample for the top electrode from the beginning. As we will see, this eliminates the need for an insulator deposition step around the entirety of the junction and possible leakage current to the bottom electrode. We start with a trilayer structure as before, although now the barrier is not LCO but some other oxide that grows epitaxially with LSCO, such as LSAO. Half of the film where the device will be created is masked off, and the other half is ion-milled completely away, all the way down and slightly into the substrate. This area is then backfilled with Al_2O_3 in a self-aligned manner with an Al_2O_3 thickness that exceeds the depth that was etched so that Al_2O_3 protrudes above the surface of the cuprate film (Figure 3a). The overall device geometry is then patterned into the film using photolithography and ion milling (Figure 3b). This is a more complicated design than the one presented in Section 2, with provisions for multiple contacts. These will allow for separately characterizing the upper electrodes, lower electrodes, and the junction area, as will become apparent from the following steps.
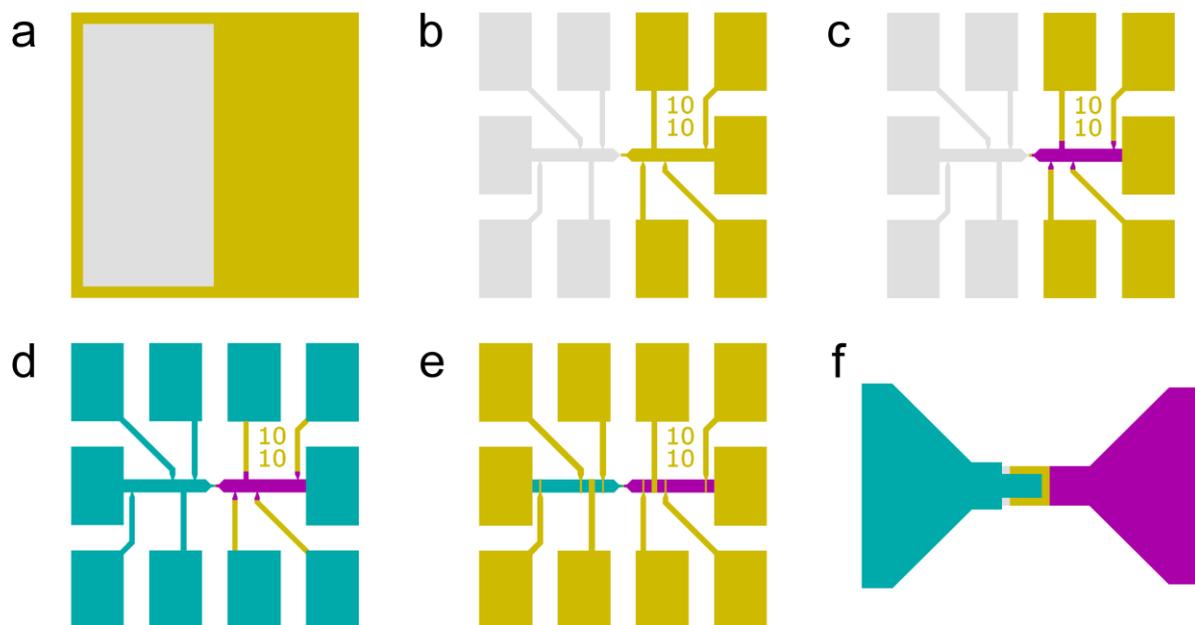

Figure 3. Fabrication scheme for creating high-T_c Josephson junctions. Gold color represents gold, magenta is the bottom LSCO layer, cyan is the top electrode, and grey is the Al_2O_3 insulation. Pictures are a top view of the device after each step. (**a**) Replacement of half of the cuprate film by Al_2O_3 in preparation for the top electrode. (**b**) Defining overall device shape. (**c**) Creation of bottom electrode. (**d**) Deposition of top electrode metallization. (**e**) Deposition of gold contacts and bonding pads. (**f**) Zoomed-in view of Josephson device area after all fabrication steps are finished. Adapted from Ref. [78].

We proceed now as before by thinning the portion of the trilayer that will become the bottom electrode (Figure 3c). Reduced ion beam voltage and current density are used again to help stop at the correct depth and minimize damage to the remaining layers. Any of the multitudes of contact pads in this design could also be used for test etchings to calibrate the proper ion milling time. The final steps in this scheme involve depositing the top electrode (Figure 3d) and extra gold for bonding pads (Figure 3e). Here, we use a stack of niobium, titanium, and gold for the top electrode. The only caveat here is that the thickness of this metallization should be larger than the thickness of the Al_2O_3 layer deposited at the beginning that projected above the film surface so that that step is completely covered. Using a superconducting material for the top electrode eliminates the electrode resistance, measured in series with the junction when the niobium goes superconducting. This, in turn, allows for smaller junction areas to be produced as we only need to make one contact with the top of the trilayer. An additional benefit is that superconducting electrodes open the door for more complicated superconducting circuits.

3.2. Preliminary Measurements

Several hundred devices have been fabricated to date following the above procedure. We have verified previous results using LCO as a barrier and have begun testing other complex oxides to try and observe the Josephson effect in *c*-axis junctions. In Figure 4, we show some results using a single stoichiometric layer as a barrier. In Figure 4a, we show the superconducting transition of a representative trilayer measured by mutual inductance immediately after film growth, i.e., before any fabrication steps were performed, and compare that to the resistive transition of the bottom electrode of some finished devices, all fabricated from the same film. The processing has not degraded the bottom electrode layers as the temperature that resistance goes to zero corresponds precisely with the temperature at which the mutual inductance signal drops or, equivalently, the temperature that screening sets in, as would be anticipated.

The superconducting transition of a few top electrodes is shown in Figure 4b. They are reproducible and reasonably close to the expected T_c of bulk niobium. Although both the top and bottom electrodes are superconducting, we still do not observe any supercurrent across the junction (Figure 4c), even for nominal barrier thicknesses as low as 6 Å. We believe that in the case of LSAO, the barrier material disrupts the superconductivity in the cuprate layers immediately next to this layer, effectively expanding the tunneling barrier [79]. Transport measurements in devices using La_2ZnO_4 for the barrier material have yielded similar results.
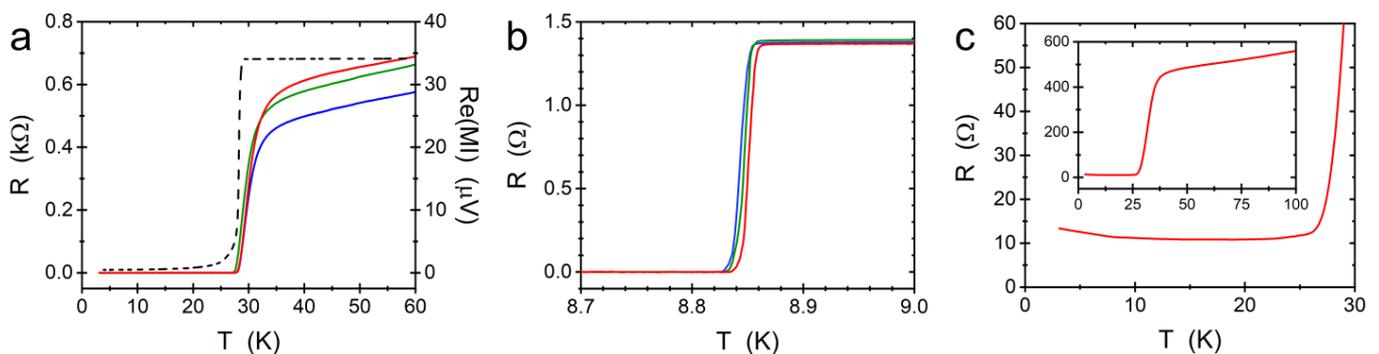

Figure 4. Preliminary results with latest attempts at Josephson devices with LSAO barriers. (**a**) The superconducting transition of a trilayer after growth was measured by mutual inductance (dashed line). This is compared to resistive transitions of some bottom electrodes after all fabrication steps were completed (solid lines). (**b**) Transitions of several top electrodes. (**c**) Resistance of a representative junction shows a transition due to the bottom electrode but does not go to zero and increases with cooling.

In the past, the main impediment to the reproducible fabrication of *c*-axis Josephson junctions was believed to be the creation of ultrathin yet pinhole-free barrier layers and sharp interfaces, which are necessary due to the extremely short *c*-axis coherence length in high-T_c cuprates. While the result shown in Figure 4c is not what was hoped for, it is still a testament to the perfect interfaces created by this technique that begins with ALL-MBE, as the many junctions we have tested are undoubtedly free of pinholes. Currently, finding a suitable barrier material with a good lattice match that does not deplete carriers or otherwise destroy superconductivity in the neighboring LSCO layers remains the main challenge to overcome. There are many other known insulators yet to try. Still, we must consider the possibility that the best barrier material may not naturally occur but can be created in very thin films under epitaxial strain, requiring much more time and effort to discover. Making good contacts that do not cause any heating to the top and bottom of the junctions is another issue that needs to be overcome for accurate measurements. The all-superconducting contacts presented here are a good step towards solving this problem. Still, until a noticeable Josephson effect is observed, we will not know if our top contact materials and geometry are optimized for this purpose.

4. Dyon Detectors

Proposed Dyon Detector Fabrication

Finally, we briefly discuss the possible fabrication steps involved in a detector for dyons. These exotic low-energy excitations that carry both electric and magnetic charge have been predicted to exist in underdoped cuprates [80]. By the symmetric version of Maxwell's equations, which include magnetic charges and currents, a wire carrying a dyon current would produce a circumferential magnetic field from the electric component of the current and a circumferential electric field from the magnetic component of the current. This electric field could be detected by a coil constructed around the wire, much like a pick-up coil can detect the induced EMF of a time-varying magnetic field passing through it.

The fabrication scheme we have proposed [80] would be difficult to realize but certainly is within the realm of current technical capabilities. It relies on removing a film grown by ALL-MBE from the vacuum chamber where the growth was performed, carrying out some processing steps, and then reinserting the processed film back into the MBE chamber for subsequent growth. This procedure relies on controllably heating the sample in the presence of ozone, which cleans contaminants from the film while monitoring the condition of the surface by RHEED until a crystalline surface is again achieved. At this point, a new ALL-MBE synthesis step may take place.

Our proposed process [80] begins by growing a layer of optimally doped LSCO followed by pattering by photolithography and then ion milling to establish one side of the detecting coil (Figure 5a). The film is then reinserted into the MBE chamber where a layer of LSAO is grown. This is subsequently patterned to leave a patch of insulator on the LSCO where the (predicted) dyon carrying wire will be placed (Figure 5b). The sample goes back into the MBE chamber again, and another layer of optimally doped LSCO that will form the basis of the wire is grown. Another round of lithography and ion milling defines the dimensions of the wire as well as its contacts (Figure 5c). Once more, a layer of LSAO is grown and patterned so that a patch remains to insulate the second half of the coil (Figure 5d). The last MBE growth and successive patterning and etching creates the second half of the coil (Figure 5e), after which lithography, metallization, and liftoff create gold contact pads for the biasing and detection (Figure 5f).
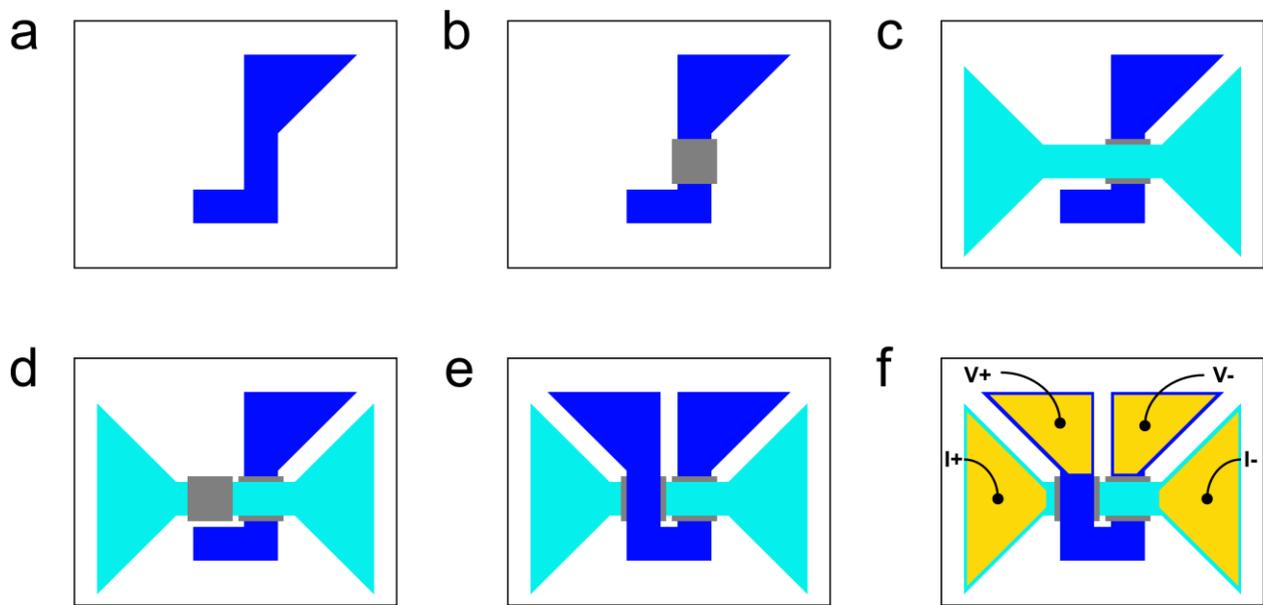
Figure 5. Proposed fabrication steps for creating a dyon detection device. (**a**) Patterning LSCO to form one side of the detection coil. (**b**) Creating a patch of LSAO to insulate the right side of the coil from the wire made in the next step. (**c**) Creating the LSCO wire that will be used to drive current. (**d**) Creating another patch of LSAO to insulate the wire from the left side of the coil that is made next. (**e**) Patterning LSCO to form the left half of the coil. (**f**) Deposition of bonding pads. Adapted from Ref. [80].

As mentioned above, this is a very demanding set of steps to be followed if the dyon detection device, as proposed here, is to become a reality. Care must be taken during the ion milling steps to minimize over-etching. The subsequently deposited layers need to be thick enough to overcome step edges created by the previous microfabrication processes. This demands careful characterization of each step and coordination among all those involved in the growth and processing stages of the device creation. Nevertheless, none of the individual processes are infeasible. Creating a dyon detection device in this manner, which should give maximum sensitivity due to its minimized active area, could be realized.

5. Conclusions

In the preceding sections, we have presented methods to create devices of interest from high-T_c cuprates grown by ALL-MBE. The atomically precise interfaces are necessary for the tunnel junctions, Josephson junctions, and dyon detection devices to be realized. The procedures given here, based on ALL-MBE, for creating such structures can be easily extended to generating more complex designs, such as Josephson junction arrays, superconducting interference devices, or more sensitive dyon detection devices with multiple coils. With careful consideration and testing, they may also be suitable for a wider variety of materials.

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Conflicts of Interest: The authors declare no conflict of interest.

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