instruments

MDPI

Article

Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution

Frédéric Nolet *, Samuel Parent, Nicolas Roy, Marc-Olivier Mercier, Serge A. Charlebois, Réjean Fontaine and Jean-Francois Pratte

Interdisciplinary Institute for Technological Innovation and Department of Electrical and Computer Engineering, Université de Sherbrooke, Sherbrooke, QC J1K 2R1, Canada; Samuel.Parent@USherbrooke.ca (S.P.); Nicolas.Roy6@USherbrooke.ca (N.R.); Marc-Olivier.Mercier@USherbrooke.ca (M.-O.M.); Serge.Charlebois@USherbrooke.ca (S.A.C.); Rejean.Fontaine@USherbrooke.ca (R.F.); Jean-Francois.Pratte@USherbrooke.ca (J.-F.P.)

* Correspondence: Frederic.Nolet@USherbrooke.ca; Tel.: +1-819-821-8000 (ext. 65795)

Received: 29 June 2018; Accepted: 20 September 2018; Published: 22 September 2018

Abstract: This paper presents a new quenching circuit (QC) and single photon avalanche diode (SPAD) implemented in TSMC CMOS 65 nm technology. The QC was optimized for single photon timing resolution (SPTR) with a view to an implementation in a 3D digital SiPM. The presented QC has a timing jitter of 4 ps full width at half maximum (FWHM) and the SPAD and QC has a 7.8 ps FWHM SPTR. The QC adjustable threshold allows timing resolution optimization as well as SPAD excess voltage and rise time characterization. The adjustable threshold, hold-off and recharge are essential to optimize the performances of each SPAD. This paper also provides a better understanding of the different contributions to the SPTR. A study of the contribution of the SPAD excess voltage variation combined to the QC time propagation delay variation is presented. The proposed SPAD and QC eliminates the SPAD excess voltage contribution to the SPTR for excess voltage higher than 1 V due to its fixed time propagation delay.

Keywords: single photon avalanche diode; quenching circuit; single photon timing resolution; SiPM; 3D digital silicon photomultiplier; 3D integrated detector; time-of-flight; positron emission tomography

1. Introduction

Single photon avalanche diodes (SPAD) are solid-state detectors used for applications requiring high timing resolution and single photon sensitivity, including positron emission tomography (PET) [1–5], fluorescence lifetime imaging microscopy (FLIM) [6,7], Raman spectroscopy [8,9], optical communication [10,11] and 3D ranging [12–14]. In clinical PET, time-of-flight (ToF) improves the positron–electron annihilation localization along the line of response resulting in a better contrast to noise ratio in the reconstructed image [15]. However, to improve significantly the contrast in the image of preclinical PET scanners, one must achieve tens of ps full width at half maximum (FWHM) of coincidence timing resolution (CTR) [16,17].

To achieve such high timing resolution, both the scintillator and the photodetector must be improved. The current scintillators used in PET (lutetium oxyorthosilicate (LSO) type crystals) are limiting the timing resolution to the order of 100 ps [16]. Using different mechanisms such as hot intraband luminescence [18] or quantum confinement in nano-scintillators [19,20], it is possible to increase the number of prompt photons to improve significantly the timing resolution. This paper focus on the development of the photodetector and its associated electronics to be used with these

scintillators. On the photodetector side, the single photon timing resolution (SPTR) must be improved to the order of tens of ps FWHM to reach a CTR of tens of ps FWHM with the fast scintillators [20].

The SPTR is the timing jitter of the whole detector, including its readout electronic, when triggered by a single photon. While applications such as rangefinders minimize this jitter by averaging multiple measurements, ToF-PET and time imaging calorimeter require optimized SPTR for single event time arrival detection. Furthermore, in low-light detection applications such as Cherenkov radiators or Cherenkov PET detectors [21–23], the SPTR is critical since very few photons are emitted, hence detected.

One of the main challenges for SPAD-based detectors is combining both high photodetection efficiency (PDE) and high SPTR. At this level, commercially available SiPMs offer high fill factor and PDE but suffer from a limited SPTR coming from their parallel and distributed architecture for two reasons: (1) since all SPADs are connected in parallel, the detector has a high output capacitance which directly affects the rising edge slope (lower $\frac{dV}{dt}$) [24,25] of the output signal; and (2) each SPAD has a timing skew coming from the SPAD-to-output distance mismatch [25,26].

Unlike in an analog SiPM, SPADs in a digital SiPM designed on a 2D ASIC (application specific integrated circuit) are readout individually by a quenching circuit (QC), eliminating the effect of the high output capacitance at the cost of a lower fill factor. Similarly to an analog SiPM, a digital SiPM has routing skew between each QC and the time-to-digital converter (TDC) usually located in the ASIC periphery [1,27,28]. These contributions constrain the SPTR of such detectors to hundreds of ps FWHM [1,24–29].

We propose to use a 3D digital SiPM as a solution to all aforementioned problems (Figure 1) [30–33]. In this approach, different silicon tiers dedicated to specific functions are stacked and routed using vertical interconnections. For example (Figure 1), a top layer could include a SPAD array designed in an optoelectronic technology with through silicon vias (TSV) to interconnect to the second tier, which could be implemented in a deep submicron technology node to optimize both timing measurements and data processing. To optimize the timing performance, a QC and a TDC integrated per pixel provides means to characterize and correct the SPAD-to-SPAD skew. Since the pixel size is in the order of 50 × 50 µm^2 range and performance under 10 ps is mandatory for some of the aforementioned applications, every individual contribution in timing and size must be optimized. The TDC developed to be integrated in the pixel has a timing jitter of 6.9 ps rms [33] and the first results of a 2D pixel in CMOS 65 nm has a 17.5 ps FWHM SPTR [34].

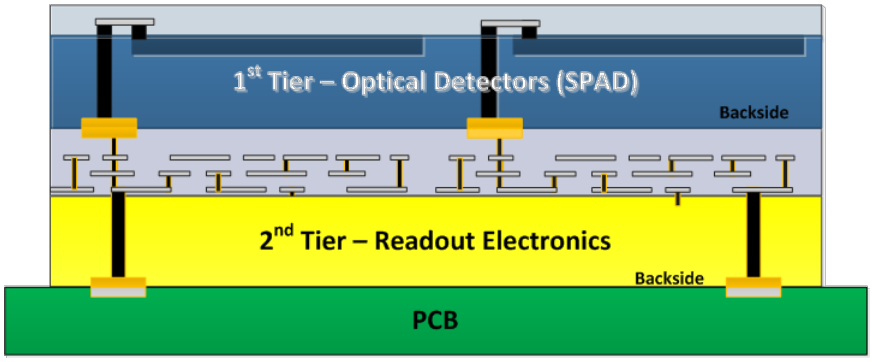

Figure 1. Cross-section of the 3D digital SiPM. The first tier contains SPAD arrays with through silicon vias (TSV) and the second tier contains quenching circuit and time-to-digital converter arrays.

To obtain a SPAD array with a 10 ps SPTR, the first step is to achieve a single SPAD and quenching circuit that can reach a SPTR of 10 ps. Many developments have been made to improve quenching circuits regarding the low area and the timing precision [35–40]. Furthermore, developments have been made on SPAD to optimize the SPTR such as a shallow trench isolation (STI) architecture to reduce the diffusion tail of the SPAD to reach a SPTR of 27 ps FWHM for a 14 µm SPAD [41]. In other development, an edge covering was added to the SPAD and it lowered their SPTR from 40 to 20 ps

FWHM with a 20 µm SPAD [26]. On the quenching circuit side, an external timing pick-off circuit with a low threshold was developed and obtain similar SPTR characteristics with a different SPAD diameter: 32 ps FWHM for 20 µm SPAD, 34 ps FWHM for 50 µm SPAD and 35 ps FWHM for a 100 µm SPAD [42]. An SPTR of 20 ps FWHM was measured with a single SPAD of 50 µm at cryogenic temperature [43]. Still, there is not a SPAD and QC architecture that reached a SPTR of 10 ps for a single SPAD.

This paper presents a fully integrated QC designed in TSMC CMOS 65 nm for high timing precision with low jitter and an optimized architecture for low time propagation delay variation. The objective is to reach a 10 ps FWHM SPTR at the SPAD and QC level. This paper also provides a better understanding of the SPAD excess voltage variation impact on the SPTR. The implemented QC occupies 30 $\times$ 18 µm^2 and uses an integrated fast comparator with an adjustable threshold to optimize the timing jitter of the photodetector. Section 2 presents the architecture and the design considerations, Section 3 presents the materials and methods and Section 4 contains the results obtained with the 2D version of the detector. Section 5 presents the discussions and Section 6 provides the conclusions.

2. Architecture

2.1. Quenching Circuit

The proposed QC is a passive quenching with an active recharge and can be divided into four sections: the recharge transistor, the quench transistor, the comparator and two monostable circuits for the programmable hold-off and recharge time (Figure 2). The transistors routed to the SPAD are 3.3 V transistors, hence setting the SPAD excess voltage limit. The recharge transistor was designed to provide 1 mA for sub-ns recharge for the full input capacitive load (SPAD, TSV and the TSV contact). The quenching path is composed of two transistors in series: a cascode 3.3 V transistor that limits the current and a second transistor switches off the branch when a hit is detected and hold it off during the hold-off time.

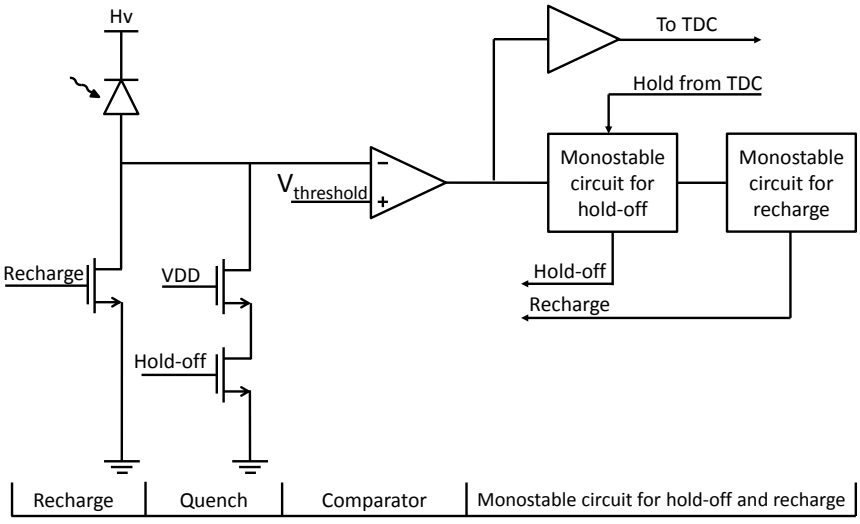

Figure 2. Overview of the SPAD and QC implemented in CMOS 65 nm.

The QC was designed to obtain high single photon timing resolution. To this end, an open-loop operational amplifier (Op-Amp) was used as a fast comparator with the advantage that the trigger following the crossing does not suffer from the time walk of a typical comparator with hysteresis. That said, the circuit is still immune to noise and undesired triggering as the SPAD is in a hold-off following the detection of an event. The Op-Amp was designed to obtain both low time propagation delay variation and low jitter as a function of input signal variations [44]. The Op-Amp is used as a leading edge discriminator. For a non-optimized discriminator, a variation in the input signal

amplitude will impact the time propagation delay of the discriminator. This variation, if not compensated or minimized, will add up to the jitter of the detector. To this end, the Op-Amp was designed to minimize the time propagation delay variation caused by the undervoltage and overvoltage variation in regards to the Op-Amp threshold. This will minimize the jitter caused by the amplitude signal build-up at the SPAD and QC interface. The Op-Amp threshold is adjustable from an external control from a few mV up to 2.5 V to select the optimal voltage threshold in the rising signal from the SPAD readout by the QC. The Op-Amp has a size of 13 × 8 µm^2.

Figure 3 shows the two stage Op-Amp used as a comparator. Since the QC must sustain 3.3 V, the transistors used in the differential input pairs (M2-M3) and the current source (M1) are 3.3 V transistors. M4-M13 are standard 1 V transistors to match the subsequent electronics supply. Consequently, the Op-Amp simultaneously acts as both a discriminator and a level down shifter from 3.3 V to 1 V. The input pair is PMOS based to optimize the timing performance of the Op-Amp when the threshold is close to 0 V. M13 acts as a switch to turn off the QC by forcing the Op-Amp output at a high level resulting in a hold-off state of the QC. M12 is a cascode transistor to limit noise injection to the differential input pair from the subsequent circuits, in this case, a TDC.

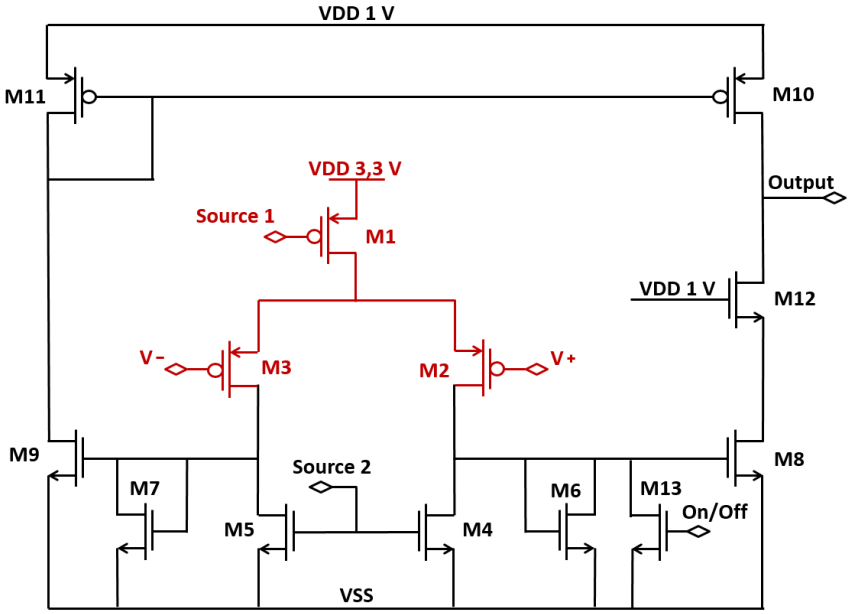

Figure 3. The two-stage operational amplifier used as a discriminator in the quenching circuit. M1–M3 are high voltage transistors (3.3 V) to sustain higher excess voltage and M4–M13 are 1 V transistor to match the subsequent electronics.

The last section of the quenching circuit is monostable circuits required for both the programmable hold-off and recharge time. The hold-off defines the time a SPAD is intentionally turned off to minimize afterpulsing coming from trapped charges in the SPAD. The hold-off thus limits the correlated avalanche rate. The TDC also gives a feedback to maintain the QC in hold-off during its conversion time. Since the QC must address different SPAD designs in size/technologies where the threshold must be tailored to, the recharge time is also programmable. An adjustable recharge time can help minimize the undesired dead time while assuring a long enough recharge time to fully recharge the SPAD. The QC has a total size of 30 × 18 µm^2 including the top contact for the TSV connection of the 3D digital SiPM architecture to be developed.

2.2. Single Photon Avalanche Diode

Figure 4 shows a cross section of the 32 sided polygon SPAD made in CMOS 65 nm. The SPAD is a standard p^+ implantation (anode) in an n-well (cathode) with a p-well guard ring. A polysilicon layer (gate) was used as blockages for shallow trench isolation (STI) to minimize its effect on the guard ring and on the dark count noise (DCR) [41]. The SPAD active area is 20 µm. The SPAD has a standard architecture and is expected to have low photodetection efficiency (PDE) and high DCR, but its low capacitance and low area make it suitable for high timing precision measurements.

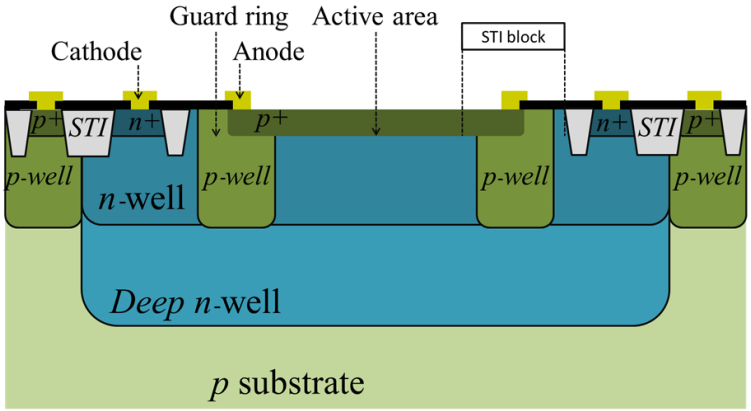

Figure 4. SPAD cross-section: p^+ anode within an n-well cathode with a p-well guard ring.

3. Materials and Methods

For test purposes, the ASIC is wirebonded on a dedicated daughterboard and powered using a motherboard, both custom designed (Figure 5). The motherboard contains an FGPA with the aim to communicate and configure the ASIC. The daughterboard is designed to fit on an optical test setup, giving the flexibility to connect different ASIC on the same motherboard. The proper supply circuits and event generator circuits used for timing measurements are on the daughterboard.

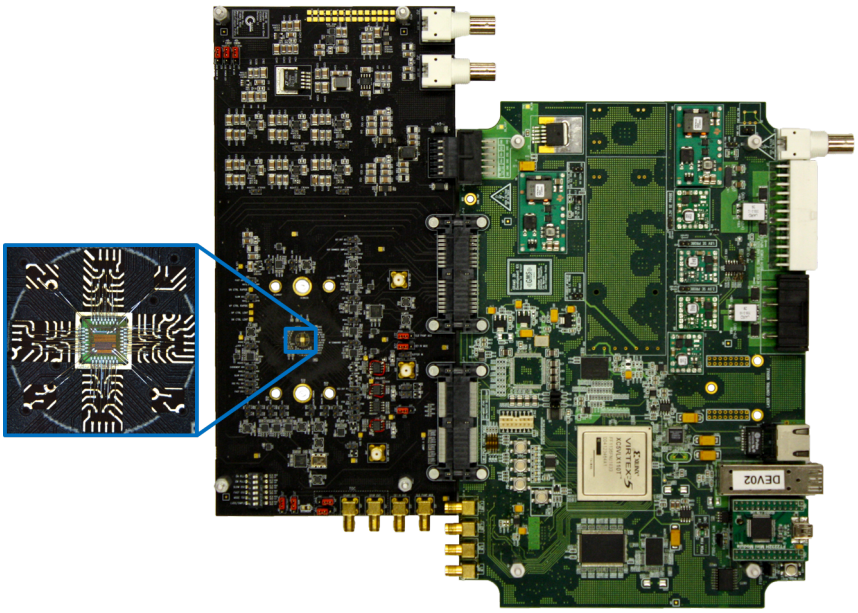

Figure 5. PCB test fixture: the motherboard with an FPGA (**right**) and the daughterboard where the ASIC is wirebonded (**left**).

3.1. Quenching Circuit Characteristics

The quenching circuit characteristics such as the dead time, the hold-off time, the recharge time and the power consumption must be measured. The QC output pulse width is the sum of the hold-off time and the recharge time. By measuring its width, it is possible to determine the QC dead time and thus the maximum count rate of the QC.

A second output was added to the QC to determine the hold-off and recharge time. The second output signal is the recharge pulse only. By measuring the recharge pulse width, one can determine the recharge time and also the hold-off time by subtracting the recharge pulse width from the QC pulse width.

The power consumption depends on the count rate and on the Op-Amp bias current source that has an impact on the timing jitter. Three measurements were made at 25 µA, 50 µA and 100 µA current sources with count rate of 1 kcps and 1 Mcps. The measurements presented in the subsequent section were performed with a current source of 50 µA unless otherwise specified.

3.2. Quenching Circuit Electronic Timing Jitter

The QC timing jitter measurements use a fast input buffer on the daughterboard designed to minimize the jitter due to the signal rise time. The input signal is buffered using a LTC6957 to minimize the effect of its rise time (400 ps over 1 V) on the timing jitter of the QC. The signals were measured with an Agilent MSO-X 90324A, with 80 GSPS, 13 GHz vertical bandwidth and differential probes. Three different measurements were made using the setup shown in Figure 6. First, the timing jitter of the test setup (input buffer, output buffer and the oscilloscope) was measured using probe 1 and probe 3. Second, the timing jitter of the quenching circuit and the input/output buffer was measured using probe 1 and probe 2. From these two measurements, the quenching circuit contribution can be obtained. The timing jitter is measured with a threshold sweep from 1 mV to 700 mV for 1 V input steps and from 1 mV to 2500 mV for 3.3 V input steps. Third, the time propagation delay of the quenching circuit is measured to determine its variation as a function of overvoltage (0 V to 2 V) and threshold level (100 mV to 1 V) using probe 1 and probe 2.

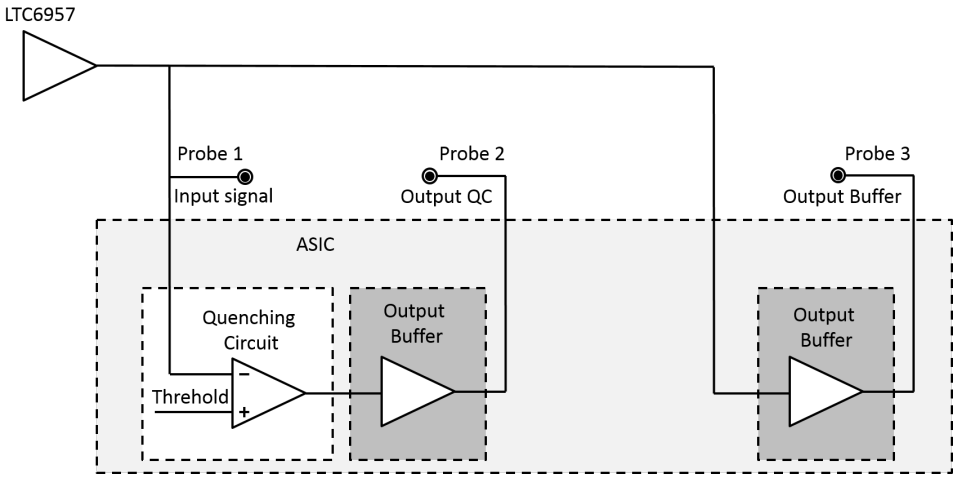

Figure 6. Simplified integrated electronics diagram of the timing setup for the quenching circuit.

3.3. Single Photon Timing Resolution

During the SPAD and QC SPTR measurements, the SPAD is illuminated by a Spectra Physics Mai Tai 80 MHz Ti:Sapphire pulsed laser (Figure 7). The pulse width is specified to be <100 s, which means that the laser contribution to the jitter is negligible. The test setup contribution including the laser, reference diode, oscilloscope and probe is measured at 3 ps FWHM. An optical parametric oscillator can tune the wavelength from 345 nm to 2500 nm (410 nm was used for the measurements). The light is attenuated with neutral density filters to ensure the measurements are made in a photon starved

environment. The beam intensity is measured using an 818-UV Newport diode and a 1918-R Newport power meter to evaluate the number of photons hitting the SPAD. The laser has been attenuated so that the average number of photons per pulse reaching the SPAD avalanche region is lower than 0.04. The timing jitter measurements are acquired with a Teledyne Lecroy SDA 6000A oscilloscope, with 20 GSPS, 6 GHz vertical bandwidth, an active probe and a Becker and Hickl PHD 400 fast diode as the reference timing detector. The light spot from the laser is defocused using the microscope lens so that the spot has a >5 mm diameter to ensure a good illumination uniformity over all the SPAD active region.The SPTR measurements are performed as a function of QC threshold (1 mV up to 1.6 V) and excess voltage (0.5 V to 1.75 V).

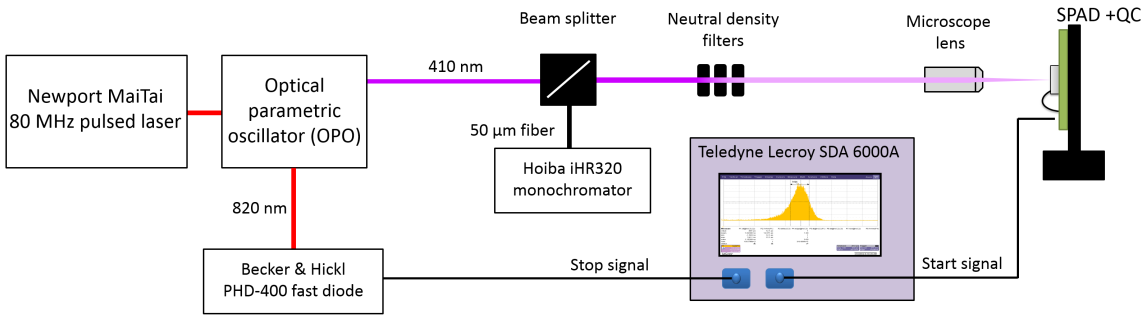

Figure 7. Optical setup used for the single photon timing resolution and the photodetection efficiency measurements of single SPAD.

3.4. SPAD Characteristics

The SPAD is characterized using the methods presented in [30,45] with the test setup presented in Figure 7. The SPAD breakdown voltage was measured using IV curves. The DCR and afterpulsing are measured as a function of the SPAD excess voltage (0.5 V to 1.5 V) at a room temperature with a hold-off of 100 ns. The single SPAD photon detection efficiency (PDE) is measured at a SPAD excess voltage of 1.5 V and wavelength from 400 nm to 700 nm. For the PDE measurements, the light spot is focused within the center of the SPAD active area using the microscope lens (5 µm spot size) (Figure 7). To make sure that the high DCR/dead time did not saturate the SPAD, a 10 ns hold-off was used to get a maximum count rate of 100 MHz with the SPAD. The DCR of <1 MHz represents a dead time of 1% compared to the maximum count rate.

3.5. SPAD Excess Voltage Variation

The SPAD excess voltage varies within a single SPAD and there are many possible factors. It is important to note that a variation of the SPAD breakdown voltage results in a SPAD excess voltage variation if the high voltage (HV) supply is fixed. There are two external factors that can have an impact on the measured excess voltage. A variation of the HV supply for a fix SPAD breakdown voltage will be seen as a variation of the excess voltage (the one use in this measurement has a sub mV variation). A temperature variation will vary the SPAD breakdown voltage and will result in a variation of the SPAD excess voltage to be quenched. The variation of the excess voltage can also be from SPAD internal contributions. These variations can be due to electric field variation within the SPAD active area, the position of the seed of the avalanche, the statistical build-up of the avalanche or a combination of them. Using the QC adjustable threshold, it is possible to measure the excess voltage that is quenched in order to stop the avalanche and see its variation between each avalanche. This measurement is done in two steps. First, the voltage comparator must be characterized to determine its discrimination threshold variation. Second, the adjustable threshold of the comparator is used to measure the variation of the quenched excess voltage applied to the QC.

An ideal comparator exactly discriminates if the input signal is below or over the threshold. In reality, the comparator slowly starts to discriminate the input signal as the amplitude approaches the threshold level. The setup presented in Figure 6 is used with step signals of varying amplitude and a fixed threshold to produce the discriminator S-curve, from which the discrimination range in mV around the threshold is extracted. More specifically, taking the derivative of the S-curve highlights this range and qualifies the discrimination noise. A sweep of ±50 mV around the threshold was used for this measurement.

Once the comparator has been characterized on a dedicated test circuit, the same measurement is done on a second test circuit where a SPAD is directly connected at the input of the QC. Since it is the SPAD excess voltage variation that must be characterized, instead of varying the input amplitude, the QC threshold is varied from ± 50 mV around the SPAD excess voltage. The resulting S-curve was differentiated to determine the variation of the excess voltage in FWHM.

3.6. Timing Jitter Due to the SPAD Excess Voltage Variation

This measurement combines the results of the time propagation delay of the QC and the SPAD excess voltage variation. The SPAD excess voltage variation is an input signal variation of the QC. This variation has an effect on the time propagation delay which impacts the SPTR. The SPAD excess voltage variation measurement is a histogram representing the different SPAD excess voltage applied to the QC. By transposing the value of time propagation delay of the QC associated to the SPAD excess voltage, the timing jitter contribution of these combined measurements is obtained.

4. Results

4.1. Quenching Circuit Characteristics

The QC programmable hold-off is measured and ranges from 2 ns up to 100 ns. The programmable recharge is measured and ranges from 2 ns up to 10 ns. The total dead time of the QC is the sum of both the programmable hold-off and recharge times, which ranges from 4 ns to 110 ns. This provides a maximum count rate of about 250 Mcps. The power consumption of the QC is 85 µW, 170 µW and 340 µW at a count rate of 1 kcps for the Op-Amp current source of 25 µA, 50 µA and 100 µA, respectively. At a rate of 1 Mcps, the power consumption of the QC is 115 µW, 200 µW and 370 µW.

4.2. Quenching Circuit Electronic Timing Jitter

The timing jitter of the setup is measured at 1.7 ps rms (∼4 ps FWHM). This represents the timing resolution lower boundary of the setup for a 1 V input signal.

Figure 8 presents the timing jitter of the QC in response to pulse generator stimuli. For the 1 V input amplitude, the timing jitter varies between 4 ps and 4.4 ps FWHM for a threshold lower than 0.5 V (Figure 9). For a threshold higher than 0.6 V, the timing jitter deteriorates due to the contribution of the input signal roll-off.

The timing jitter for the 3.3 V input step varies between 3 ps and 4 ps FWHM for a threshold between 5 mV and 2 V. At low threshold (sub 50 mV), the jitter slightly deteriorates due to a limitation in the Op-Amp. The lowest timing jitter corresponds to a 1.5 V threshold (1.3 ps rms or about 3 ps FWHM). The better balance of the Op-Amp's underdrive and overdrive explains this result. The timing jitter increases around 2.5 V (comparator discrimination limit and input signal roll-off contribution).

Figure 10 shows the time propagation delay of the quenching circuit as a function of the overvoltage and of the threshold. The overvoltage corresponds to the input applied voltage minus the threshold. The time propagation delay reaches stability above 1 V of overvoltage for a fix threshold. The threshold must be stable in order to minimize its impact on the timing performance. One could define the slope of the flat region as a metric to highlight the timing impact of the time propagation delay. In the present case, the value is ~3 ps/100 mV for the overvoltage.

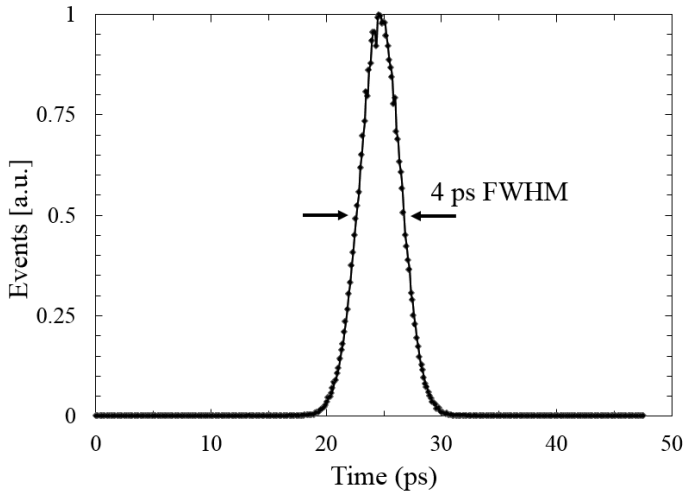

Figure 8. Histogram of the QC timing jitter in response to a 1 V step with a 200 mV threshold.

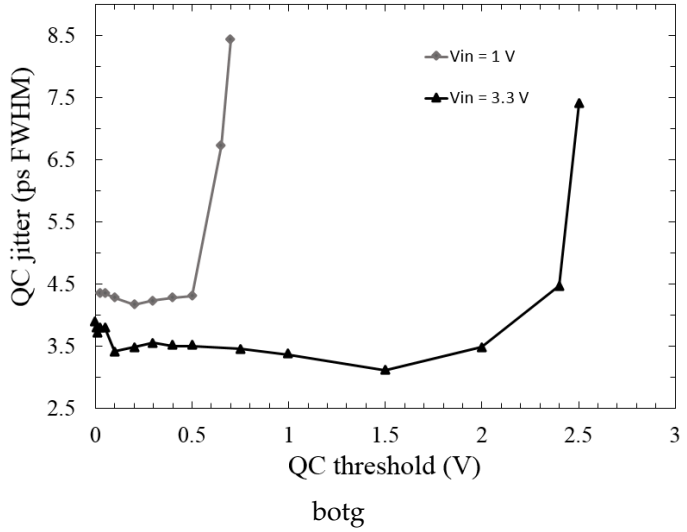

Figure 9. QC timing jitter as a function of the threshold.

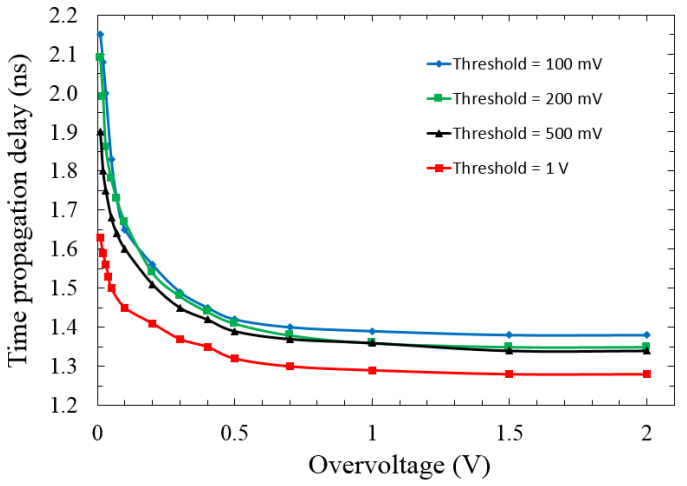

Figure 10. QC time propagation as a function of the overvoltage. The overvoltage corresponds to the input applied voltage minus the threshold.

4.3. Single Photon Timing Resolution

Figure 11 shows the SPTR of the 20 µm SPAD and the QC. The measured timing jitter is 7.8 ps FWHM. This includes the test setup contribution measured at 3 ps FWHM (oscilloscope and probe). Hence, the corrected SPTR of the SPAD and QC is $\sqrt{\left(7.8^2 - 3^2\right)}$ = ~7 ps FWHM considering that the contributions are not correlated. The second peak at 65 ps is a reflection in the optical setup.

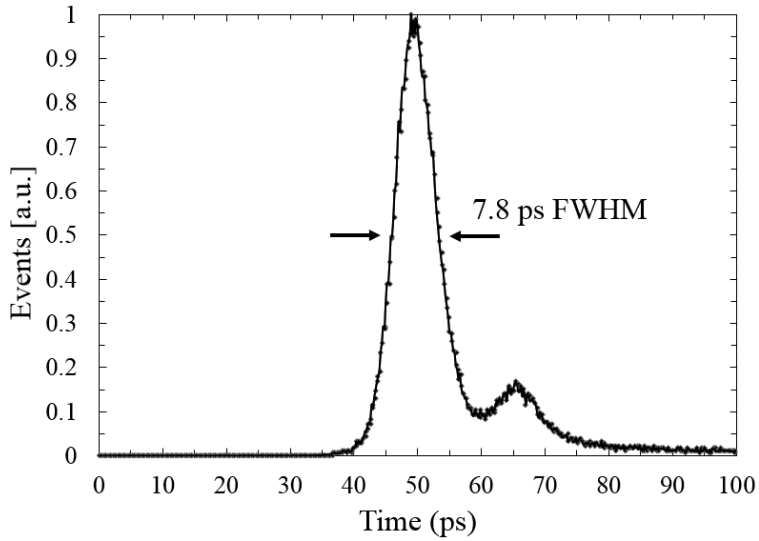

Figure 11. Histogram of the SPAD and QC SPTR at 1.75 V of excess voltage with a 100 mV threshold at a wavelength of 410 nm.

Figure 12 presents the effect of the QC threshold on the timing jitter of the detector for multiple excess voltages applied to the SPAD. The timing jitter is better at high excess voltage. Using low threshold minimizes the jitter, especially at low excess voltage.

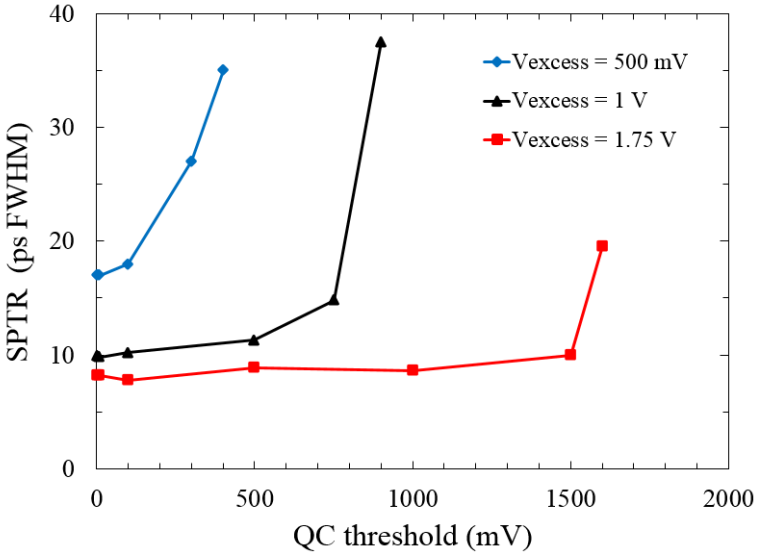

Figure 12. SPTR as a function of the QC threshold for different excess voltages.

Figure 13 shows the relationship between the SPTR and the Op-Amp power consumption. A minimum of 100 µW static power consumption is required to obtain sub-10 ps SPTR. Higher power consumption does not improve the SPTR further.

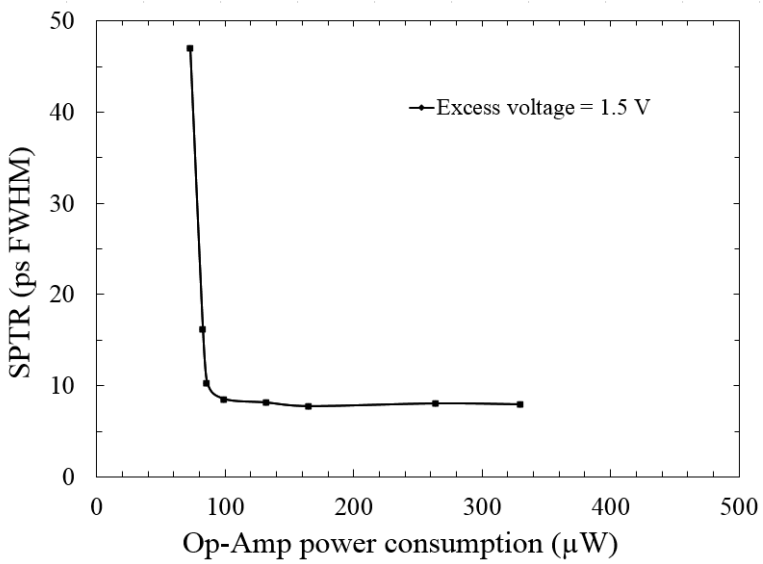

Figure 13. SPTR as a function of the QC Op-Amp power consumption.

4.4. SPAD Characteristics

The SPAD characteristics are summarized in Table 1. The SPAD breakdown voltage is 9.9 V. The single SPAD PDE is between 2% and 8% in the wavelength range of 400 nm to 700 nm with a peak at 470 nm. The SPAD architecture (shallow p^+ n-well junction) as well as the multiple intermetal dielectric layers over the SPAD may explain the low PDE. These characteristics lead to low light absorption into the thin high-field region of the SPAD.

Table 1. SPAD characteristics summary.

Characteristics	This Work	[46]	[47]	[48]	[49]	[41]	[50]
Technology	**65**	65	90	150	160	180	350
V_{BD}/V_{EX} (V)	**9.9/1.5**	9/0.4	14.9/2.4	19/5	26/3–9	11/0.8	25/6
SPAD diameter (µm)	**20**	8	6.4	10	10–80	14	20
DCR (cps/µm^2)	**2.8 k**	15.6 k	3.1	1	0.13–0.19	4 k	1.2
Afterpulsing (%)	**<10**	<1	<1	<13	<1.26	N/A	<1
@ Hold-off	(0.1 µs)	(5 µs)	(15 ns)	(50 ns)	(50 ns)		(40 ns)
Peak PDE (%)	**8**	5.5	44	32	71	N/A	48
SPTR (ps FWHM)	**7.8**	235	51	42	28	27	80

4.5. SPAD Excess Voltage Variation

Figure 14 shows the discrimination S-curve of the QC using a step signal as input. The slope is steep and the peak of the variation of the discrimination is about 15 mV. Figure 15 shows that the variation is about 3 mV FWHM at different amplitude level. This shows that the QC has a precision of 3 mV and that it can be used to evaluate the SPAD excess voltage variation of tens of mV.

The same measurements are performed using a SPAD as the input instead of the step signal (Figure 16). The discrimination variation increases from 3 mV to 30 mV. We infer this change to be from the SPAD excess voltage variation and is about 30 mV FWHM.

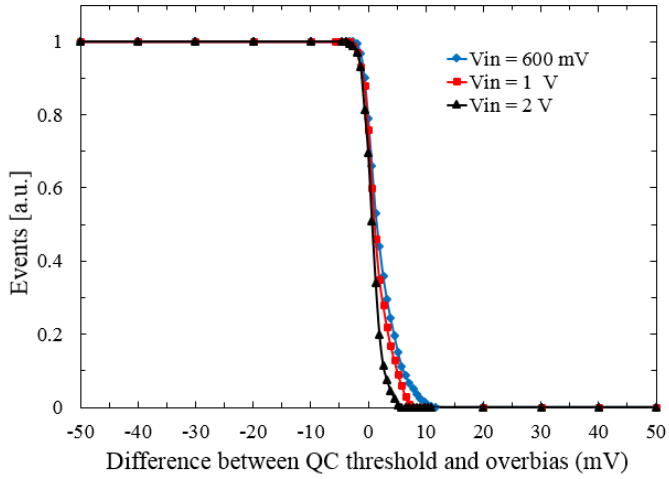

Figure 14. Operational amplifier S-curve of the discrimination.

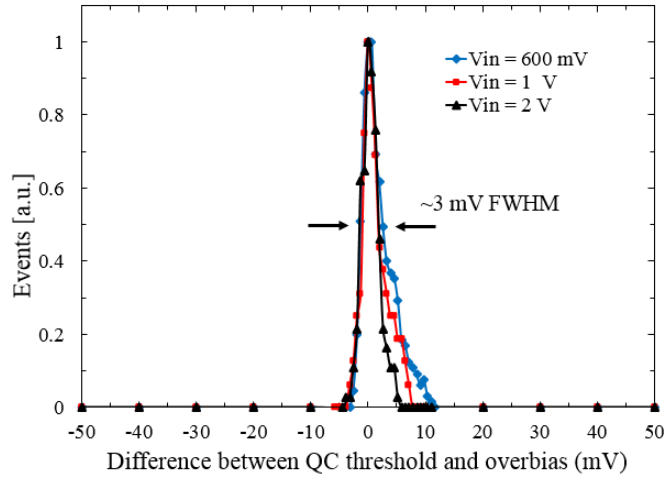

Figure 15. Derivative of the S-curve (Figure 14) of the discrimination showing a variation of about 3 mV FWHM of the electronics, without a SPAD.

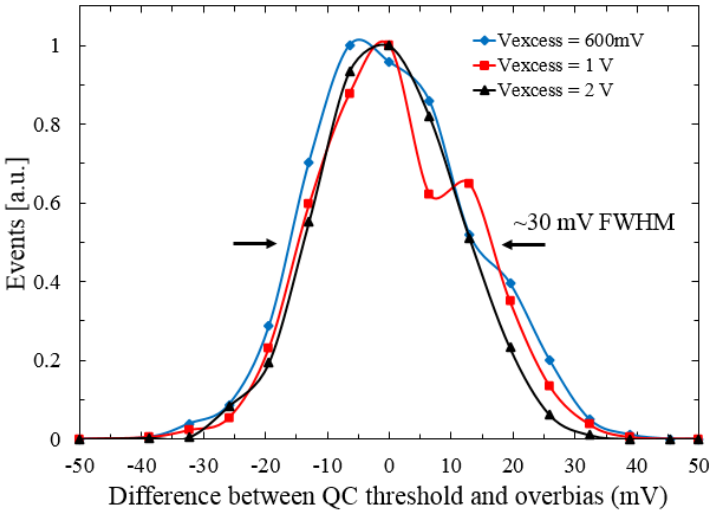

Figure 16. Derivative of the S-curve of the discrimination of the SPAD signal showing a SPAD excess voltage variation of about 30 mV FWHM. The lines are not a fit, they are drawn to guide the eye.

4.6. Timing Jitter Due to the SPAD Excess Voltage Variation

The 30 mV SPAD excess voltage variation from Figure 16 may be transposed into timing jitter thanks to the time propagation delay data from Figure 10. Figure 17 compares the SPAD excess voltage variation jitter contribution with the measured SPTR. At low excess voltage (<300 mV), the QC contribution (jitter from the time propagation delay) dominates the measured SPTR (>20 ps FWHM). From 300 mV to about 700 mV, the timing jitter of the QC associated with the variation of the input signal lowers from 20 ps to 7 ps FWHM. At higher excess voltage (>0.7 V), the time propagation delay variation is small, representing a 3 ps FWHM contribution to the single photon timing resolution.

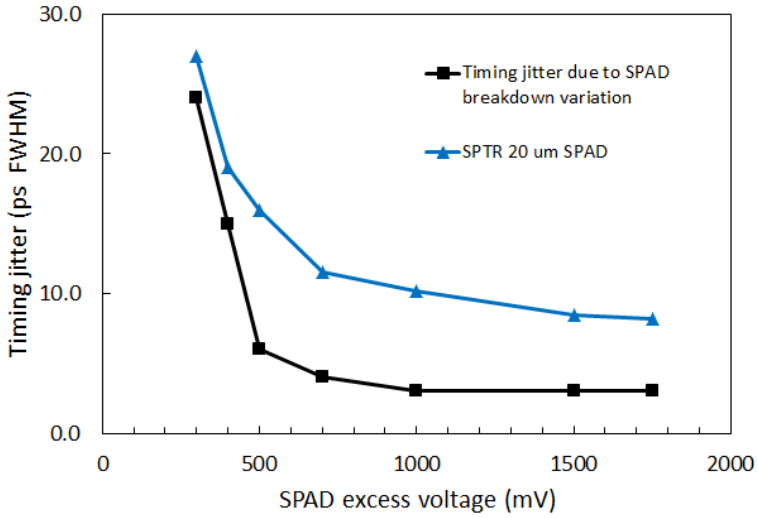

Figure 17. Timing jitter contribution of the SPAD excess voltage variation compared to the measured SPAD and QC SPTR.

This timing jitter study provides an important insight about the single SPAD SPTR: the SPAD excess voltage variation is not limiting the global SPTR if the time propagation delay of the QC is low (~3 ps/100 mV in this QC).

5. Discussion

The QC proposed in this paper is designed to be integrated in a 3D digital SiPM for which three major properties must be optimized: power consumption, size and timing performance.

The QC power consumption has two contributions, the static power consumption of the Op-Amp and the dynamic consumption of the QC. As presented in Figure 13, to obtain a SPTR below 10 ps, a static power consumption of 85 µW is required in the Op-Amp. For application requiring a limited number of pixels or a small detector area (<5 × 5 mm^2), the power consumption may not be an issue. However, for applications such as a PET scanner with large area of detectors, a 85 µW static power consumption per pixel in a 3D digital SiPM is still high. Since the projected SPAD size is 50 µm and the LabPET II rabbit scanner has about 50,000 1.1 × 1.1 mm^2 pixels, there will be 24.2 millions QC in the scanner [51]. The total power consumption of all the QC would be approximately 2.05 kW, 4 times higher than the estimated power consumption of 520 W of the current front-end electronics of the LabPET II rabbit scanner [52]. The static power consumption could be reduced or eliminated by choosing another discriminator architecture. However, this may come at the expense of the SPTR. Further optimization of the Op-Amp to reduce its static power consumption is mandatory for system integration.

Since the objective is to integrate the QC and a TDC within the 50 × 50 μm^2 pixel of the 3D digital SiPM, the QC size is of high importance. The proposed QC has a size of 30 × 18 μm^2 including a contact area for the TSV. With this architecture, the size could easily be reduced to 15 × 18 μm^2 while keeping the sub-10 ps SPTR capability if designed for a 2D device. The present version's size is larger

since it includes the TSV landing site (where no noise sensitive circuit may be placed) and some extra feature to find the best operating point (variable threshold, hold-off, etc.). Reducing the size for a 3D integrated detector would require architecture modifications of the discriminator and, as for the power consumption, may come at the expense of the SPTR. A size of 30 × 18 µm^2 represents less than 25 % of the total size of the 3D digital SiPM pixel, which seems acceptable.

The main objective of this detector is to obtain a SPTR below 10 ps FWHM. The timing jitter of the QC alone, i.e., without the SPAD, was optimized and is extremely low. Indeed, since its value is of the same order than the test setup contribution (∼4 ps FWHM), we believe that the timing jitter is dominated by either the output buffer or the measurement setup. The timing jitter of the QC alone is significantly lower than 4 ps FWHM. Knowing that the QC will drive an individual TDC in the 3D digital SiPM instead of the full test setup, its contribution to the SPTR should be lower than 4 ps FWHM. According to Table 1, the developed SPAD has an excellent SPTR (7.8 ps). Furthermore, the present SPAD design exhibits overall better results if compared to a previous SPAD design made in the same technology node [46]. In a 3D digital SiPM, a bigger capacitance is expected between the SPAD and the Op-Amp. With an adjustable threshold, the Op-Amp should provide a suitable solution to select the optimal point in the risetime of the signal to optimize the SPTR.

As for the SPAD developed, it suffers from a low PDE (8%) and from a high DCR (900 kcps) compared to other CMOS SPAD made in higher technology node [50]. These characteristics are not suitable for applications such as PET scanners, which require a high fill factor and high PDE to detect the low level of scintillation light. However, application such as rangefinding would benefit from a 2D detector made in CMOS 65 nm since correlated measurements are less affected by high DCR and lower PDE can be compensated with higher photon flux. Furthermore, on-chip post-processing can easily be added in a CMOS technology to improve the timing performance.

This work also aims to better understand the different contribution to the SPTR from the combination of the SPAD and the QC. The measured SPTR of the QC with an integrated SPAD is 7.8 ps FWHM (Figure 11). The jitter measurement with a step signal demonstrated that the QC jitter is extremely low, i.e., similar to test setup jitter of 4 ps FWHM (Figure 8). This timing jitter study provides an important insight about the single SPAD SPTR: the combination of the SPAD excess voltage variation and the time propagation delay variation must be low enough to be a negligible contribution to the SPAD SPTR. In the case of the QC developed, it does not limit the SPTR for a SPAD with an excess voltage variation of 30 mV FWHM or lower if sufficient excess voltage is applied (Figure 17). Consequently, the main contribution of the 7.8 ps must come from the SPAD itself (avalanche multiplication statistics) or from the QC input signal shape (e.g., parasitic capacitance) that affects the QC timing jitter. Considering that a proper design can be achieved on the SPAD layer, the 3D process connecting the SPAD to the QC is critical since the SPTR could be limited by the parasitic capacitance at the QC input node. Further studies with varying capacitance at the input of the QC could help determine the main contribution between the two aforementioned.

6. Conclusions

This paper presents a new QC integrated in TSMC CMOS 65 nm technology. The QC was designed with view to be integrated in a 3D digital SiPM and is optimized for fast timing, low area and low power consumption. The extremely low timing jitters measured for the QC alone (<4 ps) and for the QC with an integrated SPAD (7.8 ps) establish that fast timing electronics for single shot timing measurements in a 3D digital SiPM is achievable. To optimize the QC for timing, it is important to use a comparator that will not be affected by the amplitude variation at its input. Since the SPTR is not affected by the variation in this SPAD and QC, the Op-Amp proposed is well adapted to eliminate a contribution to the SPTR from a SPAD excess voltage variation of 30 mV or lower like in the SPAD presented in this paper. The QC's adjustable threshold feature allows timing resolution optimization as well as SPAD excess voltage characterization. The QC has a total size of 30 × 18 µm^2 including a contact for a TSV connection in the 3D digital SiPM architecture. The power consumption of the QC is 130 µW at a count

rate of 1 Mcps. The adjustable threshold, and hold-off and recharge times are essential since the SPAD and QC interconnection in the 3D digital SiPM is under development. The next step for this project is to study the mm-scale uniformity of the quenching circuit characteristics in an array. This includes the timing jitter and the time delay propagation variation to ensure that the QC developed will not affect the timing precision of a SPAD array, either from timing jitter or timing skew.

Author Contributions: F.N. is the main contributor and developed the quenching circuit and performed the device characterization and analysis; S.P. developed the SPAD and helped performed the SPAD characterization; N.R. and M.-O.M. developed the hardware and firmware for the characterization; S.A.C. and R.F. co-directed the work and provided feedback on the design and analysis; J.-F.P. directed the work, provided the funding and provided feedback on the design, characterization and analysis.

Acknowledgments: This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC), by the Fonds de recherche du Québec–Nature et technologies (FRQNT), by the Regroupement Stratégique en Microsystèmes du Québec (ReSMiQ), and by CMC Microsystems.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Frach, T.; Prescher, G.; Degenhardt, C.; de Gruyter, R.; Schmitz, A.; Ballizany, R. The digital silicon photomultiplier—Principle of operation and intrinsic detector performance. In Proceedings of the Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Orlando, FL, USA, 24 October–1 November 2009; pp. 1959–1965. [CrossRef]
2. Schaart, D.R.; Charbon, E.; Frach, T.; Schulz, V. Advances in digital SiPMs and their application in biomedical imaging. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2016**, *809*, 31–52. [CrossRef]
3. Bruschini, C.; Charbon, E.; Veerappan, C.; Braga, L.; Massari, N.; Perenzoni, M.; Gasparini, L.; Stoppa, D.; Walker, R.; Erdogan, A.; et al. SPADnet: Embedded coincidence in a smart sensor network for PET applications. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2014**, *734*, 122–126. [CrossRef]
4. Powolny, F.; Auffray, E.; Brunner, S.E.; Garutti, E.; Goettlich, M.; Hillemanns, H.; Jarron, P.; Lecoq, P.; Meyer, T.; Schultz-Coulon, H.C.; et al. Time-based readout of a silicon photomultiplier (SiPM) for time of flight positron emission tomography (TOF-PET). *IEEE Trans. Nucl. Sci.* **2011**, *58*, 597–604. [CrossRef]
5. Ronzhin, A.; Albrow, M.; Los, S.; Martens, M.; Murat, P.; Ramberg, E.; Kim, H.; Chen, C.T.; Kao, C.M.; Niessen, K.; et al. A SiPM-based TOF-PET detector with high speed digital DRS4 readout. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2013**, *703*, 109–113. [CrossRef]
6. Gersbach, M.; Maruyama, Y.; Trimananda, R.; Fishburn, M.W.; Stoppa, D.; Richardson, J.A.; Walker, R.; Henderson, R.; Charbon, E. A time-resolved, low-noise single-photon image sensor fabricated in deep-submicron CMOS technology. *IEEE J. Solid-State Circuits* **2012**, *47*, 1394–1407. [CrossRef]
7. Schwartz, D.E.; Charbon, E.; Shepard, K.L. A single-photon avalanche diode array for fluorescence lifetime imaging microscopy. *IEEE J. Solid-State Circuits* **2008**, *43*, 2546–2557. [CrossRef] [PubMed]
8. Maruyama, Y.; Blacksberg, J.; Charbon, E. A 1024 × 8, 700-ps time-gated spad line sensor for planetary surface exploration with laser raman spectroscopy and libs. *IEEE J. Solid-State Circuits* **2014**, *49*, 179–189. [CrossRef]
9. Nissinen, I.; Nissinen, J.; Keranen, P.; Lansman, A.K.; Holma, J.; Kostamovaara, J. A 2 × (4) × 128 Multitime-Gated SPAD Line Detector for Pulsed Raman Spectroscopy. *IEEE Sens. J.* **2015**, *15*, 1358–1365. [CrossRef]
10. Fisher, E.; Underwood, I.; Henderson, R. A reconfigurable single-photon-counting integrating receiver for optical communications. *IEEE J. Solid-State Circuits* **2013**, *48*, 1638–1650. [CrossRef]
11. Chitnis, D.; Collins, S. A SPAD-based photon detecting system for optical communications. *J. Lightwave Technol.* **2014**, *32*, 2028–2034. [CrossRef]
12. Niclass, C.; Soga, M.; Kato, S. A 0.18 µm CMOS single-photon sensor for coaxial laser rangefinders. In Proceedings of the 2010 IEEE Asian Solid-State Circuits Conference, Beijing, China, 8–10 November 2010; pp. 105–108. [CrossRef]

13. Bronzi, D.; Villa, F.; Tisa, S.; Tosi, A.; Zappa, F.; Durini, D.; Weyers, S.; Brockherde, W. 100,000 Frames/s 64 × 32 Single-Photon Detector Array for 2-D Imaging and 3-D Ranging. *IEEE J. Sel. Top. Quantum Electron.* **2014**, *20*, 354–363. [CrossRef]
14. Stoppa, D.; Pancheri, L.; Scandiuzzo, M.; Gonzo, L.; Betta, G.F.D.; Simoni, A. A CMOS 3-D Imager Based on Single Photon Avalanche Diode. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2007**, *54*, 4–12. [CrossRef]
15. Moses, W.W. Time of flight in PET revisited. *IEEE Trans. Nucl. Sci.* **2003**, *50*, 1325–1330. [CrossRef]
16. Gundacker, S.; Auffray, E.; Pauwels, K.; Lecoq, P. Measurement of intrinsic rise times for various L(Y)SO and LuAG scintillators with a general study of prompt photons to achieve 10 ps in TOF-PET. *Phys. Med. Biol.* **2016**, *61*, 2802. [CrossRef] [PubMed]
17. Lecoq, P.; Korzhik, M.; Vasiliev, A. Can Transient Phenomena Help Improving Time Resolution in Scintillators. *IEEE Trans. Nucl. Sci.* **2014**, *61*, 229–234. [CrossRef]
18. Omelkov, S.; Nagirnyi, V.; Vasilev, A.; Kirm, M. New features of hot intraband luminescence for fast timing. *J. Lumin.* **2016**, *176*, 309–317. [CrossRef]
19. Grim, J.Q.; Christodoulou, S.; Di Stasio, F.; Krahne, R.; Cingolani, R.; Manna, L.; Moreels, I. Continuous-wave biexciton lasing at room temperature using solution-processed quantum wells. *Nat. Nanotechnol.* **2014**, *9*, 891–895. [CrossRef] [PubMed]
20. Lecoq, P. Pushing the Limits in Time-of-Flight PET Imaging. *IEEE Trans. Radiat. Plasma Med. Sci.* **2017**, *1*, 473–485. [CrossRef]
21. Ahmed, G.; Buhler, P.; Cargnelli, M.; Hohler, R.; Marton, J.; Orth, H.; Suzuki, K. Application of Geiger-mode photosensors in Cherenkov detectors. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2011**, *639*, 107–110. [CrossRef]
22. Dolenec, R.; Korpar, S.; Krizan, P.; Pestonik, R.; Verdel, N. The Performance of Silicon Silicon Photomultipliers Photomultipliers in in Cherenkov. *IEEE Trans. Nucl. Sci.* **2016**, *63*, 2478–2481. [CrossRef]
23. Frach, T. Optimization of the digital Silicon Photomultiplier for Cherenkov light detection. *J. Instrum.* **2012**, *1*, C01112. [CrossRef]
24. Acerbi, F.; Ferri, A.; Gola, A.; Cazzanelli, M.; Pavesi, L.; Zorzi, N.; Piemonte, C. Characterization of Single-Photon Time Resolution: From Single SPAD to Silicon Photomultiplier. *IEEE Trans. Nucl. Sci.* **2014**, *61*, 2678–2686. [CrossRef]
25. Nemallapudi, M.; Gundacker, S.; Lecoq, P.; Auffray, E. Single photon time resolution of state of the art SiPMs. *J. Instrum.* **2016**, *11*, P10016. [CrossRef]
26. Acerbi, F.; Ferri, A.; Gola, A.; Zorzi, N.; Piemonte, C. Analysis of single-photon time resolution of FBK silicon photomultipliers. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2015**, *787*, 34–37. [CrossRef]
27. Mandai, S.; Charbon, E. Optimization of the digital Silicon Photomultiplier for Cherenkov light detection. *J. Instrum.* **2013**, *8*, P09016. [CrossRef]
28. Liu, Z.; Gundacker, S.; Pizzichemi, M.; Ghezzi, A.; Auffray, E.; Lecoq, P.; Paganoni, M. In-depth study of single photon time resolution for the Philips digital silicon photomultiplier. *J. Instrum.* **2016**, *11*, P06006. [CrossRef]
29. Puill, V.; Bazin, C.; Breton, D.; Burmistrov, L.; Chaumat, V.; Dinu, N.; Maalmi, J.; Vagnucci, J.; Stocchi, A. Single photoelectron timing resolution of SiPM as a function of the bias voltage, the wavelength and the temperature. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2012**, *695*, 354–358. [CrossRef]
30. Bérubé, B.L.; Rhéaume, V.P.; Therrien, A.C.; Parent, S.; Maurais, L.; Boisvert, A.; Carini, G.; Charlebois, S.A.; Fontaine, R.; Pratte, J.F. Development of a single photon avalanche diode (SPAD) array in high voltage CMOS 0.8 µm dedicated to a 3D integrated circuit (3DIC). In Proceedings of the 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC), Anaheim, CA, USA, 27 October–3 November 2012; pp. 1835–1839. [CrossRef]
31. Nolet, F.; Rhéaume, V.P.; Parent, S.; Charlebois, S.A.; Fontaine, R.; Pratte, J.F. A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS With Low Output Capacitance. *IEEE Trans. Nucl. Sci.* **2016**, *63*, 2293–2299. [CrossRef]
32. Tétrault, M.A.; Lamy, E.; Boisvert, A.; Thibaudeau, C.; Kanoun, M.; Dubois, F.; Fontaine, R.; Pratte, J.F. Real-Time Discrete SPAD Array Readout Architecture for Time of Flight PET. *IEEE Trans. Nucl. Sci.* **2015**, *62*, 1077–1082. [CrossRef]

33. Roy, N.; Nolet, F.; Dubois, F.; Mercier, M.O.; Fontaine, R.; Pratte, J.F. Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM. *IEEE Trans. Radiat. Plasma Med. Sci.* **2017**, *1*, 486–494. [CrossRef]
34. Nolet, F.; Dubois, F.; Roy, N.; Parent, S.; Lemaire, W.; Massie-Godon, A.; Charlebois, S.A.; Fontaine, R.; Pratte, J.F. Digital SiPM channel integrated in CMOS 65 nm with 17.5 ps FWHM single photon timing resolution. *Nucl. Instrum. Methods Phys. Res. Sec. A Accel. Spectrom. Detect. Assoc. Equip.* **2017**. [CrossRef]
35. Lacaita, A.; Cova, S.; Samori, C.; Ghioni, M. Performance optimization of active quenching circuits for picosecond timing with single photon avalanche diodes. *Rev. Sci. Instrum.* **1995**, *66*, 4289–4295. [CrossRef]
36. Guhilot, H.; Kamat, R.K. All nMOS 10-T AQRC for Monolithic Chlorophyll Fluorescence SPAD Sensor. *IEEE Sens. J.* **2011**, *11*, 1975–1978. [CrossRef]
37. Zappa, F.; Ghioni, M.; Cova, S.; Samori, C.; Giudice, A.C. An integrated active-quenching circuit for single-photon avalanche diodes. *IEEE Trans. Instrum. Meas.* **2000**, *49*, 1167–1175. [CrossRef]
38. Zappa, F.; Lotito, A.; Giudice, A.C.; Cova, S.; Ghioni, M. Monolithic active-quenching and active-reset circuit for single-photon avalanche detectors. *IEEE J. Solid-State Circuits* **2003**, *38*, 1298–1301. [CrossRef]
39. Gallivanoni, A.; Rech, I.; Resnati, D.; Ghioni, M.; Cova, S. Monolithic active quenching and picosecond timing circuit suitable for large-area single-photon avalanche diodes. *Opt. Express* **2006**, *14*, 5021–5030. [CrossRef] [PubMed]
40. Stipčević, M. Active quenching circuit for single-photon detection with Geiger mode avalanche photodiodes. *Appl. Opt.* **2009**, *48*, 1705–1714. [CrossRef] [PubMed]
41. Hsu, M.J.; Finkelstein, H.; Esener, S.C. A CMOS STI-Bound Single-Photon Avalanche Diode with 27-ps Timing Resolution and a Reduced Diffusion Tail. *IEEE Electron Device Lett.* **2009**, *30*, 641–643. [CrossRef]
42. Gulinatti, A.; Maccagnani, P.; Rech, I.; Ghioni, M.; Cova, S. 35 ps time resolution at room temperature with large area single photon avalanche diodes. *Electron. Lett.* **2005**, *41*, 272–274. [CrossRef]
43. Rech, I.; Labanca, I.; Armellini, G.; Gulinatti, A.; Ghioni, M.; Cova, S. Operation of silicon single photon avalanche diodes at cryogenic temperature. *Rev. Sci. Instrum.* **2007**, *78*, 063105. [CrossRef] [PubMed]
44. Pratte, J.F.; Junnarkar, S.; Deptuch, G.; Fried, J.; O'Connor, P.; Radeka, V.; Vaska, P.; Woody, C.; Schlyer, D.; Stoll, S.; et al. The RatCAP Front-End ASIC. *IEEE Trans. Nucl. Sci.* **2008**, *55*, 2727–2735. [CrossRef]
45. Bérubé, B.L.; Rhéaume, V.P.; Parent, S.; Maurais, L.; Therrien, A.; Charette, P.; Charlebois, S.; Fontaine, R.; Pratte, J.F. Implementation Study of Single Photon Avalanche Diodes (SPAD) in 0.8 µm HV CMOS Technology. *IEEE Trans. Nucl. Sci.* **2015**, *62*, 710–718. [CrossRef]
46. Charbon, E.; Hyyung-June, Y.; Maruyama, Y. A Geiger mode APD fabricated in standard 65 nm CMOS technology. In Proceedings of the 2013 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 9–11 December 2013; pp. 1–4. [CrossRef]
47. Webster, E.A.G.; Richardson, J.A.; Grant, L.A.; Renshaw, D.; Henderson, R.K. A Single-Photon Avalanche Diode in 90-nm CMOS Imaging Technology with 44% Photon Detection Efficiency at 690 nm. *IEEE Electron Device Lett.* **2012**, *33*, 694–696. [CrossRef]
48. Xu, H.; Pancheri, L.; Betta, G.F.D.; Stoppa, D. Design and characterization of a p+/n-well SPAD array in 150nm CMOS process. *Opt. Express* **2017**, *25*, 12765–12778. [CrossRef] [PubMed]
49. Sanzaro, M.; Gattari, P.; Villa, F.; Tosi, A.; Croce, G.; Zappa, F. Single-Photon Avalanche Diodes in a 0.16 µm BCD Technology with Sharp Timing Response and Red-Enhanced Sensitivity. *IEEE J. Sel. Top. Quantum Electron.* **2018**, *24*, 1–9. [CrossRef]
50. Villa, F.; Bronzi, D.; Zou, Y.; Scarcella, C.; Boso, G.; Tisa, S.; Tosi, A.; Zappa, F.; Durini, D.; Weyers, S.; et al. CMOS SPADs with up to 500 µm and 55% detection efficiency at 420 nm. *J. Mod. Opt.* **2014**, *61*, 102–115. [CrossRef]
51. Bergeron, M.; Thibaudeau, C.; Cadorette, J.; Tétrault, M.A.; Pepin, C.M.; Clerk-Lamalice, J.; Loignon-Houle, F.; Davies, M.; Dautet, H.; Deschamps, P.; et al. LabPET II, an APD-based Detector Module with PET and Counting CT Imaging Capabilities. *IEEE Trans. Nucl. Sci.* **2015**, *62*, 756–765. [CrossRef]
52. Oukaira, A.; Fontaine, R.; Lecomte, R.; Lakhssassi, A. Thermal cooling system development for LabPET II scanners by forced convection flow. In Proceedings of the 2017 15th IEEE International New Circuits and Systems Conference (NEWCAS), Strasbourg, France, 25–28 June 2017; pp. 289–292. [CrossRef]