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Efficiency Improvement of a Cascaded Buck and Boost Converter for Fuel Cell Hybrid Vehicles with Overlapping Input and Output Voltages

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Abstract: Fuel cell hybrid vehicles represent an alternative to battery electric vehicles and will gain importance in the future as they do not need large battery capacities and thus require less critical raw materials. Depending on the electric architecture, the voltage of the fuel cell stack and traction battery may overlap. Accordingly, it is necessary to use a bidirectional DC–DC converter that connects the battery to the DC bus, which supports overlapping input and output voltages. Furthermore, these converters should be non-isolating in terms of compact design. Concerning complexity and controllability, the bidirectional cascaded buck and boost converter is preferable and is the subject of this study. Published literature presents the bidirectional cascaded buck and boost converter with high losses for overlapping input and output voltages, introducing two methods for this operation mode. The method selected for this study, namely buck + boost, uses two switches, whereby one switch has a fixed duty cycle. However, there is no appropriate investigation to determine the impact of this fixed duty cycle on converter efficiency to date. Furthermore, efficiency improvement is possible by switching frequency modulation, but current literature does not address this modulation method for overlapping input and output voltages. Therefore, this paper investigates a non-isolated hard-switched bidirectional cascaded buck and boost converter for fuel cell hybrid vehicles operating with up to 19.8 kW. The study focuses on determining the optimum fixed duty cycle and efficiency optimisation through a novel critical conduction mode with adapted switching frequency by utilising the load-dependent inductance of the inductor with powder cores. Measurements with an experimental setup validate the proposed modulation method with Si-IGBT half-bridge modules. The results demonstrate that a loss reduction of 39% is possible with switching frequency modulation and the optimum duty cycle compared to fixed switching frequency. As a result, the converter achieves high efficiencies of up to 99% and low device junction temperatures.

Keywords: buck + boost; DC–DC converter; fuel cell hybrid vehicles; switching frequency modulation

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1. Introduction

The electrification of the powertrain is a promising solution for a sustainable and environmentally friendly transport system [1]. Furthermore, electromobility represents an essential contribution to climate protection and renewable energies in the transport sector [2]. For this reason, automobile manufacturers are increasingly offering battery electric vehicles (BEVs). In the electric architecture of BEVs, the battery is the only energy source for the electric drive; its operating voltage is typically below the DC bus to which the traction inverter is connected. Thus, a bidirectional buck–boost converter connects the battery to the DC bus. Furthermore, fuel-cell-based electromobility will also contribute to an environmentally friendly transport system. Studies indicate that 17% of the annually sold vehicles will be fuel-cell-based starting in 2050 [3]—for example, the fuel cell hybrid vehicle (FCHV). FCHVs use a battery as a second energy source in addition to the fuel cell,

providing peak power for dynamic load reduction on the fuel cell system [4,5]. This battery support is essential during acceleration and cold starts. Figure 1 shows the polarization curve of a proton-exchange membrane fuel cell (PEMFC) with its losses typically used in automotive applications. The cell voltage is load-dependent due to the reaction rate loss, resistance loss, and gas transport loss.

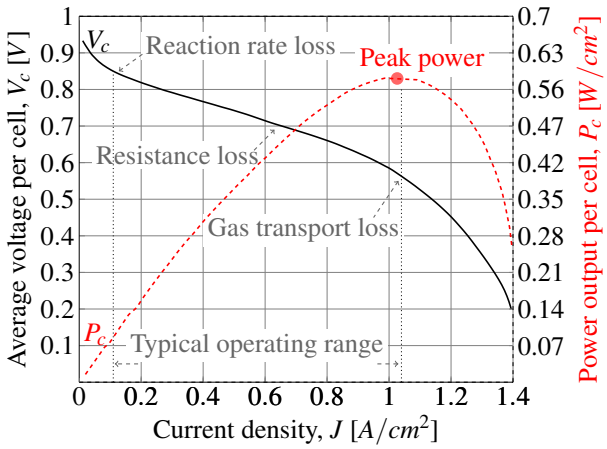

Figure 1. Output voltage of a PEMFC as a function of the current density, data according to [6].

Two electric architectures in FCHVs are of interest for future applications. Figure 2a illustrates the system in which a boost converter connects the fuel cell to the DC bus [5,7]. The motor interfaces the DC bus via a bidirectional DC–AC converter. In addition, this architecture uses a bidirectional buck–boost converter in front of the battery. Figure 2b illustrates an alternative solution, where the output terminals of the fuel cell are connected directly to the DC bus [5,7]. However, depending on the state of charge of the battery and the load-dependent fuel cell voltage (see the typical operating range in Figure 1), both voltage levels can overlap. For this reason, a bidirectional DC–DC converter is necessary, interfacing both voltage characteristics to enable good cold-start behaviour, flexible power control, regenerative braking, and to avoid dynamic current stress of the fuel cell stack by providing additional traction power during acceleration [8–10]. For these reasons, optimising the bidirectional DC–DC converters in front of the battery is essential for vehicle performance. Basically, three topologies are suitable, the bidirectional CúK, SEPIC/ZETA, and cascaded buck and boost converter. Nevertheless, a previous study [11] demonstrates that in terms of electric stress on the power semiconductors and converter volume, the cascaded buck and boost converter is an appropriate topology for FCHVs to interface the battery to the DC bus. For example, the study in [11] demonstrates that the cascaded buck and boost converter topology reduces the required inductance to a fifth and the capacitance value by ∼5% compared to the CúK and SEPIC/ZETA converter. As the inductance relates to the energy-handling capability and, therefore, the volume of the inductor, it indicates that the cascaded buck and boost converter decreases the converter volume for the application of interest accordingly. As the inductor of a DC–DC converter is a major contributor to the overall volume, the bidirectional cascaded buck and boost converter is thus a suitable topology for mobile applications such the FCHVs.

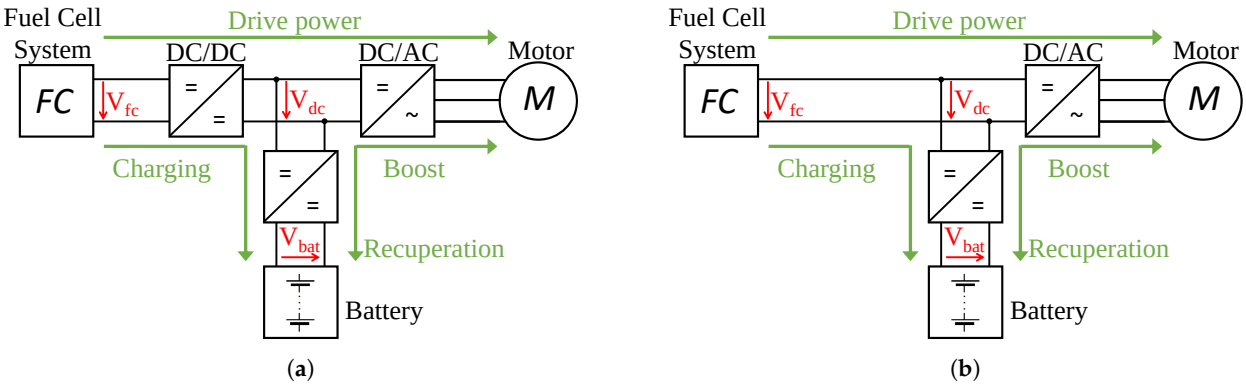

Figure 2. Electric architectures for FCHVs: (**a**) electric architecture with a boost converter for the fuel cell system; (**b**) electric architecture without a boost converter for the fuel cell system.

The published literature introduces two modulation modes for overlapping input and output voltages with the bidirectional cascaded buck and boost converter: the buck–boost and buck + boost modes. The subsequent section will quantify these modulation methods in detail. However, to summarise, the buck–boost mode uses four switches; in contrast, the buck + boost mode only uses two. Furthermore, the buck + boost mode operates with two duty cycles. One of these duty cycles needs to be constant. However, the literature does not determine the optimum for this constant duty cycle in terms of converter losses. Moreover, the literature does not sufficiently discuss the optimisation of the operation mode with overlapping input and output voltages. Instead, authors frequently introduce soft-switching concepts for efficiency improvement [12]. However, the efficiency improvement does not justify the increase in converter volume due to the additional snubber circuits.

Further, the literature often refers to lower power applications (less than 10 kW) regarding the operation mode for overlapping input and output voltages, where authors often recommend the buck–boost mode [13]. However, disregarding converter volume, which depends on the design process, application and other requirements, it is evident that the buck–boost mode would considerably reduce efficiency over the entire power range. Moreover, in the buck–boost mode, the inductor current is composed of the sum of converter input and output currents that would significantly increase magnetic core volume, especially in the mid-kW range (10 kW–50 kW).

For example, the low efficiency of the buck–boost mode is also demonstrated in [12]. The study in [12] introduces a buck–boost + LLC cascaded 1.12 kW converter using the dual-frequency PEM method. Furthermore, the authors investigate zero voltage switching (ZVS) and zero current switching (ZCS). Nonetheless, they achieve efficiencies of around 92% for the buck–boost mode. The study results in [14] confirm this statement. The 100 W bidirectional cascaded buck and boost converter in [14] does not exceed an efficiency of 95% at any operation point. Furthermore, the authors demonstrate efficiency improvement with GaN power semiconductors compared to Si power semiconductors using soft switching. However, the converter achieves a low power density of 0.5 kW/L, using a switching frequency of 10 MHz. In addition, the authors do not investigate the operation for overlapping input and output voltages. In addition, Ref. [13] mentions the buck–boost mode's disadvantages: high current ripples on the inductor and poor converter efficiency. The paper presents a hybrid buck–boost feedforward control method for a maximum power of 2.25 kW. Another example of low converter efficiency is [15]. The converter only achieves an efficiency of 93%. The authors focused on buck- and boost mode transition for a 120 W bidirectional cascaded buck and boost converter.

This article will prove that using hard switching devices in buck + boost mode and the optimum fixed duty cycle and a simple modulation method can decrease power losses by up to 39% for overlapping input and output voltages. Unlike in [12] or [15], the results will prove soft-switching is unnecessary for optimisation. Furthermore, in contrast to [14],

this article will prove that optimising converter efficiency with Si-IGBTs half-bridge modules is possible. Finally, the suggested approach eliminates the drawback of [13] of high computational effort and high current ripples due to its simplicity.

A method for efficiency optimisation is switching frequency modulation, for example, by increasing the switching frequency to operate in critical conduction mode (CrCM). The CrCM is the boundary limit between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Another approach is to adjust the switching frequency until reaching the efficiency maximum depending on the operating point. Generally, a DC–DC converter has two main power loss contributors: the power semiconductors and the inductor. By increasing the switching frequency, the switching losses of the power semiconductor will rise. However, losses of the inductor will decrease as higher switching frequencies reduce the current ripple and the AC flux density. Therefore, a critical requirement for switching frequency modulation is the percentage power distribution of the DC–DC converter. Authors in published literature introduce CrCM approaches for DC–DC converters in the power range below 10 kW. However, for such low power ranges, the power losses of the power semiconductors approximately match the power losses of the DC inductor.

An example for this modulation method would be the study according to [16] in which the authors operate the buck–boost mode with a fixed switching (FSF) frequency (20 kHz) and with switching frequency modulation (20 kHz–100 kHz) in CrCM. The results demonstrate poor efficiencies below 95% for $P \leq P_{max} \cdot 0.2$ (light-load operation). The reason for this efficiency is that the converter operates with high switching frequencies in light-load to avoid DCM. Another study presents an algorithm for the control unit to adjust the switching frequency according to a calculated loss minimum depending on the output power [17]. However, this approach has a high computational effort as the algorithm calculates the switching frequency according to power loss models with eight equations and several dynamic parameters. Moreover, the study does not investigate the operation mode with overlapping input and output voltages. The authors of the paper [18] also investigate switching frequency modulation to enhance efficiency. The proposed approach consists of an algorithm that adjusts the switching frequency according to power loss measurements. However, such power measurements result in computational effort. In addition, the converter does not avoid DCM and operates with a maximum output power of 3.6 W.

References [19,20] analyse converters for power factor correction in CrCM. The results of these studies demonstrate a significant reduction in turn-on switching losses of the power semiconductors; however, the total switching losses increases. As shown in [19,20], the control unit requires high switching frequencies to avoid DCM. Indeed, the converter topologies for power factor correction are irrelevant for the application of this article. Nevertheless, the results prove the potential due to the turn-on of the transistors at the boundary limit of 0 A. A similar approach is shown in [21] where the authors propose a CrCM control method for a boost converter. With additional hardware, the approach enables current-mirroring sensing with GaN transistors. The setup triggers the turn-on of the transistors as soon as reaching the boundary limit. Operating at the boundary limit, hence in CrCM, also reduces reverse recovery losses of diodes, which is confirmed by [22]. In [22], the authors propose a control method that increases switching frequency for CrCM, similar to [19,20]. Consequently, the results of [22] show that increasing the switching frequency in light-load for CrCM causes electromagnetic interference (EMI). Therefore, the authors in [22] propose an approach to reduce input current harmonic values for a 120 W prototype converter. The reason for EMI in CrCM in [22] is the high switching frequency to avoid DCM. In [22], the switching frequency in light-load is higher than in full-load by a factor of five. As a result, the approach achieves low efficiencies. A study comparable to this article is [16], where the authors analyse different control methods for the bidirectional cascaded buck and boost converter for hybrid electric vehicles and up

to 30 kW in a simulation environment. However, by operating with CrCM, the converter in [16] achieves a maximum converter efficiency of approximately 97%.

This study aims to improve the efficiency of the bidirectional cascaded buck and boost converter for operation with overlapping input and output voltages using the buck + boost mode. For this reason, this paper investigates the resulting problem of high current ripples and the impact of the fixed duty cycle on converter losses. This article introduces a novel load-dependent switching frequency modulation for efficiency optimisation, namely the critical conduction mode with adapted switching frequency (CrCMASF). The investigation exemplifies that the introduced modulation method ensures CCM using powder cores and the soft saturation characteristic. The findings are validated by measurements on an experimental setup and reveal that the proposed duty cycle and modulation method enable converter efficiencies of up to 99%. Furthermore, measurements demonstrate that the introduced approach decreases the junction temperature of the power semiconductors significantly. The results of this article will prove that the suggested approach will decrease computational effort considerably compared to [17] or [18]. The novel method will only use one equation with one dynamic parameter, which is the current-dependent inductance of the inductor. Furthermore, no additional hardware is necessary compared to [21]. In addition, in contrast to [22], the proposed method will decrease switching frequency in light-load. Therefore, this paper will demonstrate that by CrCMASF, EMI will not deteriorate. Finally, compared to [16,23], the proposed modulation method enables high efficiencies for the entire power range. Further discoveries on this literature review will be presented on Section 6 subject to the findings of this research.

2. PWM Control Methods

Figure 3 depicts the non-isolated hard-switched bidirectional cascaded buck and boost converter (hereinafter referred to as converter). This converter is the anti-parallel combination of a buck and boost converter (half-bridge) with a connected second-order low-pass filter. The half-bridge configuration enables the current to flow in both directions with positive input and output voltages using anti-parallel diodes. According to the circuit in Figure 3, the converter operates in buck mode by controlling S_1 or S_3 and in boost mode by controlling S_2 or S_4. The diodes D_1, D_2, D_3, and D_4 act as freewheeling diodes accordingly. The converter allows the output voltage to be higher, lower, or equal to the input voltage.

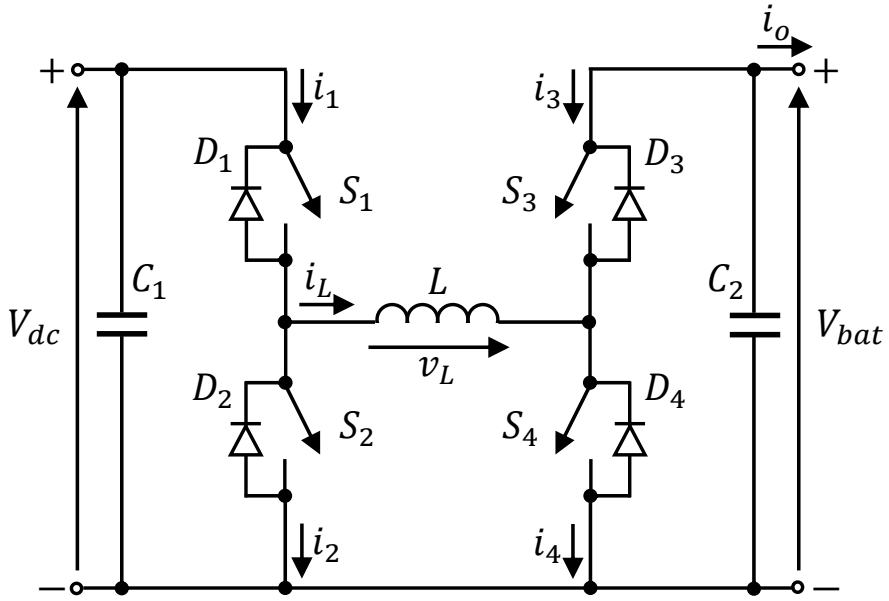

Figure 3. Non-isolated hard-switched bidirectional cascaded buck and boost converter.

Table 1 summarises the control of the transistors to operate in the respective mode. The converter can operate in buck, boost, buck–boost, or buck + boost mode; power flow from the DC bus to the battery or vice versa is possible for all operation modes. For convenience, this study assumes a power flow from the DC bus to the battery for further discussion. The following section analyses the operation mode with overlapping input and output voltages ($V_{dc} \approx V_{bat}$). The literature introduces two options for power transfer. Figure 4 illustrates the current i_L through inductance L for switches S_1 to S_4 for the first method. In this method, called buck–boost, switches S_1 and S_4 are switched simultaneously with a duty cycle $\gamma_{1,4}$, while switches S_2 and S_3 are switched simultaneously with a duty cycle $\gamma_{2,3}$. Figure 4 indicates that this method ensures that the average value of the inductor current i_L is composed of the sum of the converter currents i_1, i_4 and i_2, i_3, which represent the input and output currents of the converter [23]. This property is a disadvantage as the cores of the inductor with the inductance L would need a high DC bias compatibility, especially in the high power range and for applications such as FCHVs where high currents are possible. As a result, the volume would increase considerably [5].

Table 1. Operation modes for the converter, with controlled (c), off, and on for the switches.

Voltage Ratio	Power Flow	Mode	S_1	S_2	S_3	S_4
$V_{dc} > V_{bat}$	DC → Bat	buck	c	off	off	off
$V_{dc} \approx V_{bat}$	DC → Bat	buck + boost	c	off	off	c
$V_{dc} \approx V_{bat}$	DC → Bat	buck–boost	c	c	c	c
$V_{dc} < V_{bat}$	DC → Bat	boost	on	off	off	c
$V_{dc} < V_{bat}$	DC ←Bat	buck	off	off	c	off
$V_{dc} \approx V_{bat}$	DC ←Bat	buck + boost	off	c	c	off
$V_{dc} \approx V_{bat}$	DC ←Bat	buck–boost	c	c	c	c
$V_{dc} > V_{bat}$	DC ←Bat	boost	off	c	on	off

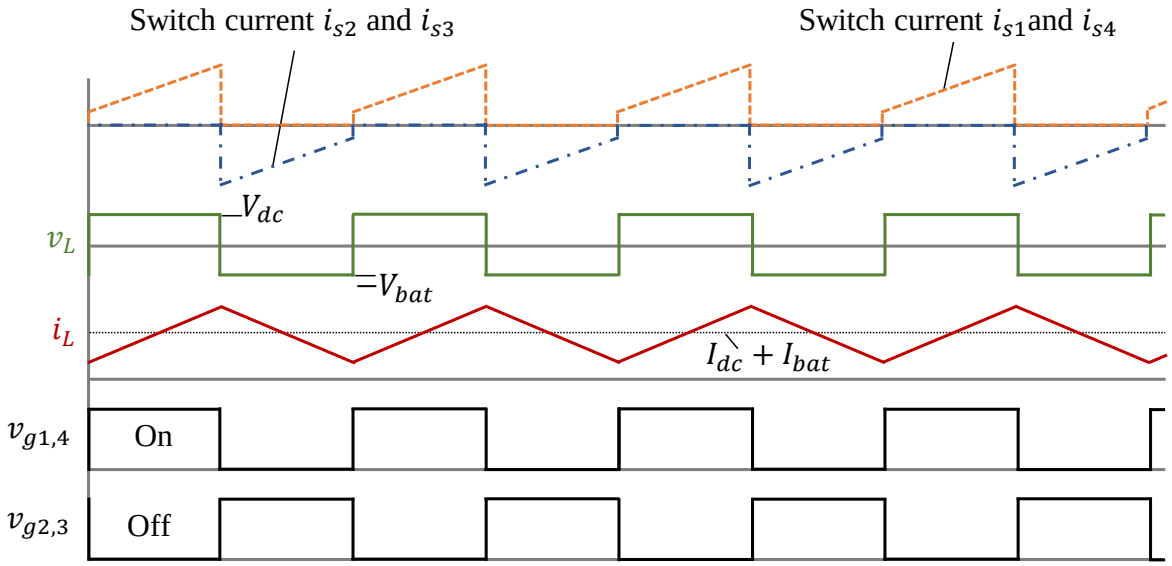

Figure 4. Characteristic of the inductor current and voltage in buck–boost mode.

Moreover, to ensure that the inductor voltage v_L on its average is zero, the duty cycles $\gamma_{1,4}$ and $\gamma_{2,3}$ must be 0.5 for equal voltages on the input and output. Furthermore, current peaks may occur. Admittedly, state-of-the-art controllers prevent the inductor current from increasing to unreasonable values. However, no controller can hold the current dynamically, which can lead to high current peaks. For example, a previous study investigated methods adapted for the control of the converter [7], where the difficulty is evident in preventing unacceptably control deviation of the inductor current i_L during the transitions between buck mode and boost mode for overlapping input and output voltages.

Moreover, for the buck–boost mode, the approximately matching duty cycles cause high current ripples Δi_L, which increase the current stress on the switches, as shown in Figure 4. The current stress results in considerable losses in the inductor and all switches.

The buck + boost mode in Figure 5 eliminates these drawbacks as it only uses two switches, switch S_1 and switch S_4. One half of the converter in Figure 3 operates as a buck converter, the other half as a boost converter. Thus, for switch S_1, a fixed duty cycle γ_1 is specified for buck mode, while switch S_4 uses a variable duty cycle γ_4 in boost mode. It can be seen in Figure 5 that by using one half of the topology as a buck and the other half as a boost converter, the inductor is energised and de-energised simultaneously after the rise time of the inductor current i_L. The average inductor current equals the output current, in this case, the battery current i_{bat}. Because of the characteristic of inductor voltage v_L, the buck + boost mode can significantly reduce the current ripple Δi_L compared to the buck–boost mode [24]. Thus, for buck + boost mode, if the duty cycle γ_1 of switch S_1 is assumed to be constant, the duty cycle γ_4 for switch S_4 is according to Equation (1) with the input voltage V_{dc} and output voltage V_{bat}:

$$\gamma_4 = 1 - \frac{\gamma_1 \cdot V_{dc}}{V_{bat}} \tag{1}$$

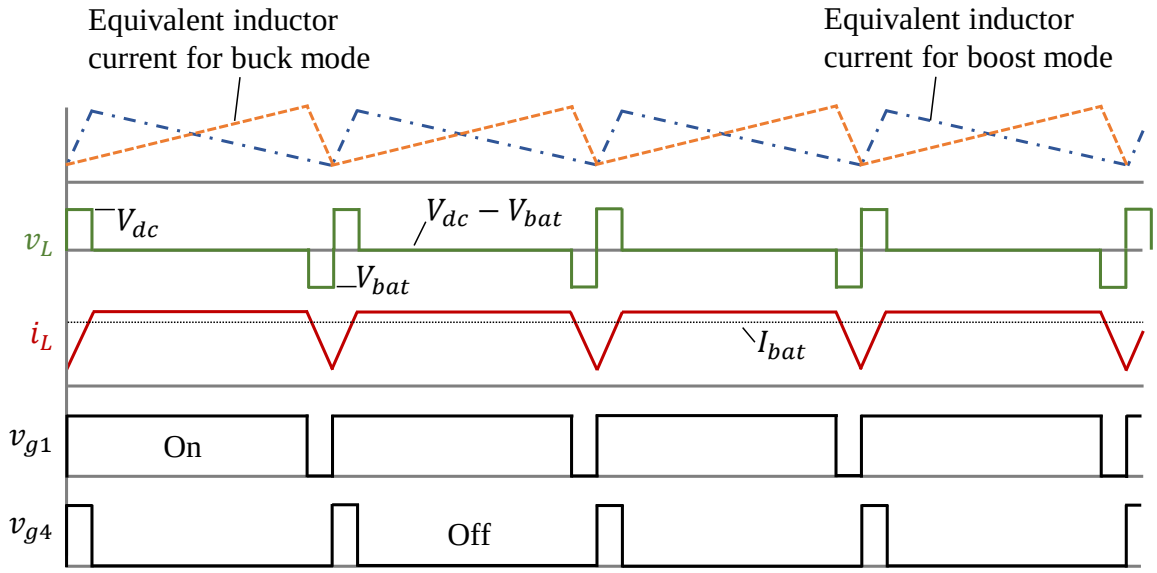

Figure 5. Characteristic of the inductor current and voltage in buck + boost mode.

However, the question of how exactly the fixed duty cycle γ_1 with an appropriate transition should be determined remains. Reference [25] confirms this statement as the literature to date does not address this topic adequately with regard to converter efficiency, and there is no appropriate investigation regarding the optimum fixed duty cycle γ_1 [26–28]. The duty cycle γ_1 for switch S_1 depends on the hysteresis, the range at which the converter should operate in buck and boost mode. This range is necessary to ensure a smooth transition between the operation modes and considers the voltage ripple on the DC bus, as shown in Figure 6 with a transition of 5%. Voltage ripples on the DC bus are typically around 10% of the DC component [29]. Therefore, it is reasonable to assume a reduction of the input voltage for the buck part with a duty cycle between 0.8 and 0.95, with sufficient input and output capacitance for voltage stabilisation.

Figures 4 and 5 illustrate the voltage–time areas of the inductor. The maximum current ripple Δi_L in a period T_s always occurs for the state with the highest voltage level on the inductor. The buck + boost mode is analysed further in the following discussion with Figures 5 and 7. As mentioned before, the power flow for this study is from the DC bus to the battery. Figure 7a illustrates the first state, where the inductor voltage equals the

DC bus voltage ($v_L = V_{dc}$). Figure 7b is the second state, where the inductor voltage is the difference between input and output voltages ($v_L = V_{dc} - V_{bat}$), and Figure 7c is the last state, where the inductor voltage equals the battery voltage ($v_L = V_{bat}$). In order to calculate the current ripple, state two is irrelevant as the voltage on the inductor cannot exceed the voltage level of input or output. Therefore, if the DC bus voltage is higher or equal to the battery voltage ($V_{dc} \geq V_{bat}$), it is possible to calculate the current ripple with the law of induction and Figure 7a with the current dependent inductance $L(I_L)$ of the powder cores, and period T_1 of the first state:

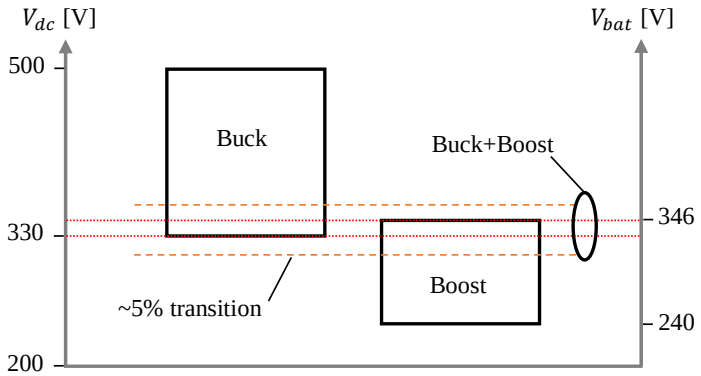

Figure 6. Mode selection for the bidirectional cascaded buck and boost converter.

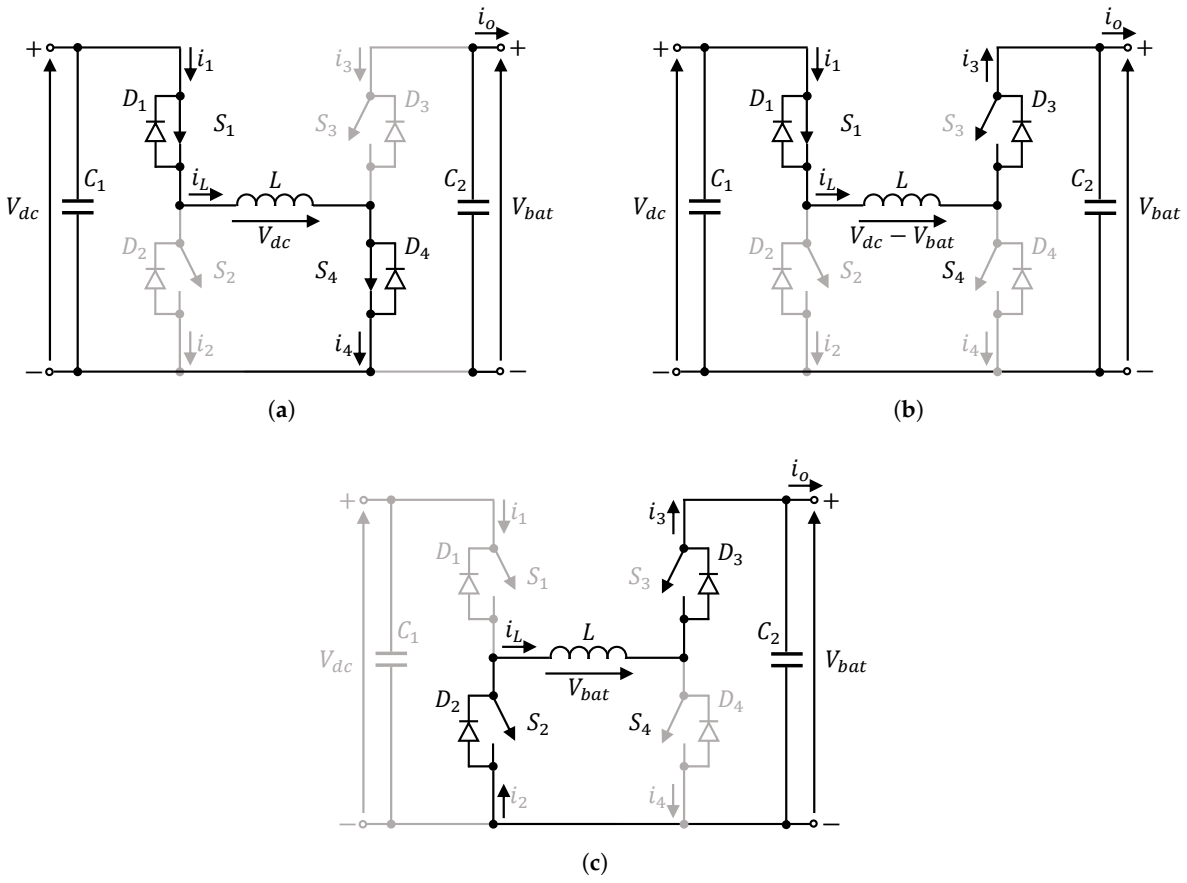

Figure 7. The three operating states of the bidirectional cascaded buck and boost converter in buck + boost mode: (**a**) first operating state in buck + boost mode with switches S_1 and S_4 turned on; (**b**) second operating state in buck + boost mode with switch S_1 turned on and and S_4 turned off; (**c**) third operating state in buck + boost mode with switches S_1 and S_4 turned off.

$$\Delta I_L = \int_0^{T_1} \frac{v_L}{L(I_L)} dt = \frac{v_L}{L(I_L)} \cdot T_1 = \frac{V_{dc}}{L(I_L)} \cdot T_1 \quad (2)$$

This first state energises the inductor for the period $T_1 = T_s \cdot \gamma_4$ according to Figures 5 and 7a. The switching frequency is defined as $f_s = 1/T_s$. Therefore, the current ripple is:

$$\Delta I_L = \frac{V_{dc} \cdot \gamma_4}{L(I_L) \cdot f_s} \quad (3)$$

To calculate the current ripple for $V_{dc} \leq V_{bat}$, the characteristics illustrated in Figure 7c define the voltage on the inductor. Using the law of induction for the third stage during time period T_3, the current ripple is:

$$\Delta I_L = \frac{V_{bat}}{L(I_L)} \cdot T_3 \quad (4)$$

In the third state, the period equals the off time of switch S_1, which is $1 - \gamma_1$. Therefore, by transforming Equation (1) for V_{dc} and substitution, the current ripple is:

$$\Delta I_L = \frac{V_{bat} \cdot (1 - \gamma_1)}{L(I_L) \cdot f_s} = \frac{V_{dc} \cdot (1 - \gamma_1) \cdot \gamma_1}{(1 - \gamma_4) \cdot L(I_L) \cdot f_s} \quad (5)$$

Equations (3) and (5) are valid for both buck–boost and buck + boost mode. From Equation (5), it is evident that for the buck–boost mode, the current ripple Δi_L is way higher for equal input and output voltages, as both duty cycles are 0.5.

The experimental setup uses parameters for validation according to the investigation in [30]. The authors in [30] assume an electric vehicle with approximately one-ton mass and a maximum DC bus current of 480 A. Generally, the maximum motor power in FCHVs is supplied 70% by the fuel cell stack and 30% by the battery [24]. The study in [30] uses a DC bus voltage of 300 V and a maximum power of 144 kW. Increasing the DC bus voltage (e.g., 500 V) decreases the maximum current. Therefore, according to the data of the FCHVs Hyundai Nexo and Honda Clarity Fuel Cell and the results of [30], this article uses the following parameters for the experimental setup:

- Maximum converter power in buck + boost mode, $P_{max} = 19.8$ kW;
- DC bus voltage range, $V_{dc} = 330$ V $- 500$ V;
- Battery voltage range, $V_{bat} = 240$ V $- 346$ V;
- Maximum converter current in buck + boost mode, $I_{max} = 60$ A;
- Maximum current ripple, $\Delta I_{L,max} \approx 31.2$ A;
- Input and output capacitance, $C_i = C_o = 200$ µ F;
- Inductance, $L(60\text{ A}) \approx 222$ µ H.

3. Experimental Setup

The DC power supply consists of three rectifiers connected in parallel with variable transformer ratio. In this way, a maximum input voltage of 500 V can be preset in the laboratory to emulate the DC bus voltage of the fuel cell system with a maximum current of 60 A. The load is a controlled resistance. Figure 8 shows the experimental setup of the converter with the associated measurement equipment. In order to measure converter power losses, the setup contains the LMG671 PowerAnalyzer. For current and voltage measurement, the setup includes the Rogowski current probe Teledyne LeCroy T3RC0120-UM and the voltage probe Fluke SI 9001. With the air/water heat exchange system AirCool Ventus ACVE 002, the RG76002 water-cooled heat sink has a coolant temperature of approximately 30 °C. The half-bridge modules are the SKM400GB066D from Semikron with the thermal interface material HT-C3200. With the Benning MM12 insertion temperature probes, the setup enables the measurement of device junction temperature. For this reason, the temperature sensor is placed inside the case, directly on the silicon die, as shown in

Figure 9. In addition, the setup contains probes to measure ambient temperature. For power loss measurement, the power analyser is connected to the input and output of the converter. Therefore, the power loss analysis does not consider losses from the gate driver, controller, and cooling system.

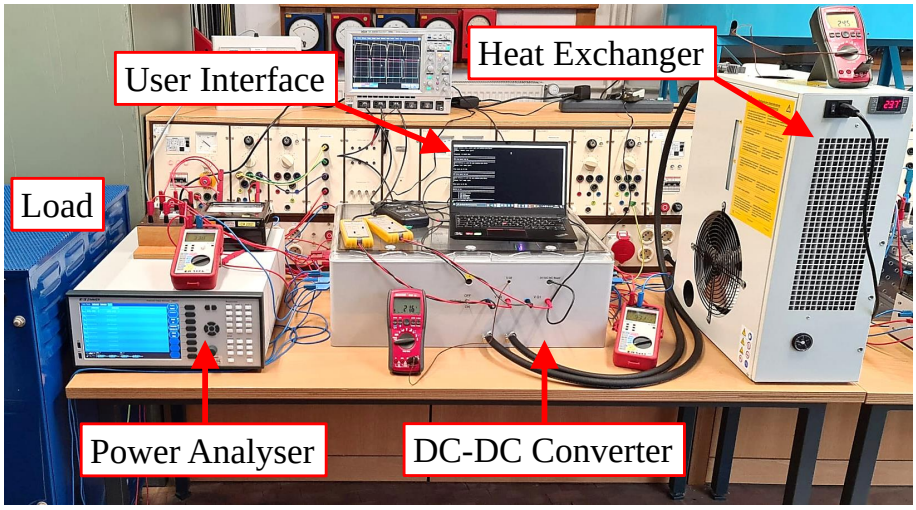

Figure 8. Full experimental setup; bidirectional cascaded buck and boost converter.

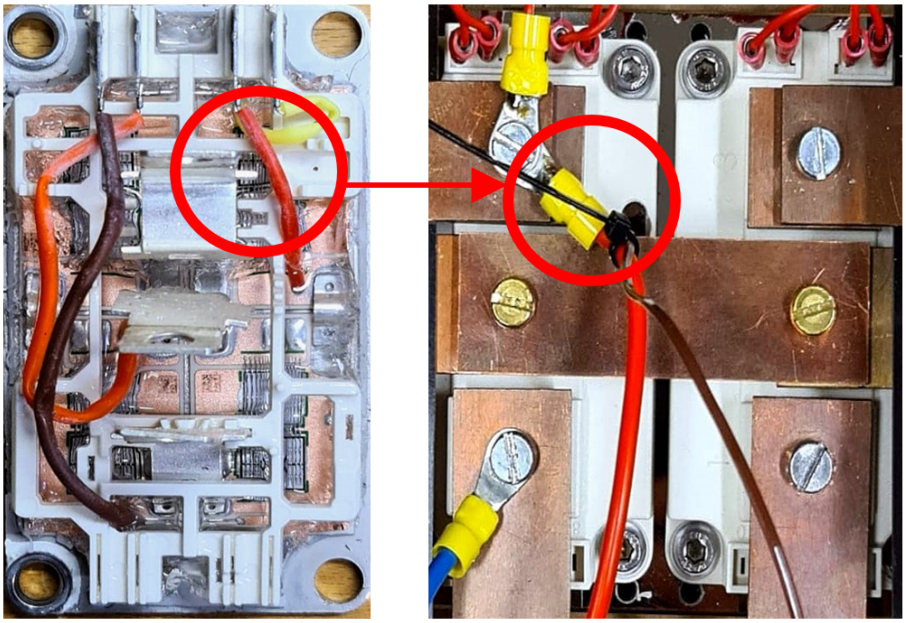

Figure 9. Half-bridge modules highlighting temperature measurement.

4. Critical Conduction Mode with Adapted Switching Frequency (CrCMASF)

A common method to decrease converter losses is to adjust the switching frequency f_s depending on the load. DC–DC converters include DC inductors designed for a specified maximum current ripple $\Delta i_{L,max}$. Authors in the published literature adjust the switching frequency depending on the load until reaching efficiency maximum, as shown in [31]. However, in the mid-kW range, realising switching frequency modulation is challenging since the inductor usually consists of ferrite cores with low saturation flux densities (0.3–0.4 T) with almost constant inductance over the entire power range [32,33]. So far, no research has been published for the converter topology shown in Figure 3 in the relevant power range with respect to the application of switching frequency modulation for the buck + boost mode.

Semiconductor switching losses dominate converter losses for the power range of interest using Si-IGBTs. For this reason, it is necessary to reduce the switching frequency to improve efficiency. However, at low switching frequencies, the current ripple Δi_L increases significantly, which in turn causes the AC flux density to rise, resulting in high losses on the magnetic cores. Consequently, the risk of reaching saturation is high. Moreover, the DC–DC converter could reach the DCM, and in terms of controller design, DCM should always be avoided. Solving these issues is possible by using powder cores with soft saturation characteristics and high saturation flux densities (0.5–1.5 T) [32,33]. The dependence of the powder cores inductance on the output current is due to the DC magnetising force-dependent permeability [34].

The following section presents a simple way to estimate power losses. The aim is to illustrate the power loss distribution of the components. The main power loss contributors are the half-bridge modules, inductor, and output capacitors. Due to the limitations of the experimental setup, the validation refers to total converter losses. Furthermore, the estimations assume a junction temperature of approximately 50 °C as the experimental setup cannot measure junction temperatures of all IGBTs and diodes.

A simple way to estimate the losses of half-bridge modules is to use the loss characteristics from the datasheet. Compared to mathematical–analytical models, which can predict the switching behaviour accurately, this method has less effort without data acquisition, for example, the parasitic inductances and the transient turn-on and turn-off characteristics.

The power losses of Si-IGBT half-bridge modules are divided into conduction and switching losses. The losses occur during the power flow from the DC bus to the battery on switch S_1 (P_{s1}), switch S_4 (P_{s4}), diode D_2 (P_{d2}), and diode D_3 (P_{d3}). Therefore, the total average power loss of both Si-IGBT half-bridge modules P_{mod} is:

$$P_{mod} = P_{s1} + P_{s4} + P_{d2} + P_{d3} \tag{6}$$

In Equation (6) the power losses of the IGBTs (P_{s1} and P_{s4}) are composed of switching losses ($P_{sw,1}$ and $P_{sw,4}$) and conduction losses ($P_{ci,1}$ and $P_{ci,4}$) and diode losses of reverse recovery losses ($P_{err,2}$ and $P_{err,3}$) and forward conduction losses ($P_{cd,2}$ and $P_{cd,3}$). Estimating the conduction losses of IGBTs $P_{ci,i}$ and diodes $P_{cd,i}$ is possible with the forward characteristic. The conduction losses of each IGBT for a periodic collector current i_c, and on-state resistance r_d is:

$$P_{c,i} \approx \frac{1}{T_s} \int_0^{T_s} (V_{tm} + r_d \cdot i_c) i_c dt \tag{7}$$

The calculation of Equation (7) is possible with the definition of the on-state voltage V_{ce} using the threshold voltage V_{tm} of the IGBTs; the calculation for the conduction losses of the diodes is possible with the same procedure:

$$V_{ce} = V_{tm} + r_d \cdot i_c \tag{8}$$

The diode and IGBT's threshold voltage and on-state resistance are temperature-dependent and determined according to the output characteristics, and the on-state parameters from the datasheet [35].

Switching losses of Si-IGBT half-bridge modules are the major contributor to converter losses in the specified power range. Accordingly, the converter losses depend on the switching frequency. The switching losses occur during the transient turn-on and turn-off process, where the current trough and voltage on the IGBT lead to power losses. The reverse recovery losses of the diodes occur during their turn-off due to the reverse current and voltage. Accordingly, the estimation of the losses is possible with the turn-on energy E_{on}, turn-off energy E_{off}, and reverse recovery energy E_{rr}:

$$P_{sw} \approx f_s \cdot (E_{on} + E_{off}) \tag{9}$$

$$P_{err} \approx f_s \cdot E_{rr} \tag{10}$$

Using the datasheet of the Si-IGBT half-bridge modules, it is possible to determine the switching energy and reverse recovery energy as a function of collector current i_c, collector-emitter voltage V_{ce}, gate resistance R_g, and junction temperature T_j by normalising the respective characteristic with nominal values of the datasheet and by determining the respective coefficients (k_C, K_r, K_i, and K_v) [35]:

$$E = E_{ref} \cdot (1 + k_C(T_j - T_{j,ref})) \cdot \left(\frac{R_g}{R_{g,ref}}\right)^{K_r} \cdot \left(\frac{i_c}{i_{c,ref}}\right)^{K_i} \cdot \left(\frac{V_{ce}}{V_{ce,ref}}\right)^{K_v} \tag{11}$$

The power losses of an inductor are divided into winding losses and core losses. The changing magnetic flux field within the core material generates core losses due to the poor magnetic response. Fore core loss estimation, three methods are of interest regarding effort and accuracy. The Steinmetz equation (SE), the modified Steinmetz equation (MSE), and the improved generalized Steinmetz equation (iGSE). These methods use the so-called Steinmetz parameters (k, α, and β), which are material constants for determining the specific core losses. However, these parameters apply to a sinusoidal voltage. In the case of a DC–DC converter (square voltage on the inductor), this method is not reasonable due to the dependence of the losses on the duty cycle γ. Using the SE is not reasonable due to the parameters which refer to a sinusoidal voltage on the inductor. The iGSE accuracy decreases for duty cycles above or less than 0.5 [36]. However, in this study, the square voltage on the inductor has a short duty cycle. Moreover, the iGSE has no DC bias sensitivity [37]. For these reasons, this study uses the MSE, which assumes losses are proportional to f^2 and f^α which is a drawback as its accuracy deceases for $\alpha \neq 2$ [38]. The simple MSE is reasonable in this study to estimate the core loss for a non-sinusoidal excitation with the peak flux density B_{pk} [39]:

$$P_{c,mse} \approx f_s \left(k \cdot f_{eq}^{\alpha-1} \cdot B_{pk}^{\beta}\right) \tag{12}$$

In Equation (12), f_s is the switching frequency, and f_{eq} is the equivalent frequency. The equivalent frequency improves the SE accuracy. This equivalent frequency assumes that the core losses are related to the ripple value of flux density ΔB and the change rate of flux density $dB(t)/dt$ over the period T_s [39]:

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^{T_s} \left(\frac{dB(t)}{dt}\right)^2 dt \tag{13}$$

However, this approach has a significant drawback. As Figure 5 illustrates, the voltage across the inductor for the buck + boost mode does not have the typical square voltage waveform as, for example, in a buck converter. In the buck + boost mode, the current and, therefore, the magnetic flux density shapes are trapezoidal. As a result, the inductor voltage is positive, negative, or zero. Therefore, the core flux increases, decreases, or remains constant. Accordingly, there is no magnetisation or demagnetisation process in the second stage. However, in this second stage, the so-called relaxation losses occur (magnetic-after-effect loss). An appropriate method to consider this effect is the improved–improved generalised Steinmetz equation (i^{2}GSE) [36]. However, while this approach is accurate, additional measurements and effort are necessary, which would be out of the scope of this study. The MSE is sufficient to illustrate an estimated loss distribution of Si half-bridge modules and magnetic cores.

Another power loss contributor of the inductor is the winding of the cores. The winding losses P_w consist of DC losses $P_{w,dc}$ due to the DC resistance R_{dc} and AC losses $P_{w,ac}$ due to skin and proximity effect:

$$P_w = P_{w,dc} + P_{w,ac} \tag{14}$$

The DC losses depend on the DC resistance of the winding, which is defined as the product of total wire length l_w and its resistivity ρ_w:

$$R_{dc} = l_w \cdot \rho_w \tag{15}$$

The inductor of the experimental setup uses a solid round copper wire. Considering the skin effect is possible with the skin effect factor $F_w(n)$ with Equation (17) and proximity effect with the factor $G_w(n)$ using Equation (18). The AC losses of the winding is the sum of the harmonic components n of the RMS currents considering the distribution of the number of turns over n_L layers [40]:

$$P_w \approx R_{dc} \cdot I_{dc,rms}^2 + R_{dc} \sum_n (I_{ac,rms,n})^2 \cdot \left(F_w(n) + \frac{n_L^2 - 1}{3} \cdot G_w(n) \right) \tag{16}$$

$$F_w(n) = \xi \cdot \frac{sinh(2\xi) + sin(2\xi)}{cosh(2\xi) - cos(2\xi)} \tag{17}$$

$$G_w(n) = 2\xi \cdot \frac{sinh(\xi) - sin(\xi)}{cosh(\xi) + cos(\xi)} \tag{18}$$

To determine the skin and proximity factors, the skin depth δ_{skin} of the non-sinusoidal inductor current is necessary. The definition of the skin depth, using permeability of free space μ_0, relative permeability μ_r, and the equivalent switching frequency, is [41]:

$$\delta_{skin} = \sqrt{\frac{\rho_w}{\pi \cdot f_{eq} \cdot \mu_0 \cdot \mu_r}} \tag{19}$$

As the inductor has a single-layer design with solid round conductors, calculating the porosity factor K_L is possible with the number of turns N, their width a, and inner width of the core b [40]:

$$K_L = \frac{N \cdot a}{b} \tag{20}$$

Finally, determining the skin effect factor and proximity factor is possible with the relative thickness of the single strand ξ. The term ξ is defined as the ratio of the height of a winding layer divided by the skin depth. In order to determine the height of the winding layer, it is necessary to transform the round wire thickness with the radius r_L into a square conductor of the same cross-sectional area. Therefore, ξ is [40]:

$$\xi = \frac{d_{opt}}{\delta} \cdot \sqrt{K_L} \tag{21}$$

In Equation (21) d_{opt} is the equivalent wire thickness. For a round wire with the radius r_L, the equivalent wire thickness is [40]:

$$d_{opt} = r_L \cdot \sqrt{\pi} \tag{22}$$

The determination of capacitor losses P_{cap} with Equation (23) are straightforward and consist of the losses caused by the equivalent series resistance (ESR) $R_{c,esr}$ and rms current $I_{c,rms}$:

$$P_{cap} = R_{c,esr} \cdot I_{c,rms}^2 \tag{23}$$

Accordingly, considering the Si half-bridge modules, inductor, and capacitors, the overall power loss of the converter P_{tot} is:

$$P_{tot} = P_{mod} + P_{c,mse} + P_w + P_{cap} \tag{24}$$

Using Equation (24), Figure 10 illustrates the power loss distribution for a fixed switching frequency of 20 kHz, γ_1 = 0.95 and overlapping input and output voltages of

330 V. According to Figure 10, it is evident that the power losses of the half-bridge modules dominate overall converter losses. Compared to inductor losses, the half-bridge modules dissipate more losses by a factor of 11. In conclusion, the motivation for the novel modulation method is to decrease the switching frequency to reduce the losses of the half-bridge modules as far as possible to achieve a balanced power loss distribution. Therefore, the aim is to operate in CrCM by adapting (reducing) the switching frequency. Hence, the CrCMASF operates at the boundary limit between CCM and DCM.

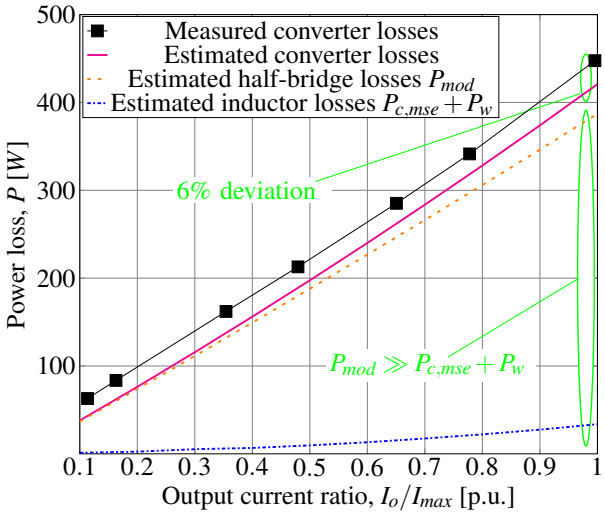

Figure 10. Power loss distribution of the converter for a fixed switching frequency of 20 kHz.

It is necessary to ensure an inductance at the maximum current for a specified current ripple for powder core design. The maximum current ripple for this study is approximately 31.2 A with a maximum switching frequency of 20 kHz.

The experimental setup, introduced in the previous section, uses an inductor consisting of three parallel-connected cores (58,617 from magnetics), each with three stacks and 39 turns of winding (size: AWG10) and can be seen in Figure 11. The inductance at the maximum output current of 60 A is approximately 222 µF.

Figure 12a illustrates the behaviour of the inductance L as a function of the inductor current I_L. Figure 12b presents the switching frequency for overlapping input and output voltages of 330 V—Equation (25) for $V_{dc} \geq V_{bat}$ or Equation (26) $V_{dc} \leq V_{bat}$:

$$f_s = \frac{V_{dc} \cdot (1 - \gamma_1) \cdot \gamma_1}{(1 - \gamma_4) \cdot L(I_L) \cdot \Delta I_{L,max}} \tag{25}$$

$$f_s = \frac{V_{dc} \cdot \gamma_4}{L(I_L) \cdot \Delta I_{L,max}} \tag{26}$$

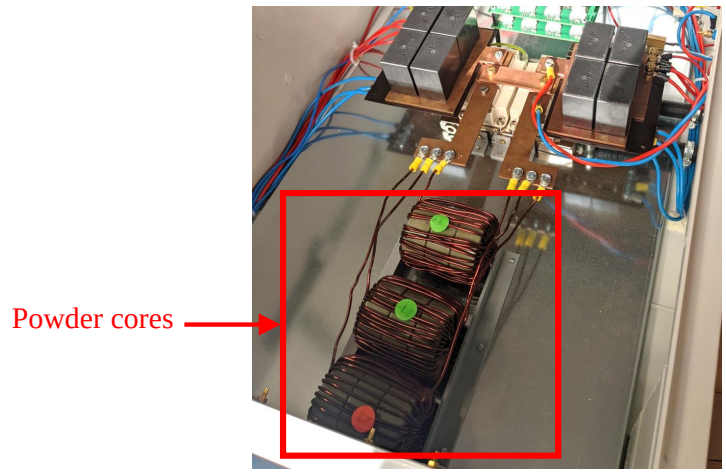

Figure 11. Powder cores of the experimental setup.

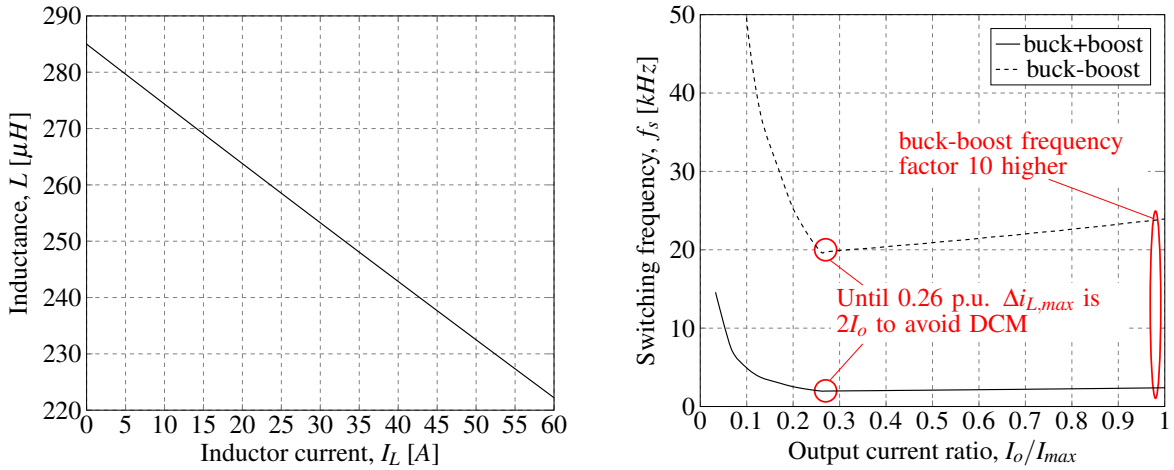

Figure 12. Inductance–current relationship of the powder cores and corresponding switching frequency for buck + boost mode and buck–boost mode: (**a**) inductance versus inductor current; (**b**) switching frequency for buck–boost and buck + boost mode for overlapping input and output voltages of 330 V.

From Figure 12b, it is evident that switching frequency modulation is not reasonable for buck–boost mode as the switching frequency f_s is not below the maximum of 20 kHz at all operation points. However, the switching frequency needs to decrease due to the high power semiconductor switching losses to enhance efficiency. On the other hand, using buck + boost mode, low switching frequencies are possible, enabling efficiency optimisation. The definition of the current ripple Δi_L is according to the law of induction and the effective inductor voltage–time areas for both modes in Figures 4 and 5. Both figures reveal that these areas are significantly larger for buck–boost mode. In contrast, in buck + boost mode, the inductor is temporarily energised and de-energised simultaneously, enabling low current ripples. The converter also considers a minimum frequency to avoid DCM by using Equations (25) and (26), therefore setting the maximum current ripple $\Delta i_{L,max}$ according to the boundary limit between DCM and CCM, which is $2I_o$ for output currents of up to 15.6 A (0.26 p.u.). The procedure uses a maximum current ripple of 31.2 A for output currents above 15.6 A. Therefore, for an output current of 60 A, a switching frequency of approximately 2 kHz is possible, as shown in Figure 12b. With Figure 12b and Equations (25) and (26), it is possible to set the switching frequency for the experimentation phase accordingly.

Figure 13 illustrates the estimated power loss distribution for overlapping input and output voltages of 330 V, γ_1 = 0.95, and CrCMASF. Compared to the results in Figure 10, the introduced CrCMASF significantly reduces power semiconductor losses. However, due to the reduced switching frequency and increased AC flux density, inductor losses increase. Nevertheless, this analysis justifies the CrCMASF, as the losses of half-bridge modules approach inductor losses, reducing overall converter losses. The subsequent section will validate these assumptions further for different fixed duty cycles and input and output voltage ratios.

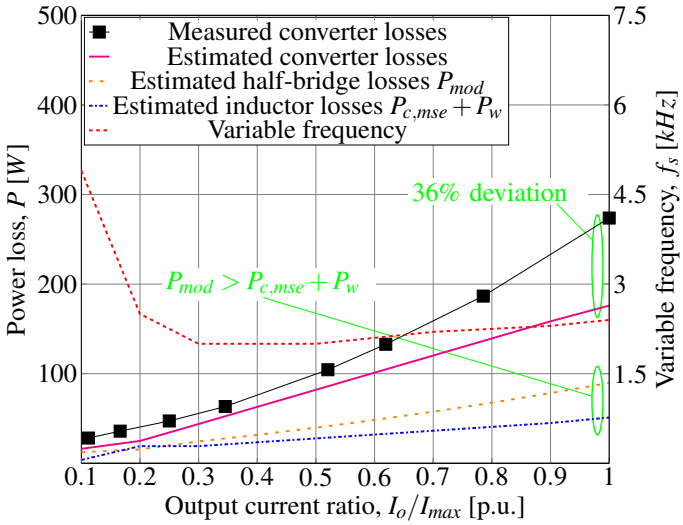

Figure 13. Power loss distribution of the converter for CrCMASF.

5. Evaluation

5.1. Converter Losses

Figure 14 presents the power losses P of the converter for a fixed switching frequency of 20 kHz and CrCMASF according to Equation (25) with input and output voltages of 330 V. For a duty cycle γ_1 of 0.95, Figure 14a reveals that the losses with switching frequency modulation at full-load are ∼274 W. In contrast, Figure 14b depicts power losses of ∼339 W for γ_1 = 0.9 and Figure 14c ∼388 W for γ_1 = 0.8. Hence, a duty cycle γ_1 of 0.95 decreases losses by up to 20% compared to a duty cycle γ_1 of 0.9 and 25% compared to a duty cycle γ_1 of 0.8. Moreover, the high duty cycle of γ_1 = 0.95 for switch S_1 decreases the switching frequency according to Equation (25). For example, the converter can operate with a switching frequency of 2 kHz even at an output current of approximately 30 A without exceeding the maximum current ripple of 31.2 A. Compared to that, using Equation (25), a duty cycle of 0.9 only enables a switching frequency of 4 kHz, whereas a duty cycle of 0.8 enables a switching frequency of 7 kHz for this operating point. As the switching losses of the Si-IGBT half-bridge modules dominate converter losses, the high duty cycle of 0.95 decreases converter losses accordingly. Due to tolerances, the switching frequency deviates from the calculated values in Figure 12 at low currents. Furthermore, compared to a constant switching frequency of 20 kHz, frequency modulation in buck + boost mode results in a power loss reduction of up to 39% by using a duty cycle γ_1 of 0.95, as Figure 14a illustrates.

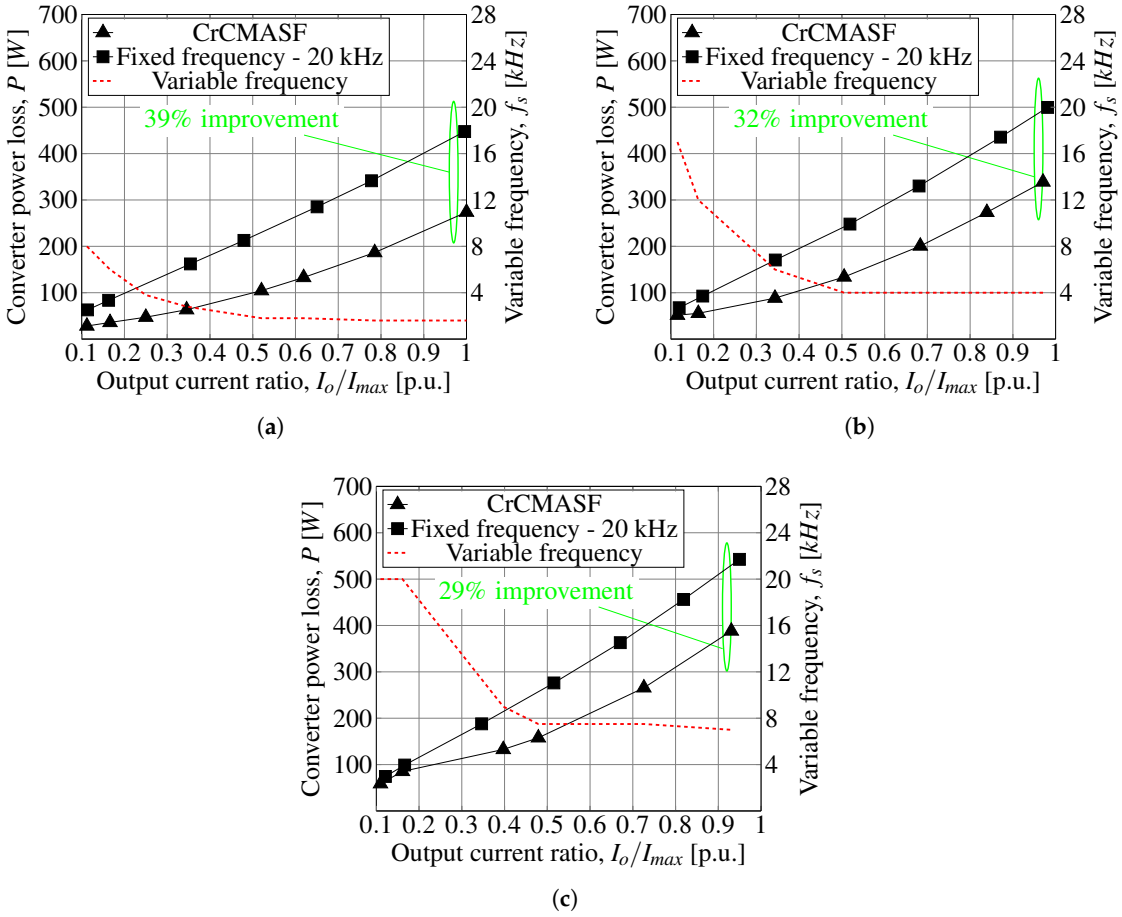

Figure 14. Measured converter losses for different duty cycles for switch 1: (**a**) converter losses for a duty cycle of 0.95; (**b**) converter losses for a duty cycle of 0.9; (**c**) converter losses for a duty cycle of 0.8.

5.2. Device Junction Temperature

Figure 15 presents the characteristic of the junction temperature T_j of switch S_1 for input and output voltages of 330 V: Figure 15a for a duty cycle γ_1 of 0.95, Figure 15b for γ_1 = 0.9, and Figure 15c γ_1 = 0.8. The junction temperature was recorded after the heat exchanger stopped its active cooling process for a meaningful comparison with a coolant outlet temperature between 30–33 °C. The coolant outlet temperature is not constant, and the ambient temperature, which is uncontrolled, also affects the junction temperature of the device as it acts as a heat source on the case, reaching values above 45 °C in the setup. Hence, the ambient is heating up due to core, capacitor, and semiconductor losses and thermally couples to the half-bridge modules. Thus, the measurements were recorded in a preheated ambient. For this reason, the temperature rise in Figure 15 refers to the starting junction temperature $T_j(\sim 0.15\ p.u.)$ of the respective test series with Equation (27):

$$\Delta T_j = T_j(I_o/I_{max}) - T_j(\sim 0.15\ p.u.) \tag{27}$$

From Figure 15, it is evident that for all duty cycles, decreasing maximum temperature rise is possible. In addition, the temperature development for the proposed modulation method indicates a small increase over the entire power range, which means that, in contrast to fixed switching frequency, the cooling system has to use less energy to maintain the coolant temperature. The improvements are particularly noticeable for output current ratios above 0.5; switching frequencies above an output current ratio of 0.5 are relatively low with the proposed modulation method. Thus, the results from Figure 15 prove that

frequency modulation in buck + boost mode is also an appropriate optimisation method to decrease device junction temperature rise ΔT_j for the entire power range.

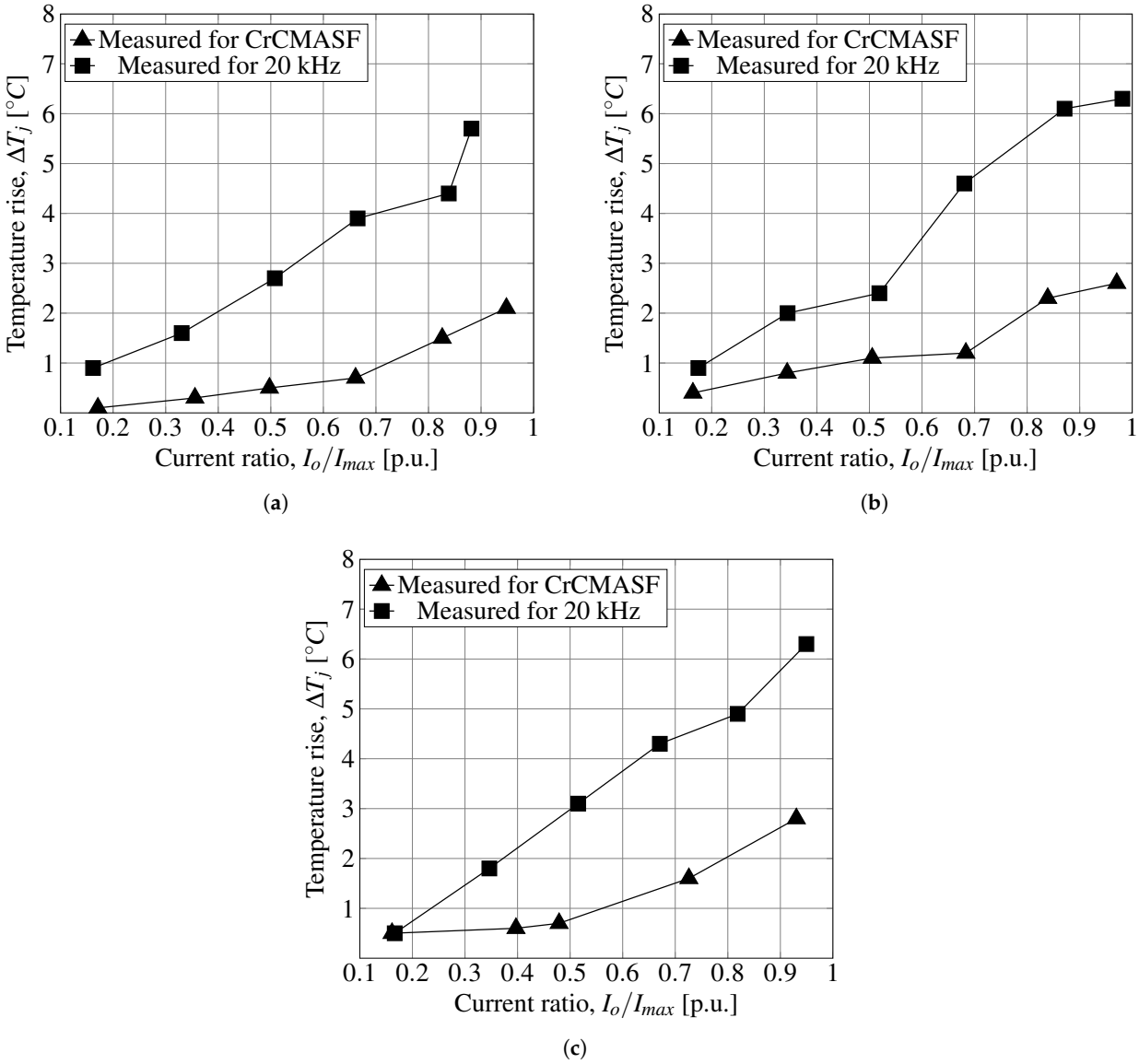

Figure 15. Junction temperature of switch 1 for different duty cycles: (**a**) junction temperature for a duty cycle of 0.95; (**b**) junction temperature for a duty cycle of 0.9; (**c**) junction temperature for a duty cycle of 0.8.

5.3. Converter Efficiency

Figure 16 presents the efficiency η of the converter for input and output voltages of 330 V and a duty cycle γ_1 of 0.95. Figure 16a shows the results for overlapping input and output voltage of 330 V, Figure 16b for an output voltage of 315 V, and Figure 16c for an output voltage of 363 V. The proposed modulation method improves efficiency by up to 1.43% for overlapping input and output voltages, 1.23% for an output voltage of 315 V, and 1.19% for an output voltage of 363 V. The results demonstrate that significant efficiency improvement is possible with the proposed duty cycle γ_1 of 0.95 and the use of switching frequency modulation and powder cores.

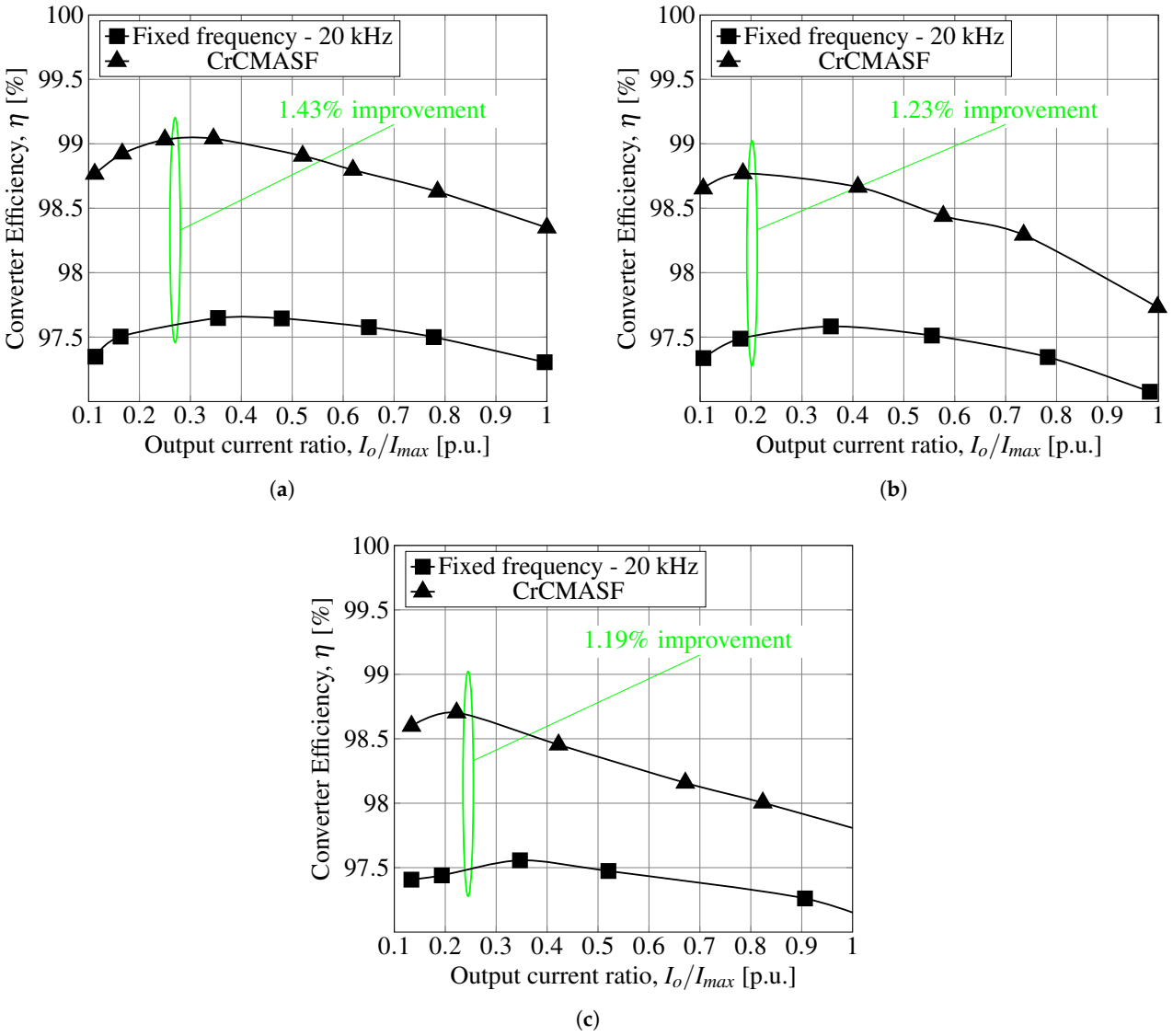

Figure 16. Converter efficiency for a duty cycle of 0.95 and an input voltage of 330 V for different output voltages: (**a**) converter efficiency for an output voltage of 330 V; (**b**) converter efficiency for an output voltage of 315 V; (**c**) converter efficiency for an output voltage of 363 V.

5.4. Converter Characteristics

Figure 17 illustrates the inductor current ripple Δi_L (only AC component) and voltage $v_{ce,s1}$ on switch 1 and voltage $v_{ce,s4}$ on switch 4 for overlapping input and output voltages of 330 V. According to Figure 12a for the inductance $L(I_o)$ and Equation (25), the current ripple Δi_L for 20 kHz in Figure 17a should be 3.4 A, and in Figure 17b for CrCMASF, it should be 33 A. Hence, the current ripple approximately matches the estimations. Deviations are due to the tolerance of the core. For example, the inductance factor A_L of the core has ±8% accuracy, while this parameter is crucial for core inductance determination [42].

In contrast to Figure 17, Figure 18 depicts inductor current ripple Δi_L and inductor voltage v_L in CCM and DCM. In Figure 18a, the characteristics in CCM are as anticipated (see Figure 5). For small output currents, the converter will reach DCM, where the relationship between duty cycles and output voltages shown in Equation (25) is lost as the inductor current i_L temporarily reaches the value of zero, and thus, the voltage on the inductance v_L. Consequently, the positive voltage–time area of V_{dc} shown in Figure 5 on the inductor no longer applies in DCM, and the mean value of the output voltage, in this case, the battery voltage V_{bat}, increases. Figure 18b,c elucidate this behaviour.

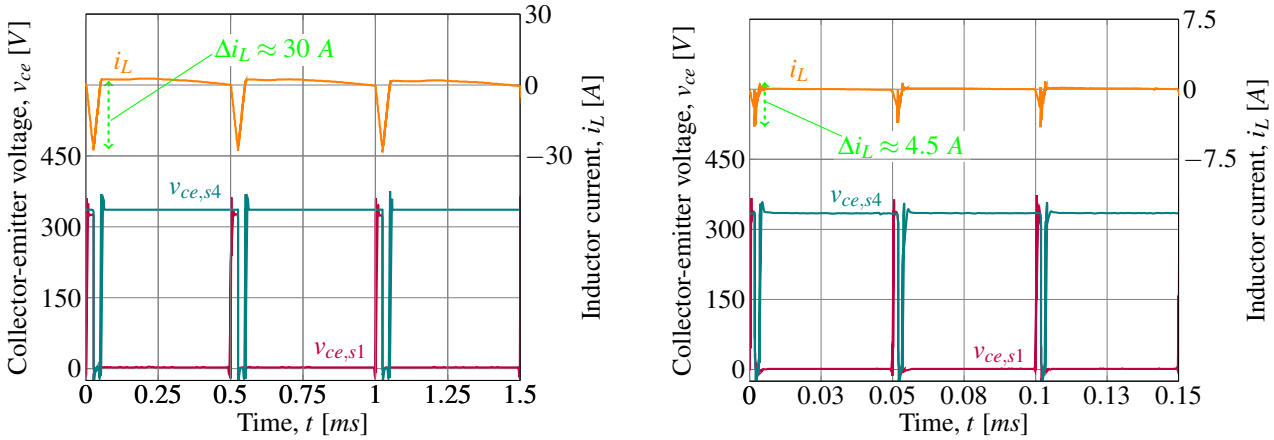

Figure 17. Characteristics for the inductor current ripple and voltages on switches S_1 and S_4: (**a**) converter characteristics for input and output voltages of 330 V with 2 kHz and an output current of 30 A; (**b**) converter characteristics for input and output voltages of 330 V with 20 kHz and an output current of 30 A.

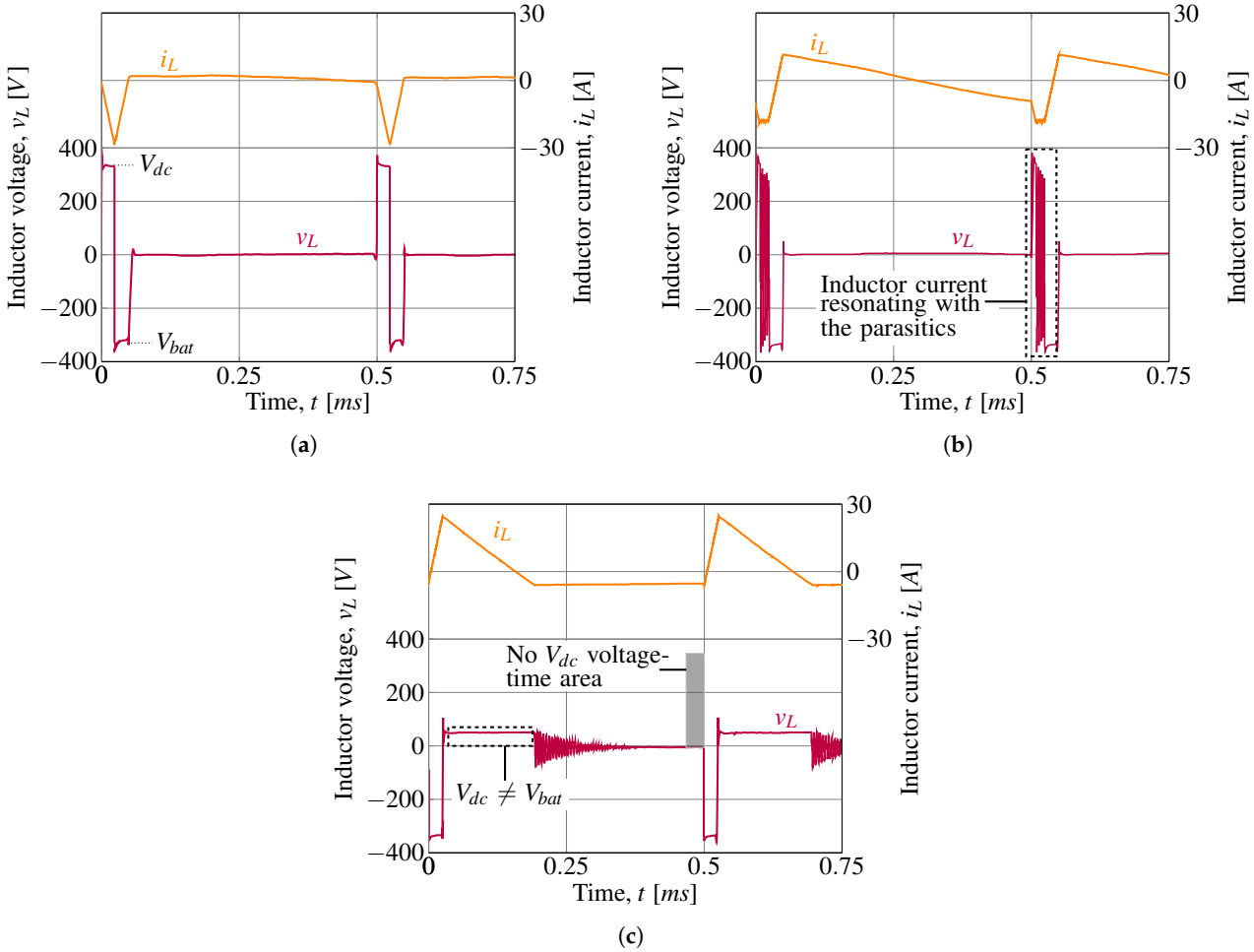

Figure 18. Inductor characteristics in CCM and DCM for different output currents: (**a**) inductor characteristics for an output current of 34 A in CCM; (**b**) inductor characteristics for an output current of 16 A in CCM; (**c**) inductor characteristics for an output current of 5 A in DCM.

If the converter reaches the DCM mode only for a short time, then the positive voltage-time area of V_{dc} is partly missing, as shown in Figure 18b. The output voltage for Figure 18b is 347 V. Hence, the voltage increases by 5.2% compared to CCM. In addition, the oscillating behaviour is present due to the parasitics of the active components and the current remaining in the inductor—for example, the freewheeling diode's parasitic capacitance results in an LC oscillation.

By decreasing the switching frequency or by reducing the output current further, as in Figure 18c, the inductor current will operate in DCM for a longer period. Consequently, the positive voltage–time area V_{dc} is no longer on the inductor. Hence, the output voltage increases drastically to 380 V, which is an increase of 15.2% compared to CCM. Due to this increase in the output voltage, the difference between the input and the output voltage is no longer zero ($V_{dc} \neq V_{bat}$), as shown in Figure 18c.

These findings underline the importance of avoiding the DCM for converter control.

6. Discussion

The presented results have proven that switching frequency modulation is possible and reasonable for the buck + boost mode in the mid-kW range. However, the simple approach of this study (CrCMASF) for the introduced DC–DC converter is only possible for the mid-kW range, as for converters with lower output powers, the magnetic core losses could represent the majority of converter losses. The authors in [18,43,44] analyse this aspect and show that by decreasing the switching frequency, the switching losses for power semiconductors decrease while core losses increase. Hence, the optimum switching frequency can differ significantly depending on the converter's electric properties. Therefore, depending on the application, the ratio of losses must be essential for efficiency optimisation when using switching frequency modulation. Another aspect to consider is semiconductor technology. For example, by using SiC-MOSFETs instead of Si-IGBTs, it is possible to decrease the impact of semiconductor losses on converter efficiency. In this case, the cores could mainly impact the converter power losses. Consequently, if cores are the main factor of the total losses, it is reasonable to increase the switching frequency to reduce the AC flux density. However, the results of this study evince that lower switching frequencies are reasonable for the mid-kW range using Si-IGBTs since they are the main factor of converter losses.

The method of switching frequency modulation is already known, as introduced in [45] for ZVS or in [31,43,45,46] where the authors predict losses and the reasonable switching frequency with complex algorithms or optimum efficiency tracking as introduced in [47]. However, the drawback of these approaches is that their applicability is limited to low power ranges. Furthermore, the known methods require an increased effort of computations. In addition, none of these methods uses the soft saturation effect of powder cores.

Regarding the duty cycles for the buck + boost mode, published literature discusses and analyses the optimum not regarding the converter efficiency [48–50] or for lower power ranges [51].

The results of this study prove that a high fixed duty cycle γ_1 of 0.95 and switching frequency modulation increase efficiency over the entire power range and decrease device junction temperature rise.

In order to compare the introduced approach for the bidirectional cascaded buck and boost converter with the published literature, Table 2 lists references with their most important properties.

Starting at the top of Table 2, the authors in [28] investigate the buck + boost mode for efficiency enhancement in the high-kW range. The authors in [28] point out that switching frequency reduction for the buck + boost mode is reasonable. The article [28] demonstrates the calculation of the minimum switching frequency to meet the inductor's current ripple requirements. Accordingly, the authors reduce the fixed switching frequency (FSF) from 12 kHz to 10 kHz to increase efficiency in the buck + boost mode. However, unlike what is

presented in this article, the authors in [28] do not use an adaptive procedure to operate in CrCM. Instead, they reduce the FSF to 10 kHz for the entire power range in buck + boost mode. Another approach is presented in [16], where the authors compare FSF with CrCM. The results of [16] confirm the assumption of this article: in order to operate in the CrCM, the authors have to increase the switching frequency while not exceeding the maximum inductor current ripple. Therefore, it is assumed that the authors in [16] are not using a magnetic core with the soft-saturation effect. Accordingly, due to the increased switching frequency in CrCM, the converter only achieves efficiencies of up to 95%. Moreover, it is unclear if the results in [16] also refer to overlapping input and output voltages.

Table 2. Literature review comparison.

Reference	Modes	Peak Efficiency	Power Loss Improvement	Method	Converter Power	(+) Pros and (—) Cons
[28]	buck, boost, buck + boost	97.96	Up to 38%	FSF reduction of ∼ 17%	150 kW–200 kW	+ No additional hardware + No computational effort + Simple — No efficiency improvement for buck + boost mode documented — Doeas not avoid DCM
[16]	buck, boost, buck/boost	99%	n/a	FSF, CrCM	30 kW	+ No additional hardware + Moderate computational effort + Simple — Low efficiency of 0.95% for CrCM — No investigation for overlapping input and output voltages
[12]	buck	92%	n/a	ZVS, ZCS	1.12 kW	— Additional hardware — Low frequency even thou using soft-switching — Complex approach — Not usable for overlapping input and output voltages
[14]	buck, boost	94,4%	n/a	GaN and ZVS	100 W	+ No additional hardware + Theoretically usable for the mid-kW range — Complex — No results for overlapping input and output voltages
[13]	buck, boost, buck–boost	97%	n/a	RAIC	<2 W	+ Moderate computational effort + Theoretically usable for the mid-kW range + No pulse skipping — Complex approach — Additional hardware
This article	buck–boost buck + boost	99%	Up to 39%	CrCMASF	19.8 kW	+ No additional hardware + Moderate computational effort + Simple — Limited to powder cores — Only applicable for $P_{mod} \gg P_{c,mse} + P_w$

Going down in the power range to compare this article with the literature review presented in the first section, reference [16] disadvantages disable the authors' approach for the mid-kW range. Even though using ZVS and ZCS, their switching frequency is ∼33 kHz. The authors in [16] achieve appropriate efficiencies. However, their methods rely on additional hardware. Another approach is [14], where the authors realise ZVS using the parasitics of the power semiconductors. Unfortunately, the authors in [14] do not investigate their method for overlapping input and output voltages. Finally, Table 2 lists reference [13]. In [13], the authors introduce the reduced average inductor current (RAIC) method. Although having a complex approach, the computational effort for realisation is

moderate without additional hardware. It would be interesting to investigate the RAIC method for the mid-kW range as the authors in [13] achieved a converter efficiency of up to 97% for the low-W power range.

By comparing the references in Table 2 with the introduced approach of this article, namely the CrCMASF, it is evident that the major drawback is its limitation. The usage of CrCMASF is only possible for converters if the power losses of the power semiconductors dominate overall power losses. Moreover, the CrCMASF relies on the soft saturation characteristics of the inductor and is therefore not usable for converters based on, e.g., ferrite cores. Nonetheless, the major advantages of the CrCMASF are its simplicity and significant power loss reduction for efficiency enhancement.

7. Conclusions

This paper investigates the buck + boost mode of a non-isolated hard-switched bidirectional cascaded buck and boost converter designed for fuel cell hybrid vehicles. This study validates the operation mode with an experimental setup operating with currents of up to 60 A and 19.8 kW. As a result, this paper identifies the optimum fixed duty cycle of 0.95 for the buck part of the converter. Compared to a fixed duty cycle of 0.9 and 0.8, the proposed duty cycle reduces converter losses by 25% at maximum output power. Moreover, this study introduces the novel critical conduction mode with adapted switching frequency with powder cores for the DC–DC converter. Experimental tests confirm power loss improvement by up to 39% compared to a fixed switching frequency of 20 kHz while avoiding discontinuous conduction mode. As a result, the proposed modulation method enables efficiencies of 99%. Finally, this paper demonstrates that the suggested method decreases device junction temperature over the entire power range by reducing semiconductor power losses accordingly.

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