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Modeling and Experimental Validation of Broad Input-Output Range Three-Voltage-Level Rectifier

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Abstract: A new type of single–conversion–step wide–input–range versatile step–up/down three–voltage–level power–factor correction stage is presented in this manuscript. The rectifier can operate both in continuous–conduction mode and discontinuous–conduction mode. First, the rectifier's principle of operation is described, and then the innovative rectifier is analyzed in continuous and discontinuous–conduction modes. After, an average model for the innovative rectifier is developed. Lastly, the proposed theory is experimentally validated using a multiplier–less dual–control–loop mode at discontinuous–conduction modes. It is shown that although no multiplier is used in the control circuitry, the power factor is near unity. It is revealed that the rectifier can swing the output voltage from 50 V to 900 V while the input voltage is 230 Vrms. Although the rectifier output has a split DC bus with three voltage levels, the required control effort is low, and the output voltage is balanced. The innovative topology suits any standard power–factor correction rectifier application, dual–stage low–voltage power supply, and three–level voltage supplement for low–harmonic inverters. Since the rectifier's output–voltage swing is extremely wide, energy storage systems and electric vehicle batteries are suitable applications.

Keywords: AC–DC; EV charger; power electronics; power–factor correction; rectifier; three–voltage–level converter

1. Introduction

Rectifiers are a primary tool for delivering power from the electric grid to the local consumer by converting AC to DC voltage. Most switch–mode power converter topologies can be utilized as a single–phase power–factor correction (PFC) rectifier [1]. The basic idea is to impose a pure resistance input impedance at the rectifier input terminal. Thus, the rectifier is required to operate continuously to keep a near unity power factor and eliminate all harmonics. This principle of operation is valid for single–phase or three–phase rectifiers [2]. For this purpose, the boost converter is the most widespread rectifier; However, it imposes a minimum DC bus voltage of ~375 V (to preserve continuous operation at the maximum amplitude of the sine wave). Most residential and commercial loads are electronic circuitry that consumes DC power. However, the grid supplies pulsating power; therefore, an additional energy storage element is required to supply continuous power. The electrolytic capacitor is commonly used as a PFC output terminal energy storage element. This element is responsible for about thirty percent of PFC failures [3] due to excessive heat dissipation and high operating–voltage ripple. Nevertheless, this issue could be addressed by implementing an electronic capacitor [4]. The boost rectifier [1] is a highly efficient, low–cost, and relatively simple PFC stage with relatively high voltage output. Nonetheless, a typical DC load consumes energy under a certain (much lower) voltage

supply and consequently requires an additional conversion stage. As a result, the cost, volume, weight, and efficiency are negatively affected.

The conventional boost rectifier presents significant conduction losses because the current always flows through the switching devices. The converter should operate at high switching frequencies to achieve high power density and faster transient response. Nevertheless, the diode reverse–recovery losses become significant as the switching frequency rises and the electromagnetic interference increases. A bridgeless topology has been presented in [5] to overcome the conduction losses. The diode reverse–recovery problems are alleviated using only a coupled inductor and two additional diodes. As the rectifier power level increased, a parallel interleaved bridgeless boost converter [5] was employed to improve the performance and reduce the size. In such an operation, the active ripple frequency is twice the switching frequency or more; thus, the input and output ripples are minimized, and the output capacitance and the input filter sizes can be drastically reduced. In the half–bridge boost converter, the current flows through one switch during each operating stage, drastically reducing conduction losses. In this topology, the output voltage is doubled while keeping the component stress voltage at the same level as a standard converter.

The buck is a step–down converter that may solve the necessity for lower voltage applications. In this topology, the output voltage must be lower than the input source voltage. Thus, the buck rectifier cannot sustain continuous operation throughout the grid cycle [1]; the input current is discontinued when the instantaneous line voltage is lower than the output voltage. Therefore, it cannot maintain the required power factor and total harmonic distortion. Buck–type PFC rectifiers allow a more comprehensive control range for the output rectified voltage (corresponding to the boost–type topologies) [6]. Due to the operation's nature, the output–voltage regulation depends on the load impedance; therefore, a larger output filter is compulsory. A bridgeless buck topology has an improved performance over the standard buck converter as a high–power levels PFC converter [5]. It offers the same current flow with a reduced number of switching devices, hence reducing thermal stress. Moreover, it introduces a higher efficiency operation with reduced input current THD, cutting down the conduction losses and ensuring that the output voltage on the DC bus is naturally balanced. The interleaved buck topology [7] has advantages like the interleaved boost–type topology. The bridgeless interleaved topology is highly efficient (95–97%) from light to full–load at universal input voltage [8].

By contrast, the buck–boost rectifier is much more versatile since it supports a voltage step–up and step–down; consequently, a wide output–voltage range is available. Nevertheless, a buck–boost rectifier is relatively less efficient; the reversing output voltage can cause a conflict with the neutral point, and the inductor peak current is higher than in a similar power boost rectifier [1]. The bridgeless buck–boost topology is based on two basics single–switch buck–boost converters, each operating over a half–grid cycle [9]. It offers high power–quality performances with low THD_i and near unity power factor under a wide load range. The structure of bridgeless buck–boost topologies is complex and limited to low–power applications [10]. The bridgeless cascaded buck–boost topology presents a reduced number of conducted switches. It escalates the electromagnetic interference and increases the voltage sensing complexity, while the efficiency is higher than the standard topology (95–97%) at a wide load range and near unity power factor [11].

The penetration of stochastic renewable sources into the electrical grid [12] requires energy backup support utilized by storage systems. Batteries are among the most appropriate storage technologies due to their energy density, volumetric density, fast response time, availability, and installation simplicity near the power generation plant and at the distribution consumption location [13]. The energy storage charging process is controlled by power electronics circuitry; in the grid–connected applications, a near unity power factor within limits of total harmonic distortion standard is mandatory. This requires a significant amount of energy to be stored in a series cell structure, which creates a high–voltage battery.

As in electric vehicles (EVs), the battery voltage can swing above and below the standard rectified voltage; thus, a wide output–voltage range is required.

The Vienna rectifier introduced an innovative approach for three–phase rectifiers. Compared with a conventional two–level converter system, the three–level Vienna rectifier reduces the voltage stress on its switches and the rated power of inductance connected on the side of the mains. The three–level DC bus is more applicable for inverters since the three–level inverter enables higher efficiencies and better harmonics immunity compared with two–level inverters [14]. However, the Vienna rectifier's output voltage is twice as high as a standard boost PFC rectifier with bus voltages of ~–400 V, neutral (0 V), and ~+400 V. This rectifier type may fit applications such as low harmonics three–level inverters and high–voltage, high–power motor drives. Applications with low–power motors, such as air–conditioners, refrigerators, etc., may require lower amplitude sine waves, where the high–voltage three–level DC bus reduces the resolution; therefore, the accuracy of the inverter may also harm the inverter's efficiency. In such a case, an additional conversion step is the preferred option for decreasing the DC bus voltage. The emergence of fully EVs and hybrid plug–in vehicles brought new challenges for power electronics engineers and pushed the battery energy density limits to new levels; although optimization of battery size was made [15], the battery capacity remains over tens of kilo watts hours, and requires powerful, fast chargers [16] or powerful wireless chargers [17]. The nominal charging voltage in EV applications varies between 100 V and 1000 V [18]. Thus, the available rectifiers cannot support universal charging in a single conversion step. A comprehensive output–voltage range [19] could be achieved by utilizing an additional conversion step; however, the overall efficiency is negatively affected. Moreover, the system cost, volume, weight, and component failure rate increase when employing two–stage conversion. The contribution of this paper compared to [20,21] is as follows. Unlike [20,21], where the rectifier runs in open–loop mode, a dual–loop controller (for the inductor current and output voltage) is implemented here:

- Experimental results are given in this paper ([20,21] has only simulation); it was shown that some of the results reported in [20,21] are unachievable because of practical driving limitations.
- Elaboration on the optional utilization of the bi–directional switch and the analysis of the required control command for each case.
- The average current mode control method for discontinuous–conduction mode (DCM) operation is implemented here.

This paper presents a new topology for a single–step universal three–level PFC rectifier (UTPR) operating in dual–loop mode. The output–voltage range can swing between 50 V and 900 V while keeping the UTPR elements at half the size of a standard buck–boost rectifier. Unlike standard buck–boost, the UTPR creates three output–voltage levels that directly fit three–level inverters for improved voltage total harmonic distortion (THD$_V$). The UTPR employs fewer components than a standard dual–step converter. Therefore, the UTPR overall efficiency is higher, and the component count is lower than in a similar traditional system. The UTPR is relevant to applications such as EVs [22], battery storage systems [12], inverters [23] or multi–level inverters [24], and front–end rectifiers [25]. First, the principles of operation and circuit analytics are introduced. Then, the UTPR average model and control approach is presented. Next, the UTPR circuit (operating in DCM) simulation and experimental results are provided, demonstrating the proposed circuit performance in a multiplier–less dual loop and validating the proposed theory of the innovative topology. Then, the results and outcome are discussed, and the conclusion is provided.

2. Circuit Topology and Analysis

In the meaning of the broad input and output–voltage range of a three–level PFC rectifier, the UTPR can fulfill all required properties. The proposed rectifier can operate in a single phase for light to medium loads or as a three–phase topology for high–power loads.

The single–phase UTPR is based on one power inductor (L), two storage capacitors (C), and three bi–directional switches (SW), as presented in Figure 1. The UTPR can operate in continuous–conduction mode (CCM) [26] and DCM [27].
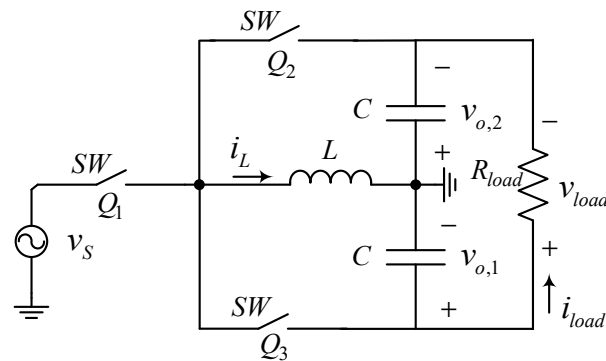

Figure 1. UTPR circuit.

Several methods could be employed for a bi–directional SW. The most straightforward technique for AC–connected SWs is by four diodes and a single transistor (MOSFET, GaN FET, SiC, or IGBT). The diodes are connected in a rectifying fashion where the transistor drain is attached to the common cathode and the source to the common anode, as exhibited in Figure 2a. Another option is a series connection of two transistors with a common source or drain connection, as presented in Figures 2b and 2c, respectively. In many applications, the switching timing sequence is crucial; consequently, particular logic circuitry or high computational switching effort is required. A possible solution is a semi–open bidirectional SW, where the opposing flow transistor is turned on before the inductor current is "looking" for a possible path; the second transistor anti–parallel diode blocks the unwanted flow. Next, when the inductor voltage reverses, the diode polarity turns ON and conducts (the SW is ON now). To reduce the losses, the active diode transistor can be turned ON. The same results could be achieved by a semi–open SW, where a drain of the transistor is series connected with the diode anode, as given in Figure 2d. The drawback of this switch is the unidirectional current flow; thus, its utilization is limited to specific cases.
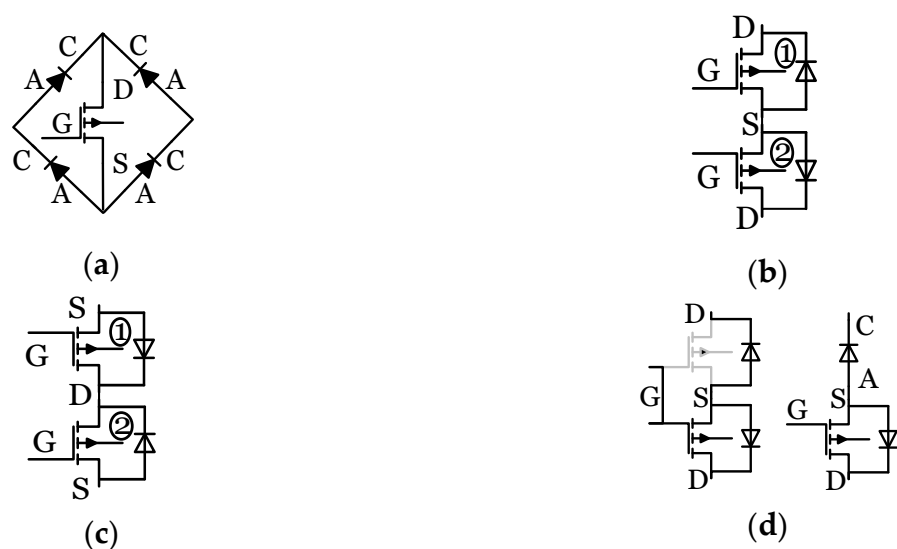

Figure 2. Implementation of the bidirectional SW: (**a**) four diodes and one transistor; (**b**) common source, two transistors; (**c**) common drain, two transistors; (**d**) semi–active transistor and diode.

The principle of operation for the positive half–sine wave includes a charging period and a discharging interval of the power inductor. The charge path (marked in Figure 3 as (a)) begins at the AC source throughout the main *SW* (Q_1 at the middle), goes to the power inductor, and goes back to the neutral, as presented in Figure 3a. The discharge path (marked as (b)) at the positive half–sine wave continues with the same current direction, discharging the inductor throughout the upper capacitor and the top *SW* (Q_2). In the discharge period, the upper capacitor is charged within the current flow direction, as marked in Figure 3b. The logic signals for driving the *SW*s are as follows: the main *SW* (Q_1) is governed by the PWM signal, and the upper SW (Q_2) is ruled by the complementary PWM signal with the condition of operating in the sine positive half–wave $\overline{PWM}\&sign(v_S(t))$.
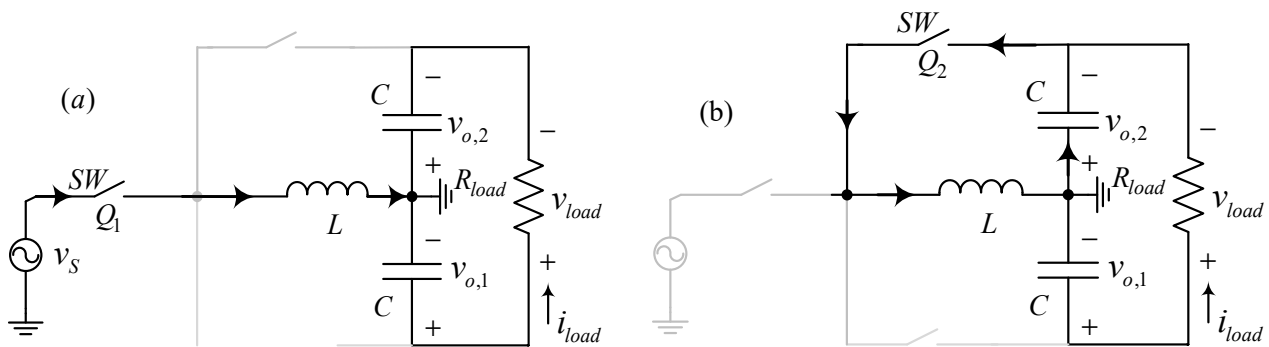
Figure 3. The UTPR operates at grid positive half–sine wave for an inductor: (**a**) charging path and (**b**) discharging path.

In the negative half–sine wave, the charge path (marked in Figure 4 as (a)) begins at the neutral and goes through the power inductor, to the main *SW* (Q_1), and back to the AC source, as exhibited in Figure 4a. The discharge path (marked in Figure 4 as (b)) continues in the same direction as the current flow, discharging the inductor's stored energy through the bottom capacitor and the lower *SW* (Q_3). The bottom capacitor is charged within the current flow direction, as marked in Figure 4b. The logic signals for driving the *SW*s are as follows: the PWM signal governs the main *SW* (Q_1), the bottom *SW* (Q_3) is controlled by the complementary PWM signal with the condition of operating in the sine negative half–wave $\overline{PWM}\&\overline{sign(v_S(t))}$.
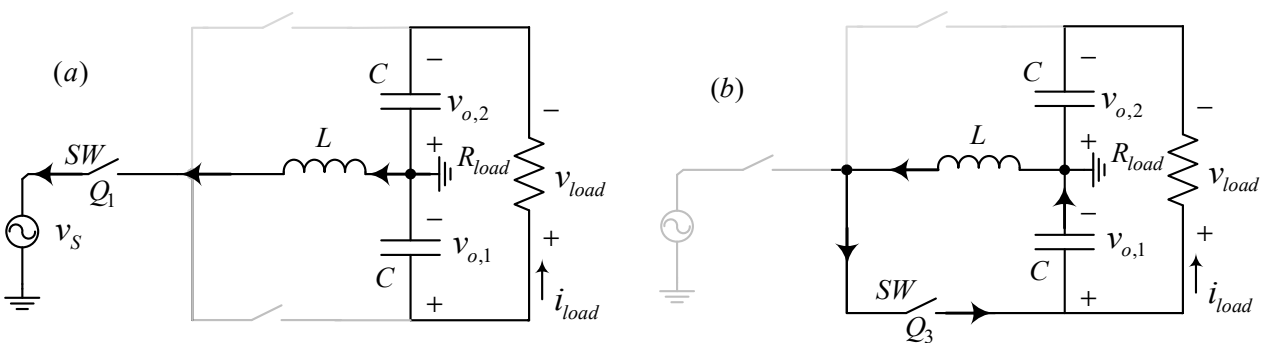
Figure 4. The UTPR operates at grid negative half–sine wave for an inductor: (**a**) charging path and (**b**) discharging path.

The analysis of UTPR is made for two operation modes, the CCM and the DCM. In CCM, the UTPR output voltage is in three–level mode, and the converter voltage gain is

$$v_{o,avg}/v_{S,rms} = -d_{rms}/(2\cdot(1-d_{rms})) \tag{1}$$

where $v_{S,rms}$ is the input terminal connected to the electrical grid r.m.s voltage ($v_S(t) = V_m sin(\omega t)$), the $2 \cdot v_{o,avg}$ is the load voltage (where $v_{load,avg} = v_{o,1,avg} + v_{o,2,avg} = 2 \cdot v_{o,avg}$), and the d_{rms} is the rectifier's duty cycle for *r.m.s* values. The inductor's current ripple is derived from the inductor voltage balance equation and from Equation (1), where the current ripple is

$$\Delta i_L = (v_{S,rms}/(L \cdot f_{sw})) \cdot 2 \cdot v_{o,avg}/(2 \cdot v_{o,avg} + v_{S,rms}) \tag{2}$$

where L is the inductance of the power inductor, and f_{SW} is the switching frequency. Thus, the average inductor current is

$$\langle i_L \rangle_T = 2 \cdot v_{o,avg} \cdot i_{load,avg}/(d_{rms} \cdot v_{S,rms}) \tag{3}$$

where $i_{load,avg}$ is the load average current ($i_{load,avg} \cong i_{load,rms}$). Therefore, the inductor peak current is

$$i_{L,m} = 2v_{o,avg} \cdot \left(\frac{i_{load,avg}}{d_{rms} \cdot v_{S,rms}} + \frac{v_{S,rms}}{L \cdot f_{sw} \cdot (2v_{o,avg} + v_{S,rms})} \right) \tag{4}$$

and the minimum inductor for CCM is

$$L_{crit} = (v_{S,rms} \cdot d_{rms})^2/(4 \cdot f_{sw} \cdot P_{load}) \tag{5}$$

where L_{crit} Is the inductor value of critical mode, and P_{load} is the average output load power. As for DCM, since the UTPR shares similar characteristics as the buck–boost converter, the input average current exhibits a perfect linear relationship with its input voltage given by

$$i_L = 4P_{load}/(v_{S,rms} \cdot d_{1,rms}) \tag{6}$$

where $d_{1,rms}$ is the inductor's duty cycle for the conduction interval when operating at DCM for the *r.m.s* values. From power equality and Equation (6), the converter transfer function is revealed in Equation (7), where the DCM duty cycle (d_1) can be revealed.

$$v_{o,avg}/v_{S,rms} = -\left(d_{1,rms}/i_{load,avg} \right) \cdot \sqrt{P_{load}/(2 \cdot L \cdot f_{sw})} \tag{7}$$

In standard rectifiers, under the assumption of unity power factor, the output capacitor value is set by the following rules of power equality, where $p_S(t)$ is the instantaneous input power, and $p_C(t)$ is the instantaneous capacitor power:

$$p_s(t) = P_{load} + p_c(t) = P_{load} \cdot \frac{1}{2}(1 + cos(2\omega t)) \tag{8}$$

The capacitor energy balance is derived from Equation (8)

$$E_c = E_0 - P_{load}|sin(2\omega t)|/(2\omega) \tag{9}$$

From Equation (9), the capacitor value is revealed as

$$C_{ripple} = P_{load}/(4 \cdot \omega \cdot \Delta v_o \cdot v_{o,avg}) \tag{10}$$

where C_{ripple} is the rectifier output filter capacitor and Δv_o is the capacitor voltage ripple. Nevertheless, the UTPR operating principle resembles a single–phase Vienna rectifier [26]. Each capacitor on UTPR is charged only in a one–half cycle and supplies energy for a whole period, as presented in Figures 3 and 4. Both capacitors must contain a hold–up energy for a half–cycle time to fulfill the energy requirements, as shown in Equation (11).

$$C_{h.up} = \pi \cdot P_{load}/(4 \cdot \omega \cdot \Delta v_o \cdot v_o) \tag{11}$$

where $C_{h.up}$ is the capacitor hold–up time. Thus, an increased output capacitance is mandatory to support the required output–voltage ripple when employing a three–level rectifier. Applying a proportional integral and notch voltage controller decreases output capacitance, as presented in [28]. The output capacitor is set by the maximum value of Equations (10) and (11)

$$C = max\left\{C_{ripple}, \; C_{h.up}\right\} \tag{12}$$

It is easy to obtain that the hold–up capacitor is more significant than the ripple capacitor $\left(C_{h.up} \gg C_{ripple}\right)$; hence, the output capacitors are set by the $C_{h.up}$ value. Since a half–cycle energy hold–up time is a standardization requirement for every grid–connected system at a specific power rating, the capacity of UTPR is equal to any other rectifier topology. In the case of a three–phase rectifier, the low–frequency power signals are shifted at $120°$, and the summation of all three voltage components is near zero ripple; hence, the required output capacitance is much lower than in a single phase.

3. Average Model and Control Approach

A cascade dual–control loop [29] is a standard methodology to tackle converter stabilization tasks [30]. An internal loop to shape the inductor current for PFC properties creates a sinusoidal envelope shape and an external outer voltage loop for the rectifier output–voltage adjustment, as presented in Figure 5. The rectifier output voltage contains a slight sinusoidal fluctuation at double–line frequency; therefore, the controller output command (i_{ref}) is a DC signal. However, the required current shape in the line frequency is sinusoidal; thus, an analog multiplier is necessary, as presented in Figure 5.
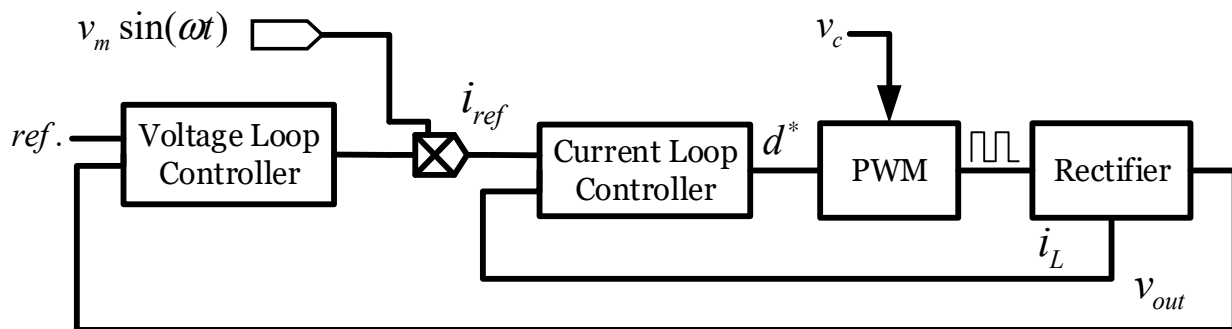
Figure 5. Standard rectifier control scheme. d^*: the reference command for the duty cycle.

Where d^* is the reference command for the duty cycle. The converter state equations present a non–linear system that is uncontrollable. The standard method to tackle this issue is modeling the converter's continuous form as an average model. It is important to note that this model describes each half–sine wave separately; however, since the overall circuit activity is the same, both circuits are presented as a single model in Figure 6. On the input side, the input voltage is marked as v_S, the r_S reflects the output active load multiplied by the operating–point duty ratio divided by the square of the output–to–input voltage–transfer function, and the last element is the average input current ($\left\langle \tilde{i}_S \right\rangle_T$) multiply by the operating–point duty ratio. The output side is affected by the input voltage multiplied by the output–to–input voltage–transfer function divided by the output active load, and the next element is the average input current multiplied by the operating–point duty ratio; the other elements are the state operating capacitor (C_X) according to the positive or negative sequence, and the output active load. A small signal state equation is accomplished by applying Kirchhoff's voltages and currents laws on the UPTR average model and splitting the parameters into intermediate components and perturbations. The state equations can

be constructed by applying Kirchhoff's voltages and currents laws on the UPTR average model and separating the parameters into average components and perturbations.
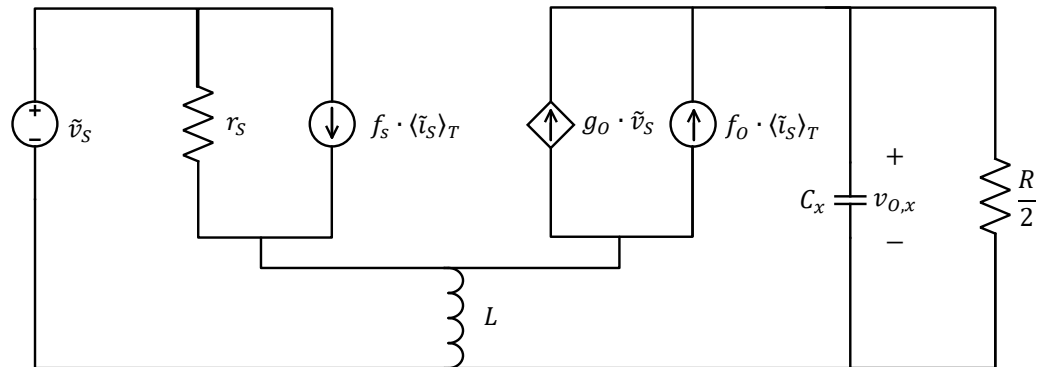

Figure 6. UPTR average model.

When operating the UTPR in DCM, the input current is a function of the input voltage and other parameters; thus, a near–unity PF is achieved naturally. Since the switching frequency has been higher than the line frequency for several decades, the line voltage is assumed to be almost constant in a single switching cycle. Under the steady–state operation assumption, the output voltage, and the duty ratio variation are slight. By performing an analysis on the UTPR, the line average current and the voltage present a perfect linear relationship, which proves that the UTPR has excellent self–PFC properties, as given in Equation (13) [31]. Consequently, the UTPR control schematics do not necessitate a multiplier, simplifying the control effort (analog or digital) and reducing the control circuitry cost.

$$\langle i_S(t)\rangle_T = \left(d_1{}^2 T_s \langle v_S(t)\rangle_T\right)/(2L) \tag{13}$$

The state equations can be constructed by applying Kirchhoff's voltages and currents laws on the UTPR. However, these state equations produce an uncontrollable non–linear system (with common compensators). The standard method to tackle this issue is transferring the converter's continuous form using an average model. Separating the average model parameters into DC components, intermediate (first–order) components, and perturbations (second–order) yields the inductor state equation, as shown in Equation (14). The plant is dismantled into coefficients utilized for system input parameters. The functional block diagram includes the transfer function of the inductor current to the duty–cycle input signal (G_{id}), where the input–voltage vector is set to zero.

$$\tilde{i}_L(s) = \left(\frac{(I_s - I_o)\left(\left(\frac{V_s}{L} - \frac{1}{T_s}\right)\cdot T_s + 1\right) + 2I_o}{\left(\frac{V_s}{L} - \frac{1}{T_s}\right)\cdot T_s d_1(2I_s - I_o)}\cdot\left(2(I_s - I_o) + I_o\frac{1}{\left(1 + s\frac{CR}{2}\right)}\right)\right)\tilde{d}(s) \tag{14}$$

where the I_s and the I_o are the rms input and output current, respectively, V_s is the rms input voltage, L is the inductor value, T_s is the switching cycle period, d_1 is the duty cycle (ON time), C is the capacitor value, and R is the load resistance (ohmic). The UTPR output–voltage state equation is revealed in Equation (15). It is important to note that the output of the voltage controller is not multiplied by the absolute value of the sinusoidal waveform as in the standard rectifiers.

$$\tilde{v}(s) = \left(\frac{I_o R}{\left(\frac{I_s V_s T_s}{V_s T_s - L} - I_o\right)}\cdot\frac{1}{\left(1 + s\frac{CR(I_s - I_o)}{(2I_s - I_o)}\right)}\right)\tilde{v}_c(s) + \frac{\frac{I_o}{d_1}R}{\left(1 + s\frac{CR}{2}\right)}\tilde{v}_s(s) \tag{15}$$

The state equation includes the UTPR output–voltage transfer function to the inductor current reference input signal (G_{vc}), where the input–voltage vector is set to zero, and the

input state vector coefficient (G_{vs}), where the input reference voltage vector is set to zero. Unlike a standard rectifier, the control scheme does not require a multiplier, as presented in Figure 7, where the $G_{cv}(s)$ is the voltage loop compensator and the $G_{ci}(s)$ is the current loop compensator.
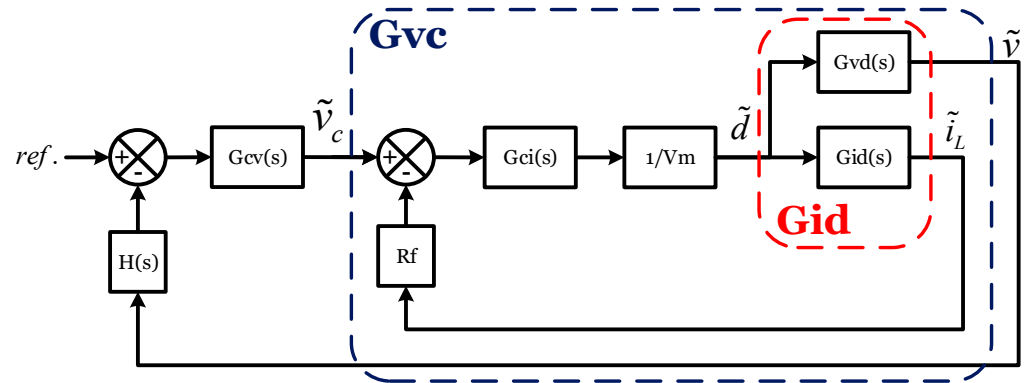

Figure 7. Dual–loop UTPR average model block diagram control scheme.

4. Simulation and Experimental Results

Based on the above analysis, the proposed UTPR circuit parameters were designed for multiplier–less dual–loop conditions at DCM. A DELL OPTIPLEX 7060 PC made the simulation with the PSIM tool (PSIM Professional 2022.2.0.17) operating at a switching frequency of $f_{sw} = 100$ kHz. The input voltage was set to $V_s = 230$ Vrms. In the design of the UTPR power inductor, the circuit output load was put into two conversion modes: step–up and step–down. At buck operation, the output load was set to 430 ohms ($R = 430\ \Omega$) and the output load voltage to 75 volts ($V_{load} = 75$ V). At the boost mode, the output load was set to 4000 ohms ($R = 4$ kΩ) and the output load voltage to 400 volts ($V_o = 400$ V). By employing Equation (5), the minimal critical inductance was found to be $L_{critical} = 498\ \mu$H; thus, the actual inductance was determined to be $L = 120\ \mu$H. The output ripple voltage was set to 5%; according to Equation (12), the output capacitors were set to $C = 470\ \mu$F (each) to satisfy the required output ripple voltage and the hold–up demand. Applying Equation (7), the duty ratio is revealed where $d_{1,buck} = 0.2$ for the buck mode and $d_{1,boost} = 0.51$ for the boost mode. The current control loop bandwidth was set to one decade below the switching frequency (10 kHz) and the voltage to one decade below the line frequency (5 Hz). The controllers' coefficients were determined by assuming a nominal input voltage of 230 V, an output capacitor voltage of 275 V, and a load of 2.2 kilo ohm. The integration coefficient was found to be $ki = 314.5$. Under the assumption of a damping coefficient in a near–critical point with a value of 0.8, the proportional coefficient value is $kp = 0.83$. The voltage loop PI controller integration coefficient is $ki = 112.6$, and with a dumping constant of 0.8, the proportional coefficient is $kp = 0.066$. Based on the above analysis, the proposed UTPR prototype parameters were designed for operation at DCM with the same values as in the simulation. The switching frequency was set to $f_{sw} = 100$ kHz, a resistive load of $R = 0.43$ kΩ, 4 kΩ. The revealed inductor from Equation (5) is $L = 120\ \mu$H, and by Equation (14), the output capacitor was set to $C = 470\ \mu$F. The circuit was fed by the California Instruments 751i AC Power Supply. The Texas Instruments C2000 Delfino MCU F28379D LaunchPad™ governed the UTPR. The MCU measured the line voltage and synchronized all required logic signals to drive the UTPR switches. The UTPR main $SW\ Q_1$ was utilized by the combination of Transphorm 950 V/15 A TP90H180PS GaN FET and the supporting four blocking Schottky diodes of ONSEMI 1.2 kV/10 A, the FFSP10120A in fashion as in Figure 2a. The upper switch Q_2 and lower switch Q_3 were utilized with the same devices in style shown in Figure 2d, as given in Table 1. The UTPR experimental board is presented in Figure 8.

Table 1. Parameters set employed in the test.

| Parameter	Description
RMS input voltage	230 Vrms
Line frequency	50 Hz
Switching frequency	100 kHz
Inductor Value	120 µH
Output capacitor C_1 and C_2	470 µF
R load	430 Ω, 4 kΩ
Main switch Q_1	One (1) GaN FET TP90H180PS 950 V/15 A and four (4) Schottky diode FFSP10120A 1.2 kV/10 A
Upper switch Q_2	One (1) GaN FET TP90H180PS 950 V/15 A and one (1) Schottky diode FFSP10120A 1.2 kV/10 A
Lower switch Q_3	One (1) GaN FET TP90H180PS 950 V/15 A and one (1) Schottky diode FFSP10120A 1.2 kV/10 A
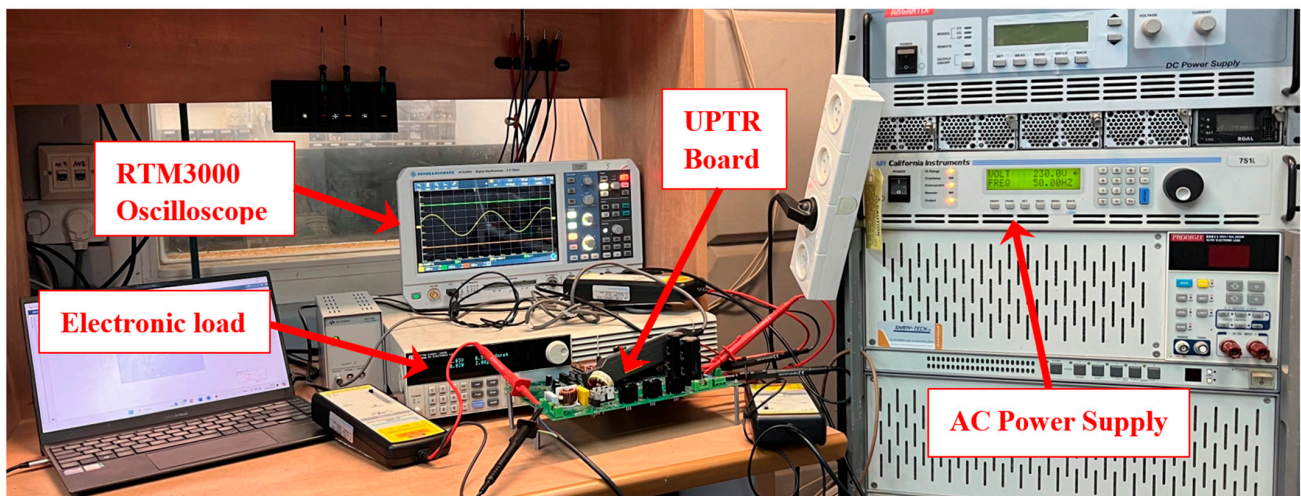
Figure 8. Experimental UTPR board and experimental setup.

The UTPR was designed for DCM operation when its control system operates in a multiplier–less dual loop; the reference signal was set according to Equation (7). Measurements were carried out with a 200 MHz Rohde & Schwarz RTM3000 oscilloscope equipped with a power analysis tool. The command signals for the switches were set as mentioned above; the main switch (Q_1) receives the *PWM* signal, the upper switch (Q_2) is active during the positive line cycle and, therefore, receives the $\overline{PWM}\&sign(v_S(t))$, and the lower switch ($Q_3$) is active at the negative line sequence and acquire $\overline{PWM}\&sign(v_S(t))$. The command signals for all switches are presented in Figure 9.
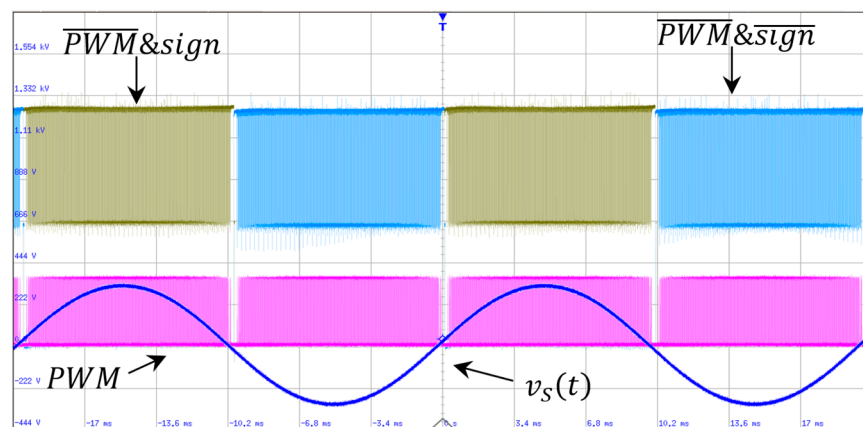

Figure 9. Experimental signal commands for all switches.

The UTPR principle of operation is similar to that of all switch–mode power supplies, where the inductor is charged during ON time. It delivers the accumulated energy to the output capacitor and the load during the discharge time, as explicit in Figure 10. The specific frame was taken during the positive line sequence where the inductor current is positive, and the output capacitor voltage is negative concerning the line neutral.
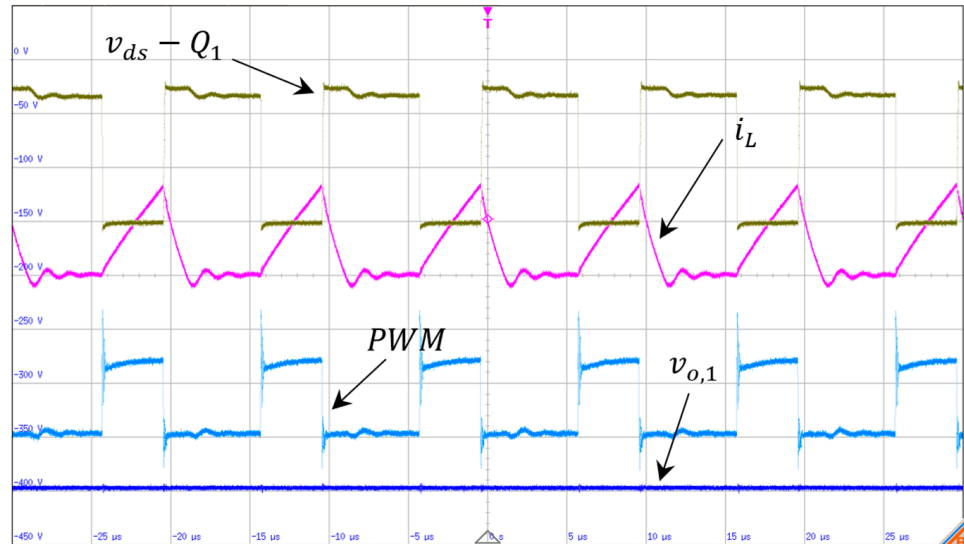
Figure 10. Experimental UTPR results of the inductor current, main switch (Q_1) voltage, PWM signal, and upper capacitor ($v_{o,1}$) voltage.

In the boost mode, experimental results display an input voltage of $V_s = 230$ Vrms, an output capacitor voltage of $v_o = 400$ V, and a load voltage of $v_{load} = 800$ V, as shown in Figure 11a. In buck mode, under the same grid supply voltage, the output voltage was $v_o = 37.5$ V, and the load voltage was $v_{load} = 75$ V. In both cases, the inductor current envelope allows the input–voltage shape, as shown in Figure 11b. The power factor is near unity ($PF = 0.97$), as indicated in Figure 11c. Although the UTPR runs at a multiplier–less dual loop, the inductor current shape is sinusoidal, an inherent feature of the buck–boost converter.
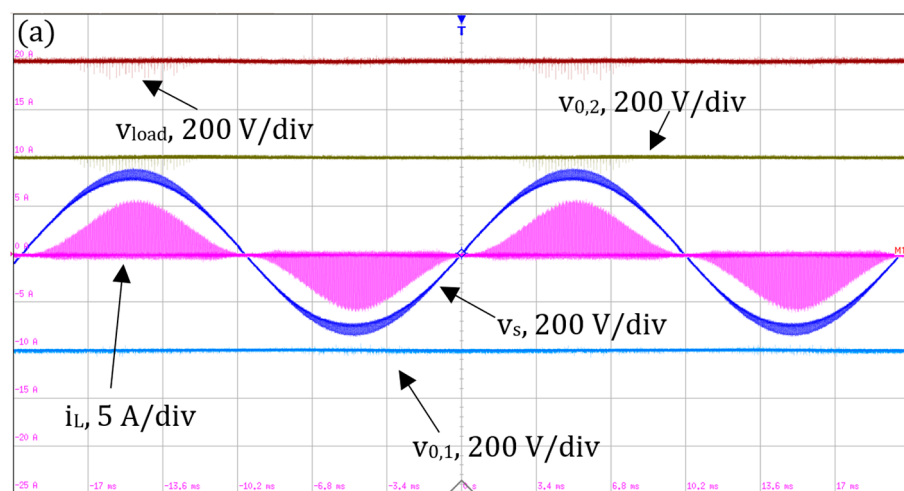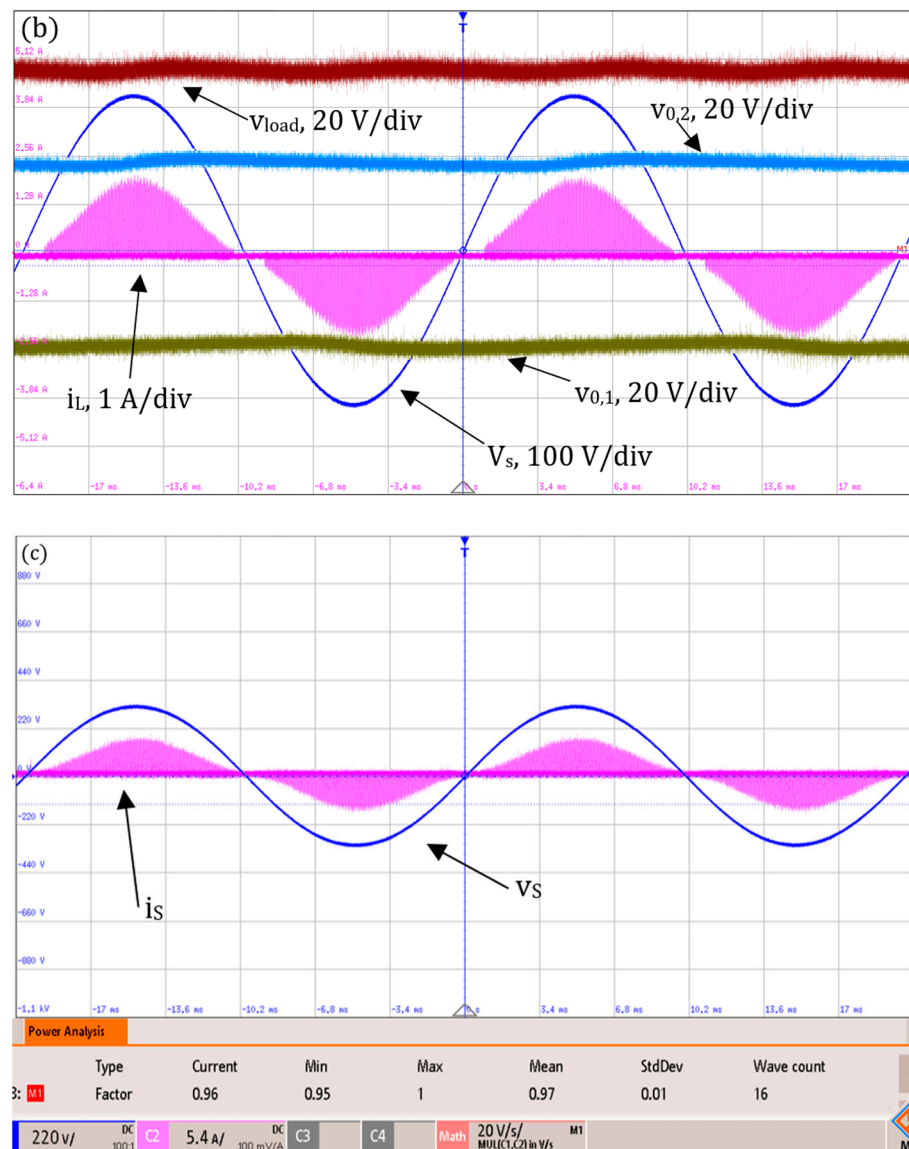

Figure 11. *Cont.*

Figure 11. Experimental results for DCM in (**a**) boost mode, (**b**) buck mode, and (**c**) power factor.

5. Discussion

The simulation and experimental results show that when operating in DCM, the UTPR can operate at a wide range in boost and buck modes. Although the control loop does not contain a multiplier, the rectifier input current envelope is aligned with the input–voltage phase, presenting a self–PFC. The results acknowledge the validity of the proposed theory, the developed analytics, and the UTPR average model. When comparing the proposed rectifier to a standard dual–stage rectifier, the component count for this topology for a single phase is one inductor, two capacitors, three MOSFETs, six diodes, and one dual–loop controller. A standard dual–stage rectifier has two inductors, two capacitors, two MOSFETs, six diodes, and two dual–loop controllers. The UTPR employs one more switch, one less power inductor, and one less dual–loop controller than a standard dual–stage rectifier. The efficiency of UPTR is expected to be higher than that of a standard dual–stage rectifier since it utilizes a single conversion step.

Bidirectional SW has multiple implementation methods; each topology's component count, conduction losses, and static losses differ. The main *SW* (Q_1—connected to the source v_S) could be implemented by the *SW*s from Figure 2a, Figure 2b, or Figure 2c (but not by Figure 2d). The static and dynamic losses and the control instructions for each case

are presented in Table 2. The upper and lower *SW*s (Q_2 and Q_3, respectively) are suitable for use by all *SW*s, as shown in Figure 2. The static and dynamic losses, alongside the control instructions for each case, are presented in Table 2.

Table 2. Control signals for different types of bidirectional *SW* utilization and losses per each case.

Figure #	Implemented Switches	Conduction Losses	Switching Losses	Command Q_1	Command Q_2	Command Q_3
Figure 2a	One Transistor Four Diodes	$I_{rms}r_{ds} + I_{avg}2V_D$	$Q_G V_G f_{SW}$	PWM	$\overline{PWM}\&sign(v_S(t))$	$\overline{PWM}\&\overline{sign(v_S(t))}$
Figure 2b	Two Transistors	$2I_{rms}r_{ds}$	$2Q_G V_G f_{SW}$	PWM	$\overline{PWM}\&sign(v_S(t))^{(2)}$ Or $\overline{PWM}\&sign(v_S(t))^{(2)}$ $\overline{PWM(-)}\&sign(v_S(t))^{(1)}$	$\overline{PWM}\&sign(v_S(t))^{(1)}$ Or $\overline{PWM}\&sign(v_S(t))^{(1)}$ $\overline{PWM(-)}\&sign(v_S(t))^{(2)}$
Figure 2c	Two Transistors	$2I_{rms}r_{ds}$	$2Q_G V_G f_{SW}$	PWM	$\overline{PWM}\&sign(v_S(t))^{(1)}$ Or $\overline{PWM}\&sign(v_S(t))^{(1)}$ $\overline{PWM(-)}\&sign(v_S(t))^{(2)}$	$\overline{PWM}\&sign(v_S(t))^{(2)}$ Or $\overline{PWM}\&sign(v_S(t))^{(2)}$ $\overline{PWM(-)}\&sign(v_S(t))^{(1)}$
Figure 2d	Two Transistors Or One Transistor + One Diode	$I_{rms}r_{ds} + I_{avg}V_D$	$Q_G V_G f_{SW}$	Not Applicative	$\overline{PWM}\&sign(v_S(t))$	$\overline{PWM}\&\overline{sign(v_S(t))}$

[Numbers] Transistor number (#) in Figure 2b,c; ($-$)—is the PWM signal with a short delay to allow the antiparallel diode to start the conduction phase.

One of the drawbacks of the UTPR operating in a single phase is the high–value output capacitance. As in the Vienna rectifier, each output capacitor is not charged during one–half of the line cycle. Moreover, since the inductor in the UTPR is not constantly connected to the input or the output, the peak current is higher than in step–down rectifiers. Future work on the subject will be implementing the dual–loop controller for DCM and CCM at a single–phase rectifier and then into a three–phase interleaved rectifier where the circuit dynamics will be analyzed. When implementing a three–phase rectifier, the output capacitance could be minimized to near zero. A parallel interleaving approach is sufficient to decrease the inductor peak current.

6. Conclusions

This paper presents a new rectifier topology inherited from the buck–boost converter. The UTPR is a single–step universal rectifier; thus, it supports a wide output–voltage range while reducing the component count, cost, volume, and weight. The output voltage can apply a two–voltage level for two terminal loads or a voltage level for low–harmonic–distortion loads. The principle of operation is demonstrated in dual–loop mode. It was shown that the UTPR prototype could step up or down while maintaining near–unity performance. This unique feature may ease the control computational effort since there is no need for a multiplier in the control circuitry when operating in DCM. The UTPR output voltage is suitable for employing a standard load or feeding three–level voltage loads. The proposed topology could correspond to many applications, especially for commercial low–voltage or high–voltage DC loads, storage applications, EVs, and three–level inverters.

7. Patents

This work is based on the international application Patent Cooperation Treaty WO2022190097 A1 of 15 September 2022.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding authors.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

AC	Alternating current
$C_{h.up}$	Hold–up capacitor value
C_{ripple}	Required capacitor value for setting the desired output ripple
CCM	Continuous–conduction mode
d	Duty cycle
DC	Direct current
DCM	Discontinuous–conduction mode
E_c	Capacitor's stored energy
E_o	Load consumed energy
EVs	Electric vehicles
f_{sw}	Switching frequency
FET	Field–effect transistor
GaN	Gallium nitride
i_L	Inductor current
i_{ref}	The reference signal for the inductor current control loop
i_s	Rectifier input current
IGBT	Insulated–gate bipolar transistor
MCU	Microcontroller unit
MOSFET	Metal–oxide–semiconductor field–effect transistor
p_c	Momentary capacitor power
p_s	Supplied grid power
p_{load}	Load power
PFC	Power–factor correction
SWs	Switches
THD_V	Voltage total harmonic distortion
UTPR	Universal three–level PFC rectifier
$v_{o,x}$	Rectifier positive or negative output voltage
v_{load}	Rectifier load output voltage
v_s	Rectifier input voltage

References

1. Wei, H.; Batarseh, I. Comparison of basic converter topologies for power factor correction. In Proceedings of the IEEE Southeastcon '98 'Engineering for a New Era', Orlando, FL, USA, 24–26 April 1998; pp. 348–353.
2. Siton, Y.; Sitbon, M.; Aharon, I.; Lineykin, S.; Baimel, D.; Kuperman, A. On the Minimum Value of Split DC Link Capacitances in Three-Phase Three-Level Grid-Connected Converters Operating with Unity Power Factor with Limited Zero-Sequence Injection. *Electronics* **2023**, *12*, 1994. [CrossRef]
3. Amar, N.; Ziv, A.; Strajnikov, P.; Kuperman, A.; Aharon, I. Topological Overview of Auxiliary Source Circuits for Grid-Tied Converters. *Machines* **2023**, *11*, 171. [CrossRef]
4. Strajnikov, P.; Amar, N.; Yuhimenko, V.; Aharon, I.; Kuperman, A. Design Constraints Generalization for Series-Stacked Buffer based Active DC Links. *IEEE Trans. Ind. Electron.* **2023**, *71*, 2133–2136. [CrossRef]
5. Chen, Z.; Xu, J.; Liu, X.; Davari, P.; Wang, P. High Power Factor Bridgeless Integrated Buck-Type PFC Converter With Wide Output Voltage Range. *IEEE Trans. Power Electron.* **2022**, *37*, 12577–12590. [CrossRef]
6. Jain, A.; Gupta, K.K.; Jain, S.K.; Bhatnagar, P. A Bidirectional Five-Level Buck PFC Rectifier With Wide Output Range for EV Charging Application. *IEEE Trans. Power Electron.* **2022**, *37*, 13439–13455. [CrossRef]
7. Choi, H. Interleaved Boundary Conduction Mode (BCM) Buck Power Factor Correction (PFC) Converter. *IEEE Trans. Power Electron.* **2013**, *28*, 2629–2634. [CrossRef]
8. Liu, Y.-C.; Pan, T.-F.; Tseng, P.-J.; Huang, C.-C.; Lo, Y.-K.; Chiu, H.-J. Study and implementation of a two-phase interleaved bridgeless buck power factor corrector. In Proceedings of the 2013 1st International Future Energy Electronics Conference (IFEEC), Tainan, Taiwan, 3–6 November 2013; pp. 42–47.
9. Kushwaha, R.; Singh, B. An Improved Battery Charger for Electric Vehicle with High Power Factor. In Proceedings of the 2018 IEEE Industry Applications Society Annual Meeting (IAS), Portland, OR, USA, 23–27 September 2018; pp. 1–8.

10. Zhao, B.; Abramovitz, A.; Smedley, K. Family of Bridgeless Buck-Boost PFC Rectifiers. *IEEE Trans. Power Electron.* **2015**, *30*, 6524–6527. [CrossRef]

11. Wang, W.; Liu, H.; Jiang, S.; Xu, D. A novel bridgeless buck-boost PFC converter. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 1304–1308.

12. Aharon, I.; Shmaryahu, A.; Sitbon, M.; Dagan, K.J.; Baimel, D.; Amar, N. Premeditated generic energy storage model for sources rating selection in grid applications. *Int. J. Electr. Power Energy Syst.* **2024**, *157*, 109837. Available online: https://www.sciencedirect.com/science/article/pii/S0142061524000589 (accessed on 15 March 2024). [CrossRef]

13. Hinz, H. Comparison of Lithium-Ion Battery Models for Simulating Storage Systems in Distributed Power Generation. *Inventions* **2019**, *4*, 41. [CrossRef]

14. Schweizer, M.; Friedli, T.; Kolar, J.W. Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems. *IEEE Trans. Ind. Electron.* **2013**, *60*, 5515–5527. [CrossRef]

15. Aharon, I.; Shmaryahu, A.; Ivanov, A.; Amar, N. Optimal sources rating of electric vehicle based on generic battery storage system model. *J. Energy Storage* **2023**, *72*, 108668. Available online: https://www.sciencedirect.com/science/article/pii/S2352152X23020650 (accessed on 15 March 2024). [CrossRef]

16. Bridgelall, R. Classifying Invention Objectives of Electric Vehicle Chargers through Natural Language Processing and Machine Learning. *Inventions* **2023**, *8*, 149. [CrossRef]

17. Ponce-Silva, M.; García-García, A.R.; Arau, J.; Lara-Reyes, J.; Cortés-García, C. Inductive Compensation of an Open-Loop IPT Circuit: Analysis and Design. *Inventions* **2023**, *8*, 104. [CrossRef]

18. Pradhan, R.; Keshmiri, N.; Emadi, A. On-Board Chargers for High-Voltage Electric Vehicle Powertrains: Future Trends and Challenges. *IEEE Open J. Power Electron.* **2023**, *4*, 189–207. [CrossRef]

19. Karneddi, H.; Ronanki, D. Reconfigurable Battery Charger With a Wide Voltage Range for Universal Electric Vehicle Charging Applications. *IEEE Trans. Power Electron.* **2023**, *38*, 10606–10610. [CrossRef]

20. Dahan, E.; Oren, Y.; Shmaryahu, A.; Aharon, I. T-type Buck-Boost PFC Rectifier in Continuous Conduction Mode. In Proceedings of the 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 20–23 June 2022; pp. 1–5.

21. Oren, Y.; Shmaryahu, A.; Dahan, E.; Aharon, I. T-type Buck-Boost PFC Rectifier in Discontinuous Conduction Mode. In Proceedings of the 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 20–23 June 2022; pp. 1–6.

22. Kim, J.-Y.; Lee, B.-S.; Kwon, D.-H.; Lee, D.-W.; Kim, J.-K. Low Voltage Charging Technique for Electric Vehicles With 800 V Battery. *IEEE Trans. Ind. Electron.* **2022**, *69*, 7890–7896. [CrossRef]

23. Khan, M.; Khan, M.; Jiang, H.; Hashmi, K.; Shahid, M.U. An Improved Control Strategy for Three-Phase Power Inverters in Islanded AC Microgrids. *Inventions* **2018**, *3*, 47. [CrossRef]

24. Omer, P.; Kumar, J.; Surjan, B.S. A Review on Reduced Switch Count Multilevel Inverter Topologies. *IEEE Access* **2020**, *8*, 22281–22302. [CrossRef]

25. Kolar, J.W.; Friedli, T. The Essence of Three-Phase PFC Rectifier Systems—Part I. *IEEE Trans. Power Electron.* **2013**, *28*, 176–198. [CrossRef]

26. Vahedi, H.; Labbe, P.-A.; Al-Haddad, K. Single-Phase Single-Switch Vienna Rectifier as Electric Vehicle PFC Battery Charger. In Proceedings of the 2015 IEEE Vehicle Power and Propulsion Conference (VPPC), Montreal, QC, Canada, 19 October–22 October 2015; pp. 1–6.

27. Tzhayek, N.; Shmaryahu, A.; Dagan, K.J.; Aharon, I. New Topology of Quasi Resonant Flyback Converter. In Proceedings of the 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 20–23 June 2022; pp. 1–4.

28. Strajnikov, P.; Kuperman, A. DC-Link Capacitance Reduction in PFC Rectifiers Employing PI+Notch Voltage Controllers. *IEEE Trans. Power Electron.* **2023**, *38*, 977–986. [CrossRef]

29. Aharon, I.; Kuperman, A.; Aharon, I.; Shmilovitz, D. Robust UDE controller for energy storage application. In Proceedings of the 2015 International Conference on Renewable Energy Research and Applications (ICRERA), Palermo, Italy, 22–25 November 2015; pp. 1269–1274.

30. Aharon, I.; Shmilovitz, D.; Kuperman, A. Multimode power processing interface for fuel cell range extender in battery powered vehicle. *Appl. Energy* **2017**, *204*, 572–581. Available online: https://www.sciencedirect.com/science/article/pii/S0306261917309157 (accessed on 15 March 2024). [CrossRef]

31. Erickson, R.W.; Maksimović, D. AC and DC Equivalent Circuit Modeling of the Discontinuous Conduction Mode. In *Fundamentals of Power Electronics*; Erickson, R.W., Maksimović, D., Eds.; Springer International Publishing: Cham, Switzerland, 2020; pp. 585–624.