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Design of a Single-Edge Nibble Transmission Signal Simulation and Acquisition System for Power Machinery Virtual Testing

He Li [1], Zhengyu Li [2], Yanbin Cai [2], Jiwei Zhang [2], Hongyu Liu [1], Wei Cui [1], Qingxin Wang [1], Shutao Zhang [1], Wenrui Cui [1], Feiyang Zhao [1,*] and Wenbin Yu [1,*]

[1] School of Energy and Power Engineering, Shandong University, Jinan 250012, China; 202214478@mail.sdu.edu.cn (H.L.); liuhongyu@mail.sdu.edu.cn (H.L.); cuiw@mail.sdu.edu.cn (W.C.); 202320707@mail.sdu.edu.cn (Q.W.); 202334614@mail.sdu.edu.cn (S.Z.); 202334550@mail.sdu.edu.cn (W.C.)
[2] Weichai Lovol Intelligent Agricultural Technology Co., Ltd., Weifang 261200, China; lizhengyu@lovol.com (Z.L.); caiyanbin@lovol.com (Y.C.); zhangjiwei1@lovol.com (J.Z.)
* Correspondence: fyzhao@sdu.edu.cn (F.Z.); wbyu@sdu.edu.cn (W.Y.)

Abstract: With the advancement of technology, the Single-Edge Nibble Transmission (SENT) protocol has become increasingly prevalent in automotive sensor applications, highlighting the need for a robust SENT signal simulation and acquisition system. This paper presents a real-time SENT signal acquisition system based on NI Field Programmable Gate Array (FPGA) technology. The system supports a range of message and data frame formats specified by the SAE J2716 SENT protocol, operates autonomously within a LabVIEW self-compiled environment, and is compatible with NI hardware-in-the-loop (HIL) systems for virtual electronic control units (ECU) calibration. This innovative, self-developed SENT system accommodates four message formats, seven data frame formats, and three pause pulse modes. Benchmarking tests were conducted by integrating this system with the dSPACE SCALEXIO HIL (located in Paderborn, Germany) system for SENT signal simulation and acquisition. The results confirm that the system effectively simulates and acquires SENT signals in accordance with SAE J2716 standards, establishing it as an invaluable asset in the electronification, intelligentization, informatization, and smart sensing of automotive and agricultural machinery.

Keywords: SENT protocol; signal simulation and acquisition; FPGA; sensor

Citation: Li, H.; Li, Z.; Cai, Y.; Zhang, J.; Liu, H.; Cui, W.; Wang, Q.; Zhang, S.; Cui, W.; Zhao, F.; et al. Design of a Single-Edge Nibble Transmission Signal Simulation and Acquisition System for Power Machinery Virtual Testing. *Designs* **2024**, *8*, 124. https://doi.org/10.3390/designs8060124

Received: 14 October 2024
Revised: 12 November 2024
Accepted: 20 November 2024
Published: 21 November 2024

1. Introduction

With the rapid advancement of automotive electronic technologies, the widespread deployment of sensors has introduced numerous challenges for vehicle electrical systems. The SENT protocol, which is widely adopted in the automotive industry, is specifically designed to transmit analog sensor signals with high precision and cost-effectiveness, eliminating the need for complex calibration systems [1]. This protocol is particularly well suited for the accurate measurement of critical parameters, such as engine temperature, speed, pressure, and position [2]. Concurrently, power machinery virtual testing has become indispensable in modern automotive development [3]. When integrated with hardware-in-the-loop (HIL) testing, power machinery virtual testing creates a realistic environment that effectively validates the control algorithms and system integration of electronic control units (ECUs) [4,5]. However, the successful execution of virtual testing requires the precise simulation and acquisition of the diverse signals needed by the ECU [6]. The complexity of the SENT protocol presents additional challenges in signal generation and interpretation, while the varied characteristics and formats of sensor signals further complicate the development of virtual testing models. Therefore, it is essential to develop a SENT signal simulation and acquisition system that is reliable, precise, flexible, and compatible with multiple operational modes to meet the requirements of virtual testing.

Regarding SENT signal transmission, P. Horsky et al. [7] analyzed the electromagnetic compatibility (EMC) principles of SENT transmission and proposed a filtering scheme for the entire pulse signal. Baran B. et al. [8] integrated a common source topology into the signal transmission circuit, thereby eliminating the need for a filter at the output. Imran Ali et al. [9] presented a design for a low-power, compact SENT signal transmitter, aimed at reducing circuit complexity while controlling hardware costs and dimensions. K. Selyunin et al. [10] employed STL and TRE to design a receiver monitoring unit, evaluating the real-time monitoring effectiveness of the SENT signal and assessing its hardware resource consumption. FPGA, a type of semi-custom circuit within application-specific integrated circuits, is widely utilized in digital circuit design due to its abundant wiring resources and reprogrammable characteristics [11,12]. FPGA-based SENT signal parsers typically exhibit high levels of integration [10,13]. Lee J-B and J. Chung [14,15] designed a digital interface for SENT signals that combines FPGA technology with onboard microcontrollers (MCUs) using the hardware description language Verilog HDL, successfully implementing the six signal transmission modes specified by the SENT protocol.

Previous research has primarily focused on electromagnetic compatibility control at the transmission end, data monitoring at the receiving end, and the miniaturization of transmitters and receivers. However, there has been limited research on the embedded application of SENT signal simulation systems and the integration of SENT signals with virtual calibration test systems. Existing signal systems are often embedded in hardware, resulting in limitations such as a restricted number of channels and incomplete channel types. Additionally, testing sensors with varying characteristics requires reconfiguring system parameters, leading to reduced testing efficiency. These systems also cannot be directly integrated into HIL systems, necessitating the use of additional hardware components. As the use of SENT modules in electronic control units (ECUs) becomes more prevalent, the demand for SENT signal simulation and acquisition systems has become increasingly critical. This paper presents an innovative SENT signal simulation and acquisition system based on LabVIEW 2023 (64-bit) and the NI FPGA board (located in Austin, TX, USA) [16]. This system integrates SENT signal simulation output with acquisition and analysis capabilities, making it suitable for the development and testing of smart sensors as well as virtual calibration of ECUs. It supports four message formats, seven basic data frame formats, and three pause modes, fully complying with the SENT protocol. The system meets performance requirements for stability and accuracy while offering data visualization and export functionality [17,18]. The design utilizes an NI FPGA board as the main platform for SENT signal simulation and acquisition, communicating with a host computer via TCP/IP. LabVIEW is used for encoding and transmitting simulated signals or decoding and visualizing acquired SENT signals on the host [19]. Ultimately, this system can operate independently within LabVIEW to provide signal simulation and acquisition for smart sensor development or be embedded into virtual power machinery testing systems for ECU testing and calibration, with added human–machine interaction features.

The original contributions of this paper are summarized as follows: 1. The system comprehensively supports all control modes specified by the J2716 standard; 2. The system facilitates real-time switching between message modes during operation; 3. Leveraging the reprogrammable nature of FPGA technology, the system allows for flexible configuration of channel numbers.

The rest of this article is structured as follows. In Section 2, a detailed introduction to the SENT protocol is provided, including the definition of the SENT signal, the composition of the signal sequence, the specific forms and implementations of the four SENT message formats, and the seven predefined data frame formats of the SENT signal. In Section 3, the architecture design and implementation approach of the SENT signal simulation and acquisition system are discussed, and based on a modular design, the independent development of the system is achieved. In Section 4, the function, stability, and reliability validation of the developed SENT signal simulation and acquisition system is conducted using the dSPACE 2022-B test bench. In Section 5, a discussion is presented on the performance and

limitation of the signal system based on the test results, along with potential directions for future research. Finally, in Section 6, the conclusions of this study are summarized.

2. SENT Protocol

The SENT protocol is a low-cost, low-power automotive communication protocol designed specifically for low-bandwidth sensor data transmission. Its key advantage lies in minimal hardware requirements, as data transmission can be achieved with only a single signal line, significantly reducing system cost and complexity. With a straightforward design that does not rely on complex protocol stacks or bus systems, SENT is easy to develop and maintain. Although its fault tolerance is not as robust as more complex protocols like CAN and FlexRay, basic error detection mechanisms ensure reliable data transmission. SENT is especially well suited for applications in which real-time requirements are low, such as temperature and pressure sensor data collection, making it an ideal solution for low-cost, low-power sensor applications. The SENT protocol is a digital communication standard designed to transmit analog signals with improved reliability and data accuracy. It facilitates efficient data transfer by converting analog signals into digital packets and utilizing a single-edge transmission method [13]. Widely used in automotive electronics and agricultural machinery, the SENT protocol is particularly well suited for sensor data transmission. Its key advantages include strong anti-interference capability, simplified hardware design, and cost-effectiveness, ensuring stable and reliable data transmission.

2.1. Definition of SENT Signal

The SENT signal is primarily used to convert analog sensor signals into digital data, consisting of a sequence of continuous pulse periods. SENT operates on a time-triggered architecture, where data are interpreted by the receiving device through a series of pulses measured from one falling edge to the next, with each pulse carrying 4 bits (nibbles). SENT measures time in clock ticks, allowing developers to set the duration of a single tick based on the sensor's output characteristics. The theoretical tick duration (t_s) typically ranges from 3 to 90 microseconds, with 3 microseconds being the common default. Each pulse cycle begins with a fixed-length low logic level of 5 clock ticks, followed by a variable-length high logic level that encodes the data value. By measuring the pulse length between two consecutive falling edges and combining this with the SENT tick period, the number of ticks within a pulse period can be calculated. This tick count is then used to identify the transmitted data through table lookup, as shown in Table 1.

Table 1. Tick count corresponding data.

N/Ticks	DEC	BIN
12	0	0000
13	1	0001
14	2	0010
15	3	0011
⋮	⋮	⋮
26	14	1110
27	15	1111

⋮ indicating a range of omitted values.

A single data packet represents a complete SENT signal sequence, as illustrated in Figure 1, which comprises five distinct components.

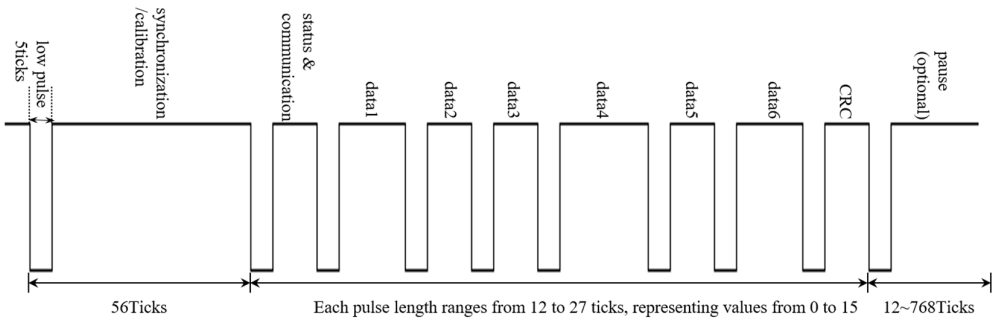

Figure 1. A frame of the complete SENT signal packet.

1. The initial pulse, known as the synchronization or calibration pulse, spans 56 clock ticks and is used for time calibration and positioning. In this study, one clock tick is equivalent to 3 μs, so the synchronization pulse lasts 168 μs.
2. The status and communication pulse, following the synchronization pulse, lasts between 12 and 27 clock ticks and transmits 4 bits of data. This 4-bit pulse serves diagnostic functions: the first two bits are reserved for specific applications, such as part numbers and error messages, while the third and fourth bits can be used to convey short serial messages or enhanced serial messages as defined by SAE J2716.
3. The status and communication pulse is followed by up to six data pulses, encompassing a total of 24 bits of data. Each data pulse lasts between 12 and 27 clock ticks, carrying 1 nibble of data. The first three data nibbles represent fast message 1, consisting of 12 bits of data, while the subsequent three nibbles define fast message 2. The specifics of the data bit signal encoding may vary depending on the particular application of the sensor.
4. The checksum pulse, lasting between 12 and 27 clock ticks, includes redundant check information to verify the accuracy of the six transmitted data nibbles. The cyclic redundancy check (CRC) is calculated using the polynomial $x^4 + x^3 + x^2 + 1$ with a seed value of 5 (0b0101).
5. An optional pause pulse follows each data packet, used to ensure equidistant SENT frame transmission or to maintain a consistent number of clock ticks. The duration of this pulse can vary between 12 and 768 clock ticks.

2.2. Message Format

The SENT signal exhibits the unique capability to transmit data at two distinct rates simultaneously. The six data nibbles are utilized to transmit fast channel data, which conveys the primary information from the sensor. Additional sensor details, such as manufacturer information or ambient temperature, may be encoded in the status nibble to constitute slow channel data. Accordingly, depending on whether the slow channel is enabled and the bit width of the transmitted data, SENT messages can be categorized into four distinct formats:

1. Fast Message Format: The most fundamental transmission mode of the SENT protocol operates without the slow channel enabled, transmitting two 12-bit data values;
2. Short Serial Message Format: Serial messages are used to transmit additional data through SENT messages, with the slow channel particularly effective for transmitting sensor data that changes minimally, such as temperature, humidity, and other factors. Given that these data points are relatively stable, they do not require rapid monitoring and can be segmented into the fast channel's data frames. A short serial message comprises 16 consecutive SENT messages. As depicted in Figure 2, bit 3 of the status nibble serves as a flag, while bit 2 transmits the data. Each 16-bit serial message contains a 4-bit message ID, 8 bits of data, and a CRC checksum.
3. Enhanced Serial Message Format with 16 bits: An enhanced serial message consists of 18 consecutive SENT messages. As illustrated in Figure 3, bit 3 of the status nibble in

the first eight SENT messages functions as a flag. The 16-bit enhanced serial message comprises a 4-bit message ID, a 16-bit data section, and a 6-bit CRC checksum;

4. Enhanced Serial Message Format with 12 bits: As illustrated in Figure 3, the enhanced serial message format with 12 bits is similar to the 16-bit format, with the main difference being that it includes an 8-bit message ID, a 12-bit data section, and a 6-bit CRC checksum.

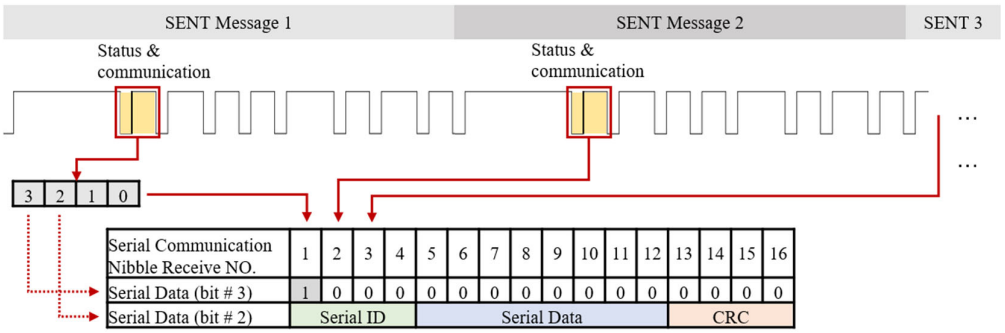

Figure 2. Short serial message format.

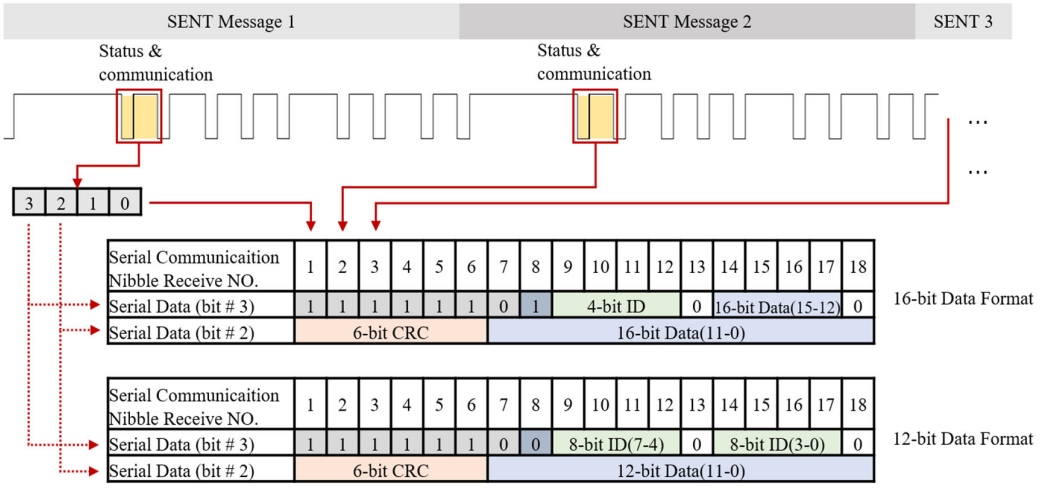

Figure 3. Enhanced serial message format.

2.3. Data Frame Format

A single SENT message is able to contain up to six data nibbles, which may be arranged in various combinations based on the specific output characteristics of the sensor. The allocation of data bits across different data frame formats is flexible and can be determined by the magnitude of the output values. The SAE J2716 SENT standard defines seven predefined protocols, along with the prescribed sequence and content of data encroachment pulses, as illustrated in Table 2. For fast channel 1, the data vector (from MSB to LSB) is segmented into 4-bit groups, corresponding to nibbles, which are then mapped sequentially to their designated nibbles. For fast channel 2, the data vector (also from MSB to LSB) is similarly divided into 4-bit groups, but is mapped in reverse order to the assigned nibbles. When sensor data from two channels share a nibble, the most significant bits (MSBs) of the shared nibble are used as the least significant bits (LSBs) for fast channel 1, while the least significant bits (LSBs) of the shared nibble are used as LSBs for fast channel 2.

Table 2. Data frame formats, data channels, and nibble orders.

Data Frame Format	Data Nibbles	Data1	Data2	Data3	Data4	Data5	Data6
Two 12-bit fast channels	6	CH1 MSN	CH1 MidN	CH1 LSN	CH2 LSN	CH2 MidN	CH2 MSN
One 12-bit fast channel	3	CH1 MSN	CH1 MidN	CH1 LSN	Not Applied	Not Applied	Not Applied
High-speed with one 12-bit fast channel	4	Bits 11-9	Bits 8-6	Bits 5-3	Bits 2-0	Not Applied	Not Applied
Secure sensor with 12-bit fast channel 1	6	CH1 MSN	CH1 MidN	CH1 LSN	Counter MSN	Counter LSN	Inverted CH1 MSN
Single sensor with 12-bit fast channel 1	6	CH1 MSN	CH1 MidN	CH1 LSN	0	0	0
14-bit fast channel 1 and 10-bit fast channel 2	6	CH1 MSN	CH1 MidMSN	CH1 MidLSN	CH1/CH2 LSN	CH2 MidN	CH2 MSN
16-bit fast channel 1 and 8-bit fast channel 2	6	CH1 MSN	CH1 MidMSN	CH1 MidLSN	CH1 LSN	CH2 LSN	CH2 MSN

3. System Architecture Design and Implementation

In previous research, many scholars have designed and developed SENT signal simulation and acquisition systems [7–10,14,15,20]. However, these designs often fail to encompass all SENT message patterns and are typically limited to specific combinations of data pulses. Furthermore, slow channel messages require secondary analysis after export, as they cannot be processed directly. As a result, these systems generally lack comprehensive functionality and exhibit limited efficiency in message processing. In contrast, the SENT signal simulation and acquisition system presented in this paper has been specifically designed and verified to support multiple message patterns defined in SAE J2716, as well as data pulse combinations from specific sensors.

In this study, FPGA programming was implemented through the LabVIEW platform. Using LabVIEW's FPGA module for hardware design, its graphical programming interface facilitated the writing of the FPGA code. LabVIEW enabled direct deployment of the design onto FPGA hardware (National Instruments (NI), located in Austin, TX, USA), achieving data acceleration and real-time processing capabilities. During the programming process, system modules were first designed and simulated in LabVIEW, then compiled to generate an .lvbitx file suitable for FPGA hardware. This approach made system design and debugging more intuitive, while leveraging FPGA's parallel processing advantages to significantly enhance computational performance. The system architecture, illustrated in Figure 4, primarily consists of two components: the host computer program and the real-time computer with an FPGA board. The host computer utilizes LabVIEW to write the FPGA program, with the simulation and acquisition sections of the SENT signal operating independently. These components are programmed separately while running at the same clock frequency. To meet the requirement for integration into a HIL testing system, the real-time computer employs the NI-PXIe-8881 (located in Austin, TX, USA) controller in conjunction with the PXIe-7856R (located in Austin, TX, USA) module. Communication between the host and real-time computers is achieved via TCP/IP.

The FPGA program is compiled into an .lvbitx file, which is subsequently downloaded to the controller. The SENT signal simulation and acquisition system can operate autonomously, using LabVIEW as the upper-level software for signal simulation or analysis. Additionally, it can be operated with Veristand 2023 Q2 software as the upper-level interface, enabling its integration into HIL testing systems for virtual calibration testing of ECUs.

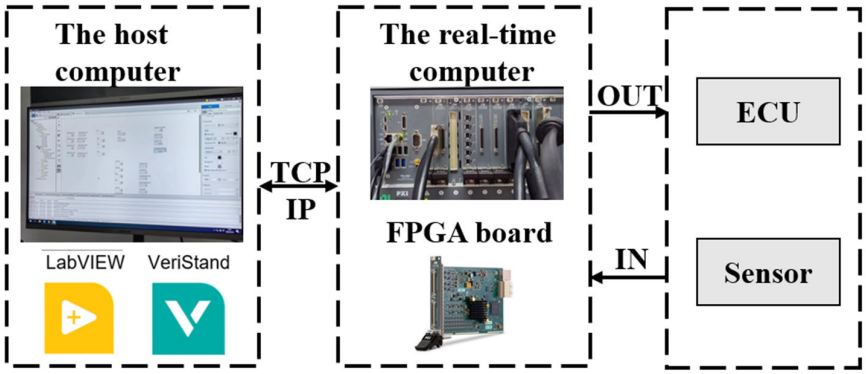

Figure 4. System architecture.

The architecture of the SENT signal simulation system is illustrated in Figure 5. The system consists of several core modules, including parameter configuration, tick conversion, message format encoding, data frame format encoding, CRC generation, and signal generation. The parameter configuration module receives parameters set by the host computer, such as message format, data frame format, and the activation of pause pulse, among others. It accommodates four message formats, seven data frame formats, and three pause pulse modes. The tick conversion module translates FPGA clock ticks into time units ranging from 3 to 90 microseconds. Once the parameters are configured, the system sequentially encodes the message format and data frame format. After the encoding process is completed, the encoded data is passed to the CRC generation module for checksum creation. The J2716 protocol provides three methods for implementing CRC checks: the 256 element array lookup, the 16 element array lookup, and the modulo-2 division. This paper adopts the modulo-2 division to implement CRC generation and validation, wherein the division is implemented through bitwise exclusive OR operations between the dividend and the divisor. Once the CRC checksum is generated, the signal generation module outputs the signal to external ECU.

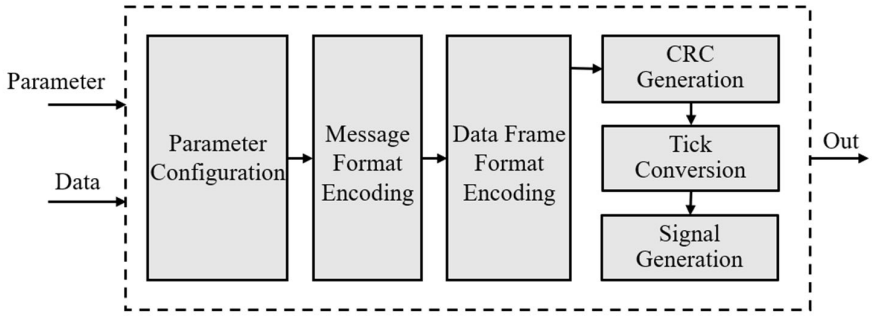

Figure 5. SENT signal simulation system.

The architecture of the SENT signal acquisition system is illustrated in Figure 6. The system comprises several key components, including parameter configuration, tick conversion, signal capture, message format decoding, data frame format decoding, CRC verification, and data visualization. The parameter configuration module allows for the input of configuration parameters, accommodating four message formats, seven data frame formats, and two pause pulse modes. The signal capture module identifies the synchronization pulse and determines the tick length based on its duration. After capturing the complete SENT message, the system sequentially decodes both fast and slow channel data. The decoded data are then transmitted externally, contingent upon successful CRC verification.

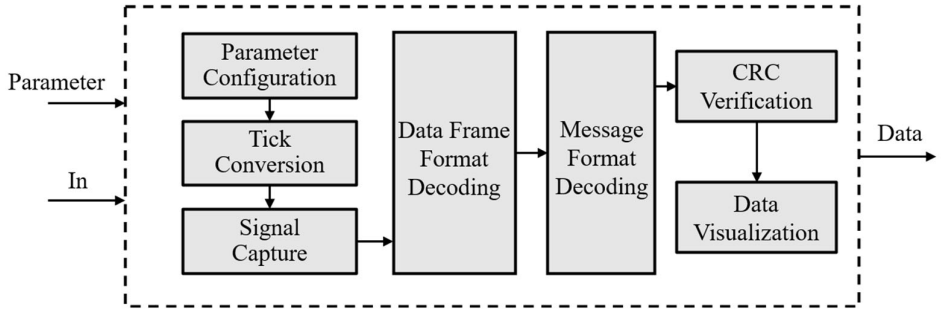

Figure 6. SENT signal acquisition system.

4. Test and Results

4.1. Test Method

To verify the functionality of the SENT signal simulation and acquisition system, the dSPACE SCALEXIO HIL system was employed for validation. The architecture of the system validation test bed, as illustrated in Figure 7, utilizes signal lines to connect the NI HIL test bed with the dSPACE test bed for signal interaction. Data transmission and analysis are facilitated through NI VeriStand and dSPACE ControlDesk 2022-B software. Relying on the results obtained from dSPACE ControlDesk, the SENT signal simulation system is assessed by verifying whether the SENT In Function successfully receives and decodes the data transmitted by the system, thereby confirming the operational integrity of the simulation functionality. In contrast, the SENT signal acquisition system is evaluated by examining the capability of NI VeriStand to successfully capture and decode the SENT signal transmitted by the SENT Out Function, thereby assessing its acquisition functionality. Additionally, custom programming in NI LabVIEW enables monitoring of the encoding and decoding processes, providing a different approach compared to the method employed with the dSPACE test bed.

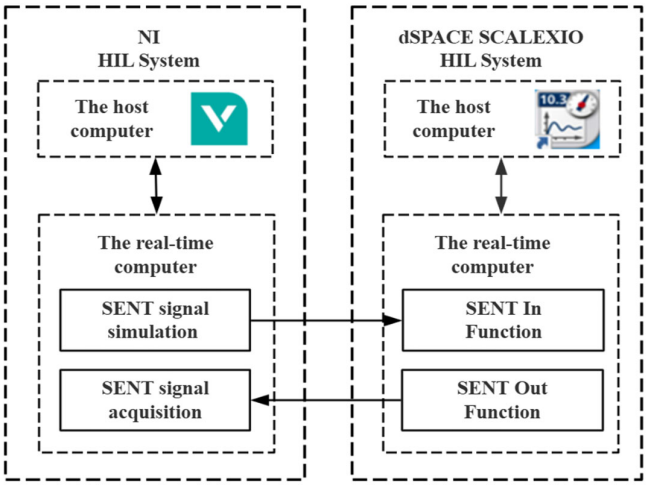

Figure 7. Functional test system architecture.

4.2. Functional Test of SNET Signal Simulation System

4.2.1. Fast Message Format

The fast message format in the SENT protocol operates independently of the slow channels, transmitting data exclusively through data pulses. The seven data frame formats within the SENT protocol are distinguished solely by the quantity and arrangement of these data pulses. Consequently, the validation of the data frame format is performed in the fast message format mode. The data used for the SENT system simulation test are presented in Table 3, all of which are randomly generated. The test results, as shown in Figure 8, compare the SENT signal transmission interface in the self-developed NI (located

in Austin, TX, USA) system software (left), with the signal visualization interface in the dSPACE system ControlDesk software (right). The results demonstrate that the SENT signal simulation system can accurately simulate various types of fast message formats. The simulated data can be correctly received and decoded by the dSPACE system. Both the transmitted and received data values, along with their checksums, remain consistent.

Table 3. Test data in fast message format.

Test Number	Data Frame Format	Data 1		Data 2		CRC
		DEC	BIN	DEC	BIN	
Test 1	Two 12-bit fast channels	179	0000_1011_0011	3871	1111_0001_1111	15
Test 2	One 12-bit fast channel	2508	1001_1100_1100	Not Applied	Not Applied	6
Test 3	High speed with one 12-bit fast channel	2676	101_001_110_100	Not Applied	Not Applied	0
Test 4	Secure sensor with 12-bit fast channel 1	1572	0110_0010_0100	Not Applied	Not Applied	unfixed
Test 5	Single sensor with 12-bit fast channel 1	4031	1111_1011_1111	0	0	4
Test 6	14-bit fast channel 1 and 10-bit fast channel 2	10,086	1001_1101_1001_10	606	10_0111_1001	6
Test 7	16-bit fast channel 1 and 8-bit fast channel 2	60,980	1110_1110_ 0011_0100	123	1011_0111	4

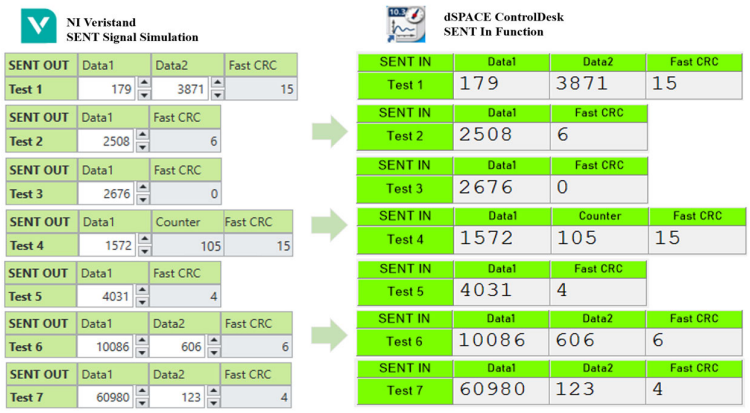

Figure 8. Fast message format results of signal simulation testing.

4.2.2. Serial Message Format

There are three distinct serial message formats. Each utilizes different encoding methods to transmit the serial ID, serial data, and CRC. In the slow channel, data are conveyed through status pulses within sequences of 16 or 18 consecutive SENT signals. The test data, as outlined in Table 4, include the serial ID, serial data, and data transmitted across 16 or 18 frames, along with the corresponding status pulse values. These test data are randomly generated. To verify accuracy, comparisons are carried out on the received data with the CRC values in dSPACE ControlDesk against the transmitted data. The results, as illustrated in Figures 9 and 10, show both the status pulse values observed during the decoding process in NI LabVIEW and the data received in dSPACE ControlDesk. As shown in Figure 9, the status pulse values of the three serial message formats are consistent with the expected values of the status data listed in Table 4, indicating that the SENT signal simulation system correctly encodes the serial message format. As indicated in Figure 10, it is confirmed that all tests are operating correctly and reliably, demonstrating that the system performs as intended.

Table 4. Test data in serial message format.

Test Number	Message Format	Serial Message ID	Serial Message Data	CRC	Status Data (HEX)
Serial 1	Short Serial Message Format	10	211	8	c040_4404 _0044_4000
Serial 2	Enhanced serial message Format with 16 bit	13	56754	35	c8_88cc_4c8c _484c_80c0
Serial 3	Enhanced serial message Format with 12 bit	158	3986	7	88_8ccc_44c4 _480c_8840

Figure 9. Status pulse values in serial message format.

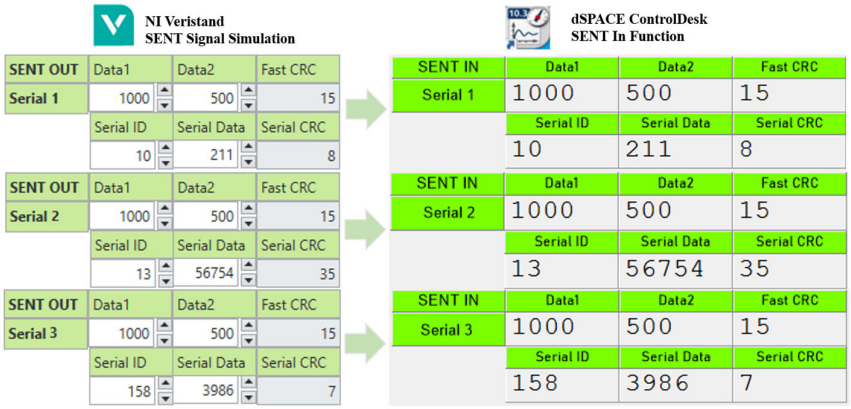

Figure 10. Serial message format results of signal simulation testing.

4.3. Functional Test of SENT Signal Acquisition System

4.3.1. Fast Message Format

The testing of the SENT signal acquisition system contrasts with that of the SENT signal simulation system. The dSPACE SCALEXIO HIL system is utilized to generate various types of SENT signals and continuously transmit them to the SENT signal acquisition system. Data from Table 3 are sent to the SENT acquisition system, and the visualization interface in NI VeriStand is configured accordingly. As shown in Figure 11, the signal tests for the seven types of data frame formats are correctly received and recognized in NI VeriStand, with the calculated CRC checksum values matching those in Table 3, except for Test 4. The discrepancy in Test 4 arises from the variable nature of the counter value, which causes fluctuations in the calculated CRC value. These test results indicate that all data frame format tests are functioning correctly and reliably, and the data acquisition capabilities are operating as expected.

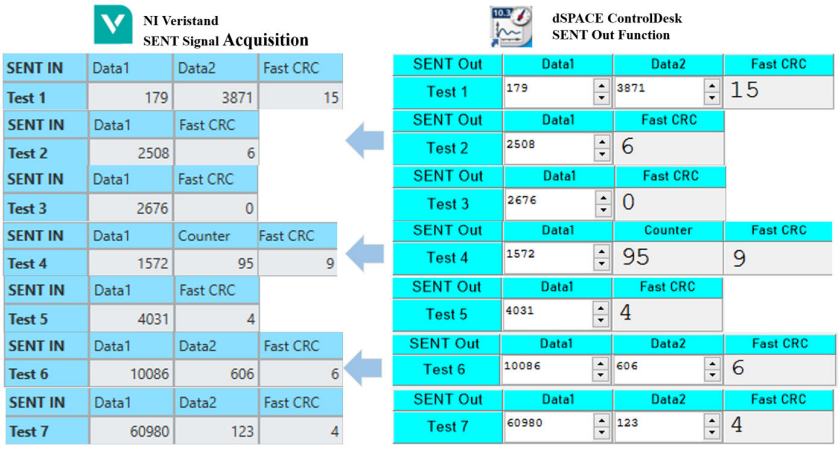

Figure 11. Fast message format results of signal acquisition testing.

4.3.2. Serial Message Format

For testing the serial message mode of the SENT signal acquisition system, the data series from Table 2 is utilized, and the visualization interface is configured in NI VeriStand. As shown in Figure 12, the results indicate that all slow channel tests are performing correctly when compared with the benchmarked data in dSPACE, and the data acquisition functionality is operating as expected.

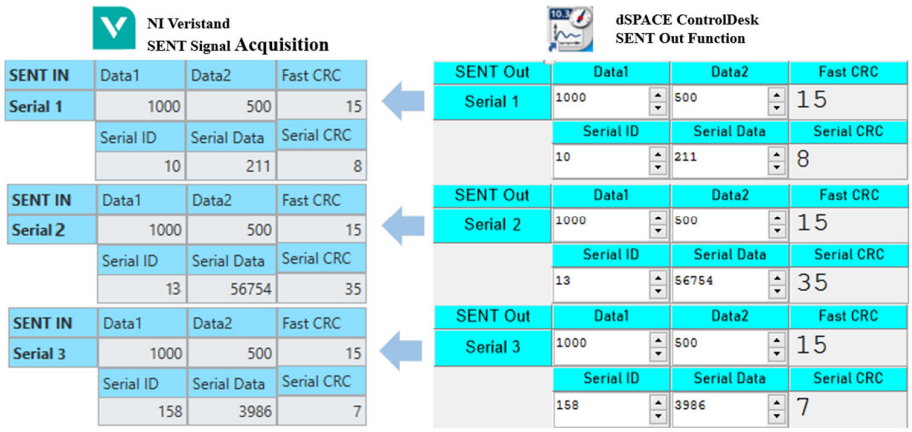

Figure 12. Serial message format results of signal acquisition testing.

4.4. Accuracy Test

To validate the accuracy of the SENT signal system, we simulated the output signals of an automotive pressure sensor, which generates two signals, d, whose sum remains constant at 4095. The output characteristics are described by Equation (1). The pressure values P_1 and P_2 are derived from the conversion of Y_1 and Y_2. Within the 0–70 bar range, pressure points were selected at 7 bar intervals for testing the SENT signal simulation system and at 10 bar intervals for testing the SENT signal acquisition system. These pressure values were converted into signal outputs using Equation (1) and recorded separately in dSPACE ControlDesk and NI VeriStand. Data from each system were used to generate curves, with the output signal of the simulation system shown in Figure 13a and the acquired signal from the acquisition system shown in Figure 13b.

$$\begin{cases} P_1 = (Y_1 - 193)/52.9 \\ P_2 = (3092 - Y_2)/52.9' \end{cases} \quad (1)$$

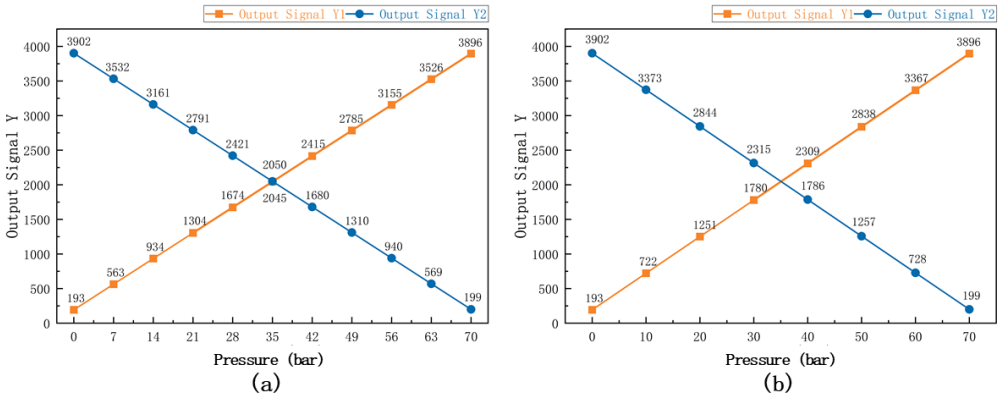

Figure 13. Accuracy test: (**a**) simulation system and (**b**) acquisition system.

The pressure points were applied cyclically, and multiple repeated experiments were conducted to increase the sample size for analysis. The resulting curves from both systems were found to be fully aligned, with identical pressure values obtained after conversion using the output characteristics formula. This consistency demonstrates the accuracy of the collected data and confirms that both the SENT signal simulation and acquisition systems meet the design accuracy requirements.

4.5. Reliability Test

To validate the stability of the SENT signal system, the simulation and testing system designed in this study was placed in a controlled environment. The same SENT signal was continuously simulated and collected for 24 h, with the output signal recorded in both dSPACE ControlDesk and NI VeriStand. A random 1 h segment of the recorded data was selected to generate the output curve. The output signal from the simulation system is shown in Figure 14a, while the signal from the acquisition system is shown in Figure 14b. Throughout the testing period, there was no external interference, and the data collection error rate remained at zero. These results demonstrate that the SENT signal system's stability meets the design requirements.

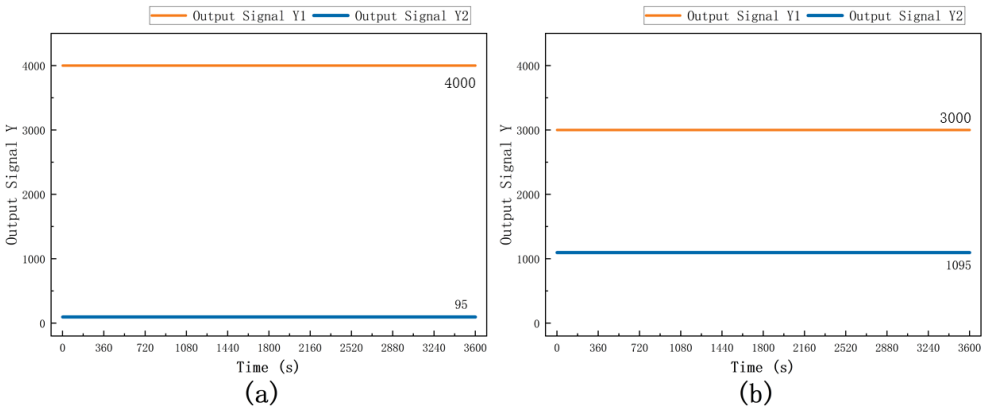

Figure 14. Reliability test: (**a**) simulation system and (**b**) acquisition system.

5. Discussion

Our research demonstrates that the proposed SENT signal simulation and acquisition system fully supports all transmission modes defined by the J2716 protocol. The system exhibits exceptional accuracy and stability under various testing conditions, with both the false acceptance rate and error rate remaining at zero throughout the tests. Notably, the system provides remarkable flexibility and real-time capability, enabling users to configure the number of channels and modify test parameters dynamically, thus facilitating

seamless mode switching. It is capable of executing a wide range of hardware tests directly, thereby eliminating the need for additional testing equipment in HIL setups. The high flexibility and real-time performance of the system are attributed to its FPGA configuration, single-cycle timing loops (SCTL), and low latency, all of which significantly enhance data processing efficiency. These characteristics align with prior research highlighting the potential of FPGAs for real-time signal processing [10–14]. In contrast to previous SENT signal systems [15,16], our system offers exceptional versatility, supporting multiple signal modes and combinations to meet diverse sensor signal acquisition requirements. Users can also customize the output as needed. The system uses LabVIEW for the development of the host computer interface and integrates with Veristand software for HIL system compatibility. This design allows the entire system to run on any personal computer or workstation without the need for additional hardware.

However, this study has some limitations. The tests were conducted only under room temperature and indoor conditions, without accounting for environmental variables such as temperature fluctuations or external noise, which may impact the reliability of the results.

Future research should explore the integration of additional message types to further assess the system's scalability. Additionally, power efficiency under varying operational conditions should be investigated to enhance the system's performance in real-world applications. The system's robustness in diverse environmental conditions, especially in high-noise environments, warrants further exploration. Ultimately, the developed system should be applied to virtual calibration studies for ECUs.

6. Conclusions

This paper presents a comprehensive design and implementation of an innovative SENT signal simulation and acquisition system tailored for power machinery virtual testing. The system integrates custom-developed host software with hardware components to achieve its intended functionality. The results demonstrate that the system supports all SENT message modes, maintaining zero error and misread rates during a 24 h testing period. Additionally, the system offers significant advantages in terms of flexibility and real-time performance.

Author Contributions: Conceptualization, W.Y.; methodology, H.L. (He Li); software, H.L. (He Li), S.Z. and W.C. (Wenrui Cui).; validation, H.L. (He Li); formal analysis, W.C. (Wei Cui).; investigation, Y.C.; resources, Z.L.; data curation, H.L. (He Li) and H.L. (Hongyu Liu); writing—original draft preparation, H.L. (He Li); writing—review and editing, F.Z.; visualization, Q.W.; supervision, W.Y.; project administration, J.Z.; funding acquisition, Z.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Shandong Provincial Natural Science Foundation grant number No. 2022HWYQ-061 and No. ZR2022QE268.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Acknowledgments: The authors extend their appreciation to AVL List GmbH for their invaluable contribution of both software and hardware resources, which were essential for the testing of the system.

Conflicts of Interest: Authors Zhengyu Li, Yanbin Cai and Jiwei Zhang were employed by the company Weichai Lovol Intelligent Agricultural Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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