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Design of High-Speed Signal Simulation and Acquisition System for Power Machinery Virtual Testing

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Abstract: The rapid advancement of model-based simulation has driven the increased adoption of virtual testing in power machinery, raising demands for high accuracy and real-time signal processing. This study introduces a real-time signal simulation and acquisition system leveraging field-programmable gate array (FPGA) technology, designed with flexible scalability and seamless integration with NI hardware-based test systems. The system supports various dynamic signals, including position, injection, and ignition signals, providing robust support for virtual testing and calibration. Comprehensive testing across scenarios involving oscilloscopes, signal generators, and the rapid control prototyping (RCP) platform confirms its high accuracy, stability, and adaptability in multi-signal processing and real-time response. This system is a state-of-the-art and extensively virtual field-tested platform for both power systems and power electronics.

Keywords: virtual testing; engine position simulation; dynamic signal acquisition; FPGA

1. Introduction

The advent of sophisticated model simulation technology has precipitated a surge in the utilization of virtual technology in the tangible world. This phenomenon entails the substitution of actual systems with scientific mathematical or physical models, which are then employed for the purpose of conducting pertinent research. In the field of power machinery, the use of model-based design (MBD) methodology in conjunction with the V-process is a widely adopted methodology for the development of controller systems. Empirical evidence demonstrates that this approach is an effective design tool for significantly shortening the research and development cycle [1–3]. This approach outlines a comprehensive workflow, encompassing the stages from conceptual design to prototype testing. It incorporates methodologies such as model-in-the-loop (MIL), software-in-the-loop (SIL), rapid control prototyping (RCP), and hardware-in-the-loop (HIL). The MBD approach is capable of performing calibration and testing tasks for virtual test benches in a variety of scenarios, thereby meeting the need for rapid development and validation of increasingly complex controller systems. This approach also allows for the attainment of superior economic benefits and a reduction in time to market [4–6].

In simulation-based virtual testing, a substantial amount of information is exchanged between the controller and the model [7]. In the real environment, the state signals of the environment as well as the plant are generated by the sensors and acquired by the controller. The control signals are generated by the controller and passed to the controlled object through the actuators. In contrast, in the virtual environment, all these signals must

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be accurately simulated and acquired by the test system, and then passed to the model through the interfaces [8].

The growing intricacy and interconnection of powertrain systems, coupled with the proliferation of sensors and actuators, present a significant challenge to virtual testing. The accurate simulation of sensor signals and the timely acquisition of actuator signals represent a crucial research area. Benchao [9] studied the simulation of oxygen sensors in HIL based on the dSPACE system and built an oxygen sensor and fault simulation system with a wide aging range for HIL testing of electronic control units. Yousif et al. [10] developed the Light Detection and Ranging (LIDAR) Phenomenological Sensor Model, and the results of the validation demonstrated that the model's processing speed is 20 times higher than that of the LIDAR frame rate. This superior performance enables its utilization for HIL system integration, thereby providing a versatile and efficient solution for virtual testing and development.

Among the variety of sensors and actuators that comprise a powertrain, a subset can be represented by 2D curves or 3D MAPs with a straightforward correlation between physical and electrical values. These sensors and actuators typically do not have stringent requirements for response speed. However, some of the devices have more complex signal forms and very high signal frequencies, which means that the frequency of the model running in the CPU is often insufficient to meet the requirements of simulating these signals. In the majority of engine HIL systems in current use, the signals in question include those relating to the position of the crankshaft and camshaft, as well as signals pertaining to fuel injection and ignition, detonation, and PWM signals [11]. Therefore, it is evident that devices capable of running at a faster pace are necessary for the simulation process. Field-programmable gate arrays (FPGAs) are an ideal solution for signal simulation and acquisition due to their adaptability to a diverse range of signal types and precise timing requirements [12].

FPGAs are capable of high-performance, real-time data processing, with each signal output customizable to a nanosecond level of precision, making them a popular choice for use in virtual systems. Bowen Jiang et al. [13] established a set of FPGA/CPU-based electric vehicles with high-fidelity electric drive models. The vehicle model is located in the CPU, while the electric drive model is located in the FPGA. The study employed vehicle skid control as a case study for validation purposes. The results for torque, rotor speed, and current exhibited a high degree of concordance between the simulation and the experimental results. Oreiller [14] constructed a model of an induction motor in FPGA and discussed the integration of this model with a HIL system. The model demonstrated high accuracy and a rapid response time, with a response speed of less than 1 ms for varying control quantities. Khimchenko et al. [15] employed Simulink to construct a mathematical model of the sensor within a HIL environment. Additionally, they conducted a comparative analysis between the FPGA scheme and the software-based simulation. The results show that the software-based simulation is nearly 35% slower than the simulation computation of the FPGA-based method, indicating that FPGAs have a greater advantage in realizing the speed response of the sensor.

In HIL studies applied to engine power systems, signal simulation, and acquisition are typically customized for specific models, with insufficient generalization capability to switch quickly between many different requirements. Additionally, the reports on the integration of signal systems with virtual test applications are relatively rare [16,17]. Conversely, systems reliant on general-purpose processors or software simulations typically exhibit high latency, which can result in delays in signal processing. FPGA computation and processing are independent in HIL test systems and do not interact with other compu-

tational tasks. Furthermore, the sensor logic allows for maximum determinism and true hardware timing reliability [18,19].

This paper puts forth a novel system that is capable of high real-time virtualization of numerous intricate sensors integrated in the engine system, as well as the precise acquisition of ECU control signals. The objective of the design is to adopt a more integrated approach to achieve multiple signal simulation and acquisition functions for the test system without the necessity for additional equipment. This innovative, independently developed approach not only meets accuracy requirements but also has the potential to reduce test costs and streamline the test process. The system is implemented based on FPGA boards, which can be readily embedded into the power machinery virtual test bench, facilitating the flexible realization of signal communication and enabling the completion of the virtual test and calibration.

The second part of this paper provides a comprehensive description of the types of signals that can be simulated or acquired by the system. It analyses the patterns and characteristics of these signals, explains the reasons for requiring signal simulation or capture, and gives the definition of signal patterns. Section 3 presents an in-depth examination of the system's architectural design and implementation, elucidating the platform utilized, a meticulous delineation of the design's sub-functions, and a comprehensive account of the optimization methodology and outcomes employed to achieve a high-performance design. Section 4 presents the methodology and results of the testing conducted on the signal system, employing a range of test systems to assess its functionality and accuracy. The results of the tests are discussed in Section 5, wherein the constraints of the tests and the deficiencies of the signaling system are analyzed. The study is concluded in Section 6.

2. Simulation and Acquisition Signal

In the virtual testing of an engine-based power system, the types of high-speed signals can be classified into two principal categories according to their respective functions. Each signal type is associated with specific roles and characteristics, and plays a pivotal role in the system's simulation and control.

The engine's position signal represents a fundamental and pivotal signal type, generated by the crankshaft and camshaft position sensors. It is utilized to ascertain the crankshaft angle and the relative position of the camshaft in real time, thereby facilitating the accurate determination of the operational status of each cylinder by the controller. The signal can be classified into three categories according to the signal pattern: encoder, $N - M$, and $N + 1$. Each category contains both digital and analog signals, which are utilized to meet the specific positioning and synchronization requirements.

Injection and ignition signals represent another crucial signal type in engine control, as they are employed directly to regulate the combustion process and optimize engine economy, power performance, and emission characteristics. Injectors can be classified into two main categories: direct and port injection systems. Similarly, ignition systems can be broadly divided into two types: electronic and mechanical. The injection signal records the essential parameters of the injection process, including the injection start moment (SOI), duration, and, in the case of multi-stage injection technology, the distinction between pre-injection, main injection, and tail injection. These parameters must be accurately captured within a cylinder's operating cycle in order to reflect the dynamic characteristics of the injection. In contrast, ignition signals are designed to capture pivotal moments in the ignition process, such as the ignition start moment. This is particularly crucial in modern electronic ignition systems, where high-precision trigger control is achieved through the analysis of the rising and falling phases of the voltage signal.

These signals furnish high-fidelity and high-precision data that facilitate the virtual testing of the powertrain, markedly enhancing the realism of the system simulation and the comprehensiveness of the control. A summary of all signal types is shown in Table 1.

Table 1. All signal types.

Functional	Category	Pattern	Signal Type
Simulation	Engine Position	Encoder N − M N + 1	Digital and Analog
Acquisition	Injection and Ignition	Injection Current Ignition Voltage	Analog

3. System Architecture Design and Implementation

The system architecture design is highly integrated in order to unify the acquisition and simulation functions of multiple signals. Furthermore, the expansion design allows for the joint use of multiple FPGA boards, thereby achieving an exponential increase in the number of sub-function channels. The system is capable of performing all-mode simulation of engine position signals, multi-channel acquisition of injection and ignition signals. Furthermore, it considers resource optimization to achieve the maximum utilization of a single board's resources.

3.1. Implementation Platform

In order to conduct this study, National Instruments (NI) products were selected to form a hardware system comprising a PXIe-1095 Chassis, a PXIe-8881 Controller, and two PXIe-7856R FPGA boards. The chassis has 18 available slots and can accommodate one or more boards. This controller is responsible for facilitating communication with the host PC, conducting simulations, and regulating the activity of all the boards. The configuration of these hardware connections is illustrated in Figure 1. The Control PC plays a pivotal role in overseeing the system's operations, with the Engine Control Unit (ECU) serving as the object under test. All signals are routed through a conditioning circuit, facilitating interaction with the ECU.

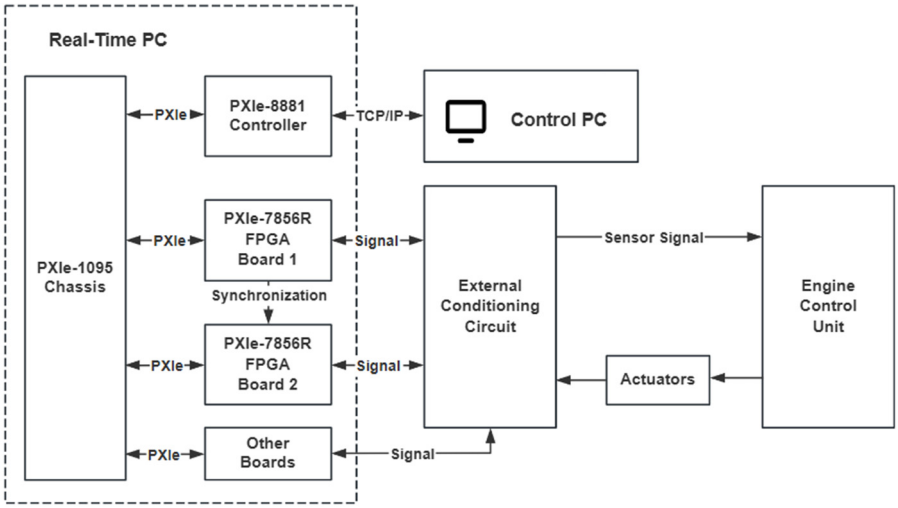

Figure 1. Hardware connection diagram.

It should be noted that this system has been designed to provide integrated high-speed signal simulation and acquisition functions for the power machinery virtual test system, and that these hardware components form part of the aforementioned system.

The system has been designed and implemented using NI LabVIEW, which provides FPGA programming modules, thus enabling the design of FPGA boards using graphical programming. The use of LabVIEW offers a lower barrier to entry and greater compatibility with NI FPGA boards than alternative hardware design languages, such as Verilog and Very High-Speed Integrated Circuit Hardware Description Language (VHDL). This facilitates the acceleration of FPGA development for applications including digital protocol communications, HIL simulation, and RCP.

3.2. System Design

The FPGA program is executed in strict accordance with the specified clock frequency. In this study, the default clock frequency of 40 MHz serves as the baseline running frequency. The system design was conducted in accordance with the cyclic programming approach.

In order to facilitate the simulation and acquisition of system signals, it is necessary to utilize a real-time simulation-based crankshaft angle degree (CAD). Consequently, the CAD calculations are executed as the highest priority task at runtime. The system combines the specified pattern and the current CAD at runtime to generate crankshaft and camshaft signals, which are then output. While the CAD is being updated, the analog input signals for the injection and ignition channels are acquired cyclically and recorded when changes in the signals are detected. The recorded data are then read and written through memory. These functions are configured in two FPGA boards, which collectively constitute the functional layer of the system design, in addition to the operational layer situated in the Control PC, which predominantly contains two pieces of NI software, Veristand (2023 Q2) and LabVIEW (2023 Q1); and the hardware interface layer for interaction with the outside. The system architecture is illustrated in Figure 2.

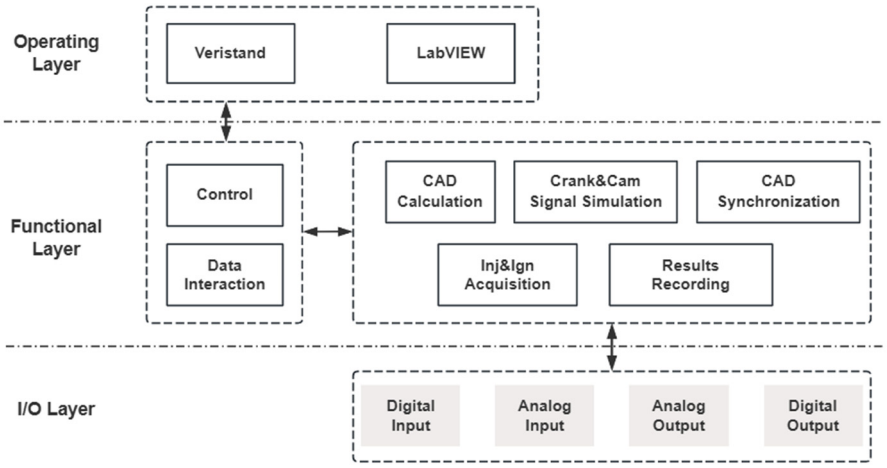

Figure 2. System software function design architecture.

3.2.1. Engine Position Simulation Function

The new calculated value of CAD is obtained by adding an angular change value to the previous moment's angle in the loop. This value is defined as the angular step value and is calculated as follows:

$$\begin{aligned} CAD_{t+1} &= CAD_t + \delta_{deg}, \\ \delta_{deg} &= N \times 6/f_{clk}, \end{aligned} \quad (1)$$

where δ_{deg} is the angular step value in degrees; N is the engine speed in rpm; and f_{clk} is the FPGA clock frequency, a constant value, 40 M.

It is necessary to adjust CAD for the effective angle range, which depends on the specific engine type. For a two-stroke engine, the value of CAD upper limit should be 360, while for a four-stroke engine, it should be 720. In the event that CAD_{t+1} exceeds the specified range, it is necessary to subtract CAD_{t+1} from the upper limit of the corresponding range.

Crankshaft and camshaft signals can be classified into two main categories: digital and analog. The generation of digital signals is achieved through the generation of Boolean values corresponding to high and low levels. The generation of analog signals; however, necessitates the calculation of sine wave frequencies. The crankshaft and camshaft signals are specified in different ways. The pattern of the crankshaft signal is described in terms of the number of teeth N, the number of missing teeth M, the high pulse width (HPW), the low pulse width (LPW), the offset of the missing teeth, and whether or not the TDC is rising. Figure 3 illustrates a simulated signal in the classic N-M pattern.

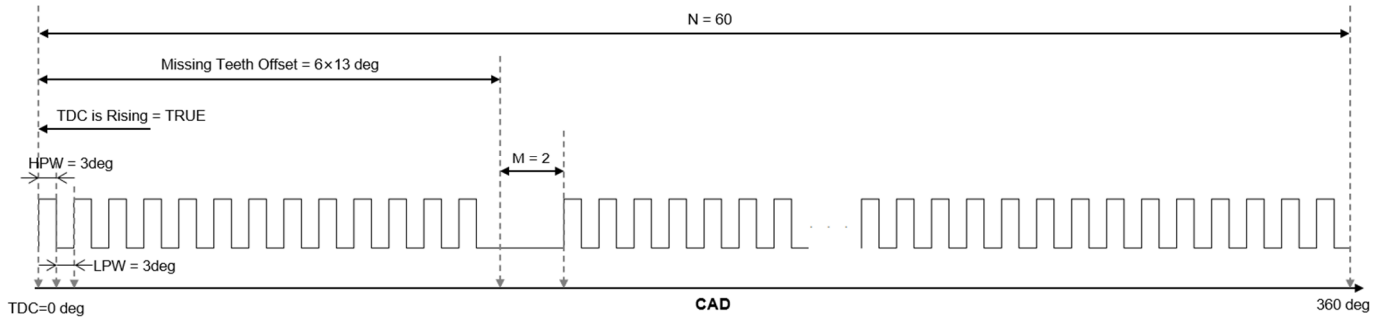

Figure 3. N-M pattern signal. N = 60, M = 2, TDC is Rising = True.

The relationship between the number of teeth and pulse width is expressed by the following equation:

$$HPW + LPW = 360/N, \quad (2)$$

The camshaft signal pattern is described in terms of the start and end angles of each tooth, as well as whether the first angle represents a rising edge. These angles are defined as the inversion angle, indicating that the signal is inverted at this position. An illustration of the inversion angle is provided in Figure 4, and it corresponds to the CAD.

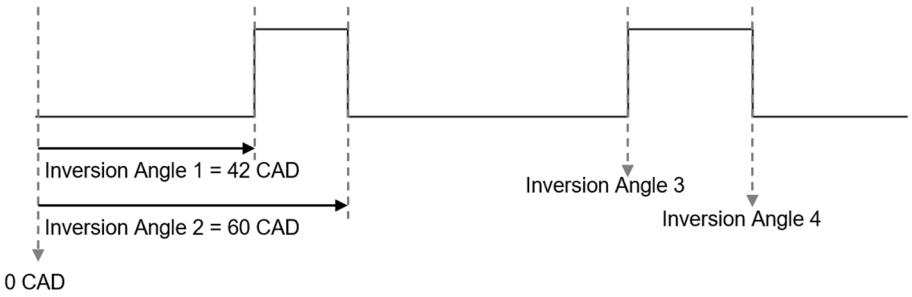

Figure 4. Schematic of inversion angle (First Angle is Rising = True).

The present CAD is juxtaposed with the angle delineated by the pattern to ascertain whether it is situated at a specific tooth position. In the event that it is, the Boolean value representing the digital signal is designated as True, signifying a high value, and conversely, False, indicating a low value. In the missing teeth, the Boolean value is set to False, and this Boolean value is conveyed through the corresponding FPGA I/O node for digital signal output.

In the case of digital signals, a change in rotational speed results in a change in the angular step value. As the rotational speed increases, the step value also increases, leading to faster transitions between the high and low levels. In consequence, for analog signals, the frequency of the sine signal must be altered. Generation of the sine signal is not merely a matter of comparing angles; it also entails resetting the sine signal module to the new frequency. LabVIEW provides a functional component for generating sine signals, designated the Sine Wave Generator. This accepts a frequency and an offset as inputs and can be reset using the reset interface. The input frequency is expressed in period/tick, which is distinct from the conventional unit of Hz. The relationship between them and the angular step value is described by the following equation:

$$f_{pt} = f/f_{clk} = \delta_{deg}/\text{Pulse Width}, \quad (3)$$

where f_{pt} is the sine wave frequency in period/tick and f is the sine wave frequency in Hz. For crankshaft signal, Pulse Width is the sum of HPW and LPW, and for camshaft signals, Pulse Width is the difference between the two inversion angles, with the difference between the first inversion angle and the last inversion angle being corrected by adding 360 or 720 for correction to ensure signal continuity.

The reset input signal is reset at the conclusion of each pulse cycle, thereby ensuring that speed alterations between teeth are duly updated in a timely manner for the generation of the analog signal.

3.2.2. Injection and Ignition Signal Acquisition Function

The injection and ignition signals are acquired using an analog input channel, and the raw signals must be converted to acceptable voltage signals by the signal conditioning board in advance. By identifying the trend of the analog signal, it is possible to distinguish whether the signal is in the rising or falling edge. A signal exceeding the rising threshold can be considered the onset of a valid signal, while a signal below the falling threshold can be regarded as the conclusion of a valid signal. Through the comparison of analog signals, they can be converted to digital signals, with a Boolean value of True representing a valid signal. The establishment of reasonable rising and falling thresholds allows for the majority of noise signals to be disregarded, thereby enhancing the accuracy of recognition. The complete conversion process is illustrated in Figure 5.

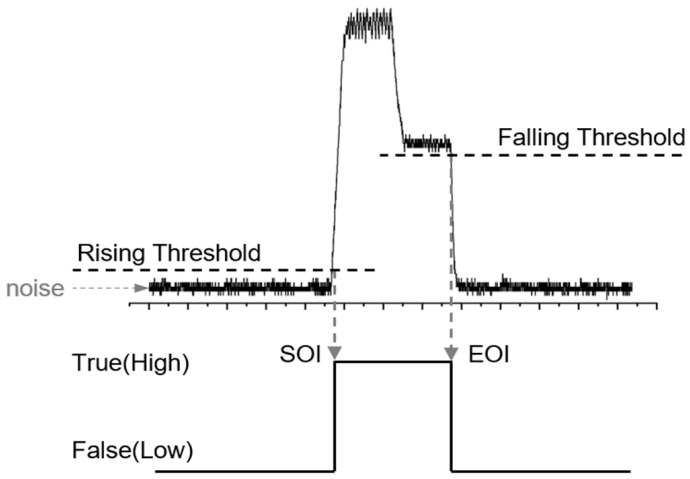

Figure 5. Analog-to-digital conversion of injection signal.

In order to reduce the interference of noise and improve the accuracy of the acquisition results, a dual filtering function comprising analog and digital filtering was designed. Prior

to signal comparison, analog filtering is employed utilizing the moving average method, whereby a specific number of samples are averaged to generate the filtered output. The moving average filtering method is represented by the following equation:

$$M_i = (y_{i-n+1} + y_{i-n+2} + \ldots + y_i)/n, \quad (4)$$

where M_i is the average filtering result value, y_i is the i-th sample value, and n is the average number of filter samples.

Before detecting whether the signal is valid or not, digital signal filtering is used to prevent jitter during the rise or fall of the signal from causing incorrect comparison judgment results, the filtering method used is the de-jittering filtering method. At the same time, the design of the digital filter takes into account the possible effect of the delay on the angle recording: when the first signal change is detected, the current CAD is locked in the filter, and if there is no change in the N consecutive sampling points, the angle is output together.

Timing uses a cyclic accumulation of ticks, resetting the count at the start, accumulating it as the cycle progresses and outputting it at the end. The relationship between count and time is calculated using the following equation:

$$\text{Time} = \text{Count}/f_{clk}, \quad (5)$$

The result recording function is used to store the information of multiple injection or ignition signals, write the SOI, EOI, and duration to memory for management, and record the number of injections or ignitions. The recording program reads and outputs all the data stored in memory at the end of the current engine working cycle.

3.2.3. Integration and Extension

The traditional LabVIEW programming methodology employs the discrete architectural framework of the RT-FPGA. However, virtual test benches utilize NI Veristand as the unified configuration, management, and runtime software for the system. The separate architecture is not conducive to integration. Veristand provides a means of setting up custom devices that can be invoked by designing an FPGA program set as an FPGA add-on device. Veristand employs an Interrupt Request (IRQ) function in the program design, assigns the interrupt address a value of 30, and places this interrupt function before all programs are executed. Veristand utilizes this IRQ to regulate the initiation of read and write operations.

In consideration of the necessity for system expansion, the system has been designed with a master-slave architecture, which permits the connection and operation of multiple FPGA boards in order to increase the number of channels available for a given function. It is important to note the distinction between the master and slave programs, which are executed on different boards. Both are required to perform CAD calculations. Upon completion of a work cycle, the master program issues a high-level reset command, which is received by the slave program via a digital channel. This enables synchronization of the angle with the master program. This synchronization guarantees that the simulation engine positions of multiple FPGA boards are aligned, thereby ensuring the consistency of the simulation and acquisition of signals. In the example implemented in this study, FPGA board 1 serves as the master FPGA, while board 2 serves as the slave FPGA, as illustrated in Figure 1. The architectural design is illustrated in Figure 6.

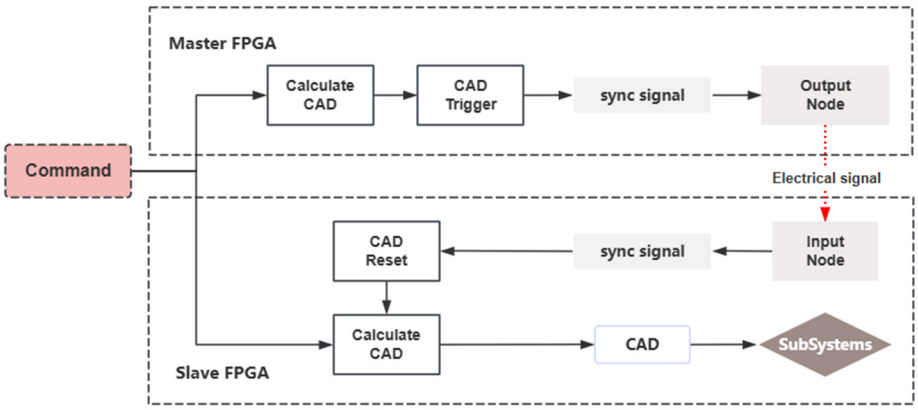

Figure 6. Synchronized architecture design.

3.3. Optimization of the Design

The LabVIEW 2023 Q1 software provides a Single-Cycle Timed Loop (SCTL) module for the design of FPGAs. The use of a traditional while loop in an FPGA necessitates a minimum of three clock ticks to complete each iteration. In contrast, the SCTL module enables all functions within the loop to be well performed within a single clock tick. The FPGA clock employed in the system operates at a frequency of 40 MHz, which corresponds to a duration of 25 ns for a single clock tick. The utilization of the SCTL ensures a deterministic response for signal simulation processing, with the exception of functions that are not supported by the SCTL itself, such as Analog IO Node, For Loop Body, and Division. The remainder of the system functionality is implemented within the SCTL through an optimized architectural design. The system's functions have been implemented within the SCTL through an optimized architectural design, which has significantly enhanced the real-time and response determinism of the system at the design stage.

In the original architectural design of the injection and ignition signal acquisition system, subfunctions were processed in multiple while loops, with multiple for loops nested within the while loops. This resulted in a program that was unnecessarily complex and placed undue burden on the limited hardware resources of the FPGA.

In accordance with the aforementioned optimization methodology, this study proceeds to partition the function and refine the configuration of the original architectural framework. The signal processing stage comprises four distinct phases: signal acquisition, analog filtering, digital-to-analog conversion, and digital filtering. Collectively, signal processing and signal detection constitute the content of the first while loop. The optimization process is achieved by maintaining the analog signal processing component within the while loop and implementing the digital signal processing component within the SCTL. In the original structure, the result recording of all channels is performed in parallel. That is to say, all channels are scanned in a single loop, and the results are read or written to memory. The output uses a for loop to construct the result array. The result recording component is not constrained by execution speed requirements. Consequently, the optimized structure transitions from a parallel procedure to a sequential execution approach, whereby the result of a single channel is processed within a single loop. Additionally, the reading or writing process is independent and does not interfere with the other, allowing for the application of SCTL and enhanced efficiency.

A sketch of the original architectural designs and optimized structures are illustrated in Figures 7 and 8, respectively.

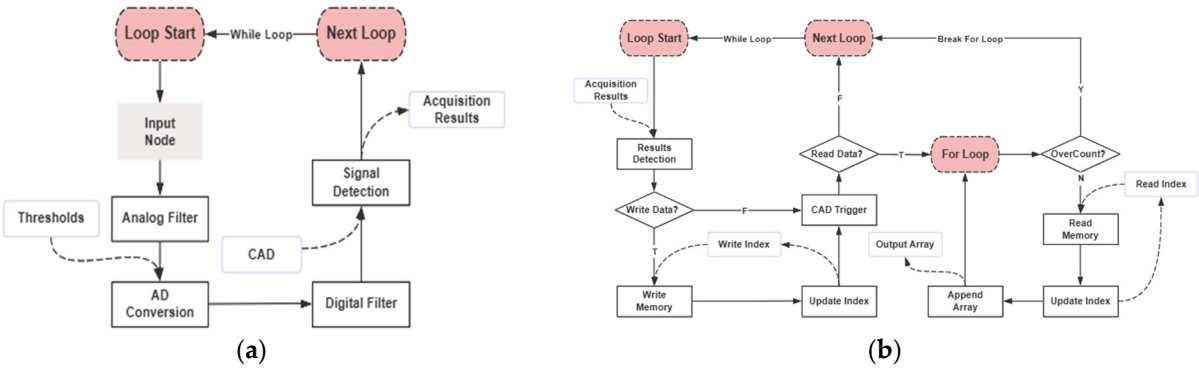

Figure 7. Architecture before optimization. (**a**) Signal acquisition and detection function; (**b**) Result recording.

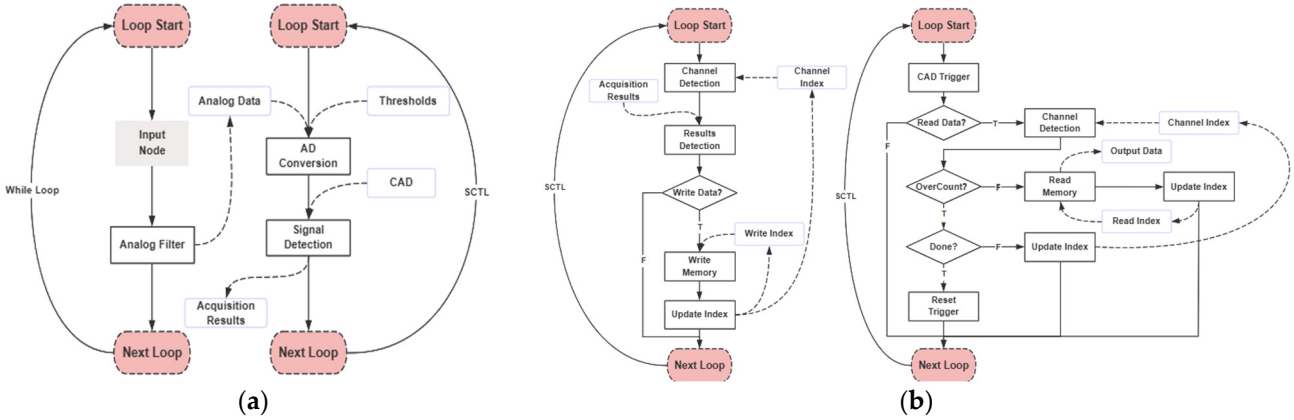

Figure 8. Architecture after optimization. (**a**) Signal acquisition and detection function; (**b**) Result recording.

A comparison of the FPGA resource usage before and after optimization is shown in Table 2, where it can be seen that the resource usage has been effectively reduced.

Table 2. Comparison of resource usage.

Device Utilization	Total	Used (Before)	Percent (Before)	Used (After)	Percent (After)
Slice Registers	202,800	114,019	56.2	40,536	20.0
Slice LUTs	101,400	98,849	97.5	41,303	40.7
Block RAMs	325	36	11.1	42	12.9
DSP48s	600	40	6.7	27	4.5

4. Test and Results

Once the system has been designed and implemented, it is essential to conduct a series of tests to ascertain whether the system meets the desired functionality and accuracy requirements. This section introduces the test methods employed in the present study and subsequently presents the results of each test of the system in turn. These include the functional test and the accuracy test.

4.1. Test Methods and Systems

The present study combines a variety of test systems utilizing oscilloscopes and signal generators to verify basic functionality. In addition, a laboratory-developed RCP platform

is employed for the purposes of accuracy testing. The architecture of the test program is illustrated in Figure 9.

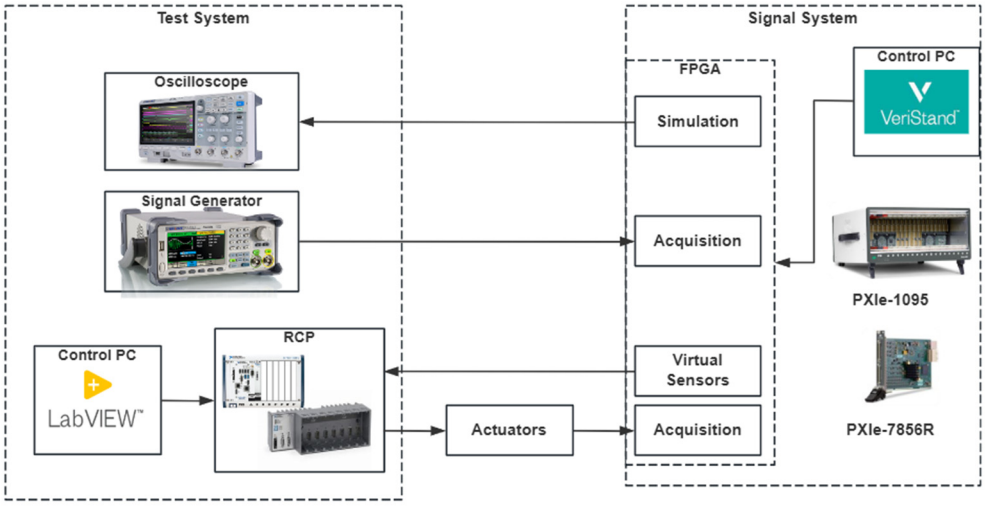

Figure 9. Architecture of the test program.

The oscilloscope is the SIGLENT SDS1104X-U, which has a maximum sampling rate of 1 GSa/s, a bandwidth of 100 MHz, and four sampling channels. The signal generator is the SIGLENT SDG2122X, which has two output channels, a maximum output frequency of 120 MHz, and is capable of generating square, sine, or pulse waveforms.

The RCP platform is constructed using NI equipment that incorporates the MATLAB/Simulink design tool chain, thereby facilitating the development of bespoke control strategies and models. Additionally, it is equipped with actuators, including injectors and valves, which are utilized to regulate the powertrain, and is capable of detecting a diverse range of sensor signals. The RCP system consists of a PXIe-1082 chassis, a PXIe-8840 controller, an NI 9155 CompactRIO chassis, and some boards. The NI 9155 contains a Virtex-5 LX85 FPGA chip, communicates with the controller via MXI-Express, and has eight slots that integrate multiple C Series modules. LabVIEW FPGA programs have the capability of calling upon these modules in order to implement a number of functions, including engine position tracking, injection control, and analog signal detection.

4.2. Functional Test

In the engine position simulation function test, the test is set to rotate at 1200 rpm, the number of strokes is four, the crankshaft signal pattern is set to 60-2 teeth, the offset of missing teeth is 132 CAD, the TDC is Rising is set to True, and the inversion angle of the camshaft signal pattern is set as shown in Table 3.

Table 3. Camshaft signal pattern.

Channel Number	Inversion Angle	Signal Type	First Angle Is Rising
1	48 54 168 174 288	Digital	True
2	294	Digital	False
3	408 414 528 534 558	Analog	True
4	564 648 654	Analog	False

The crankshaft and camshaft signals captured by the oscilloscope are shown in Figures 10–12.

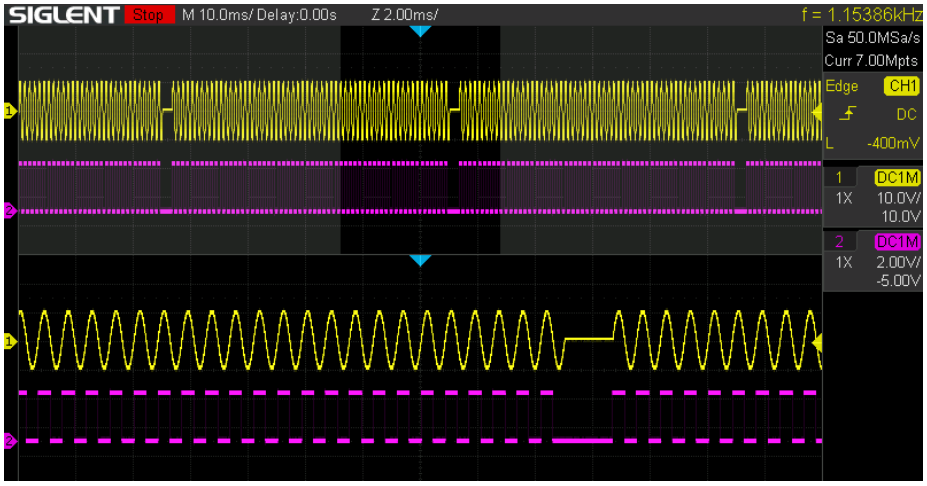

Figure 10. Crankshaft signal waveforms.

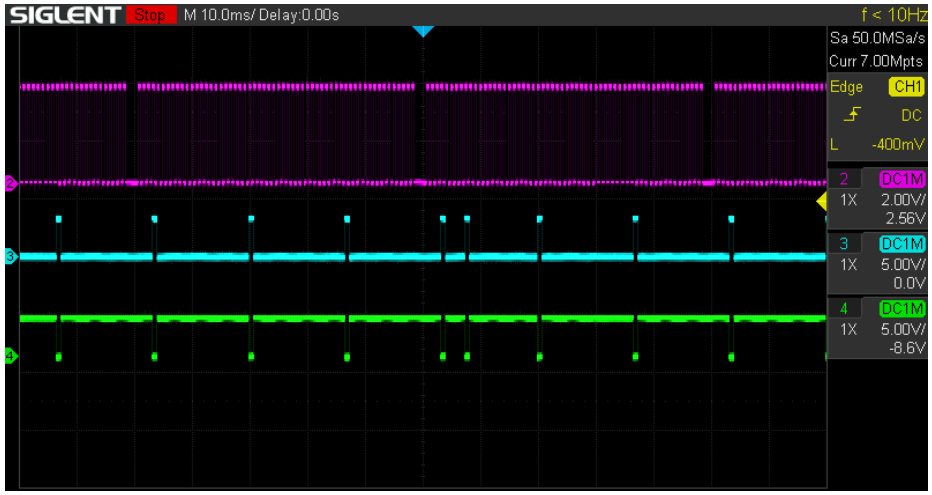

Figure 11. Digital signal waveforms of camshaft.

Figure 12. Analog signal waveforms of camshaft.

To test the functionality of the injection and ignition signal acquisition, a signal generator was used to generate a sinusoidal signal matched to the appropriate signal frequency based on the engine position simulation, allowing the signal to be acquired multiple times

in a single cycle. Four different test cases were used and the error in the results with and without filtering was compared. The results are shown in Table 4.

Table 4. Functional test results of injection signal acquisition test.

No.	Sine Wave Frequency	Expected Number of Acquisitions	Actual Number (Without Filtering)	Actual Number (With Filtering)
1	10	1	151	1
2	30	3	134	3
3	50	5	72	5
4	70	7	154	7

4.3. Accuracy Test

The accuracy of the system was expressed as the error between the signal parameters of the RCP and the signal parameters of the system. The RCP integrates control strategy models designed in MATLAB R2023a/Simulink to achieve efficient variation in the control parameters.

The EPT function of the RCP was tested on both digital and analog signals. The accuracy was checked by comparing the difference between the CAD of the EPT and the CAD of the simulation. The equation is as follows:

$$\begin{aligned} E_{CAD} &= CAD_{RCP} - CAD_{sys}, \\ E_{Speed} &= Speed_{RCP} - Speed_{sys}, \end{aligned} \tag{6}$$

where the subscript 'sys' represents the simulation value of the system and the subscript 'RCP' represents the identified value of the EPT function in the RCP.

The error is defined as the observed value minus the true value. The true value is the setpoint or simulated value, while the observed value is the acquired data. The maximum error value under the test condition is recorded, and subsequent error values are similarly documented.

The results of the accuracy test for the engine position simulation are presented in Table 5.

Table 5. Accuracy test results of the engine position simulation.

Test Speed (rpm)	CAD Error (deg)		Speed Error (rpm)	
	Digital	Analog	Digital	Analog
600	−0.037	−0.156	0.009	0.010
1200	−0.043	−0.171	0.035	0.033
2000	−0.048	−0.183	0.100	0.105
3000	−0.063	−0.190	0.221	0.241
5000	−0.049	−0.203	0.625	0.673

The injection signal employed for the test is generated by the RCP-driven DI injector. The injection control parameters are provided by the injection control model constructed in Simulink. This model utilizes speed and throttle as inputs, calculating the injection degree before TDC (DBTDC) and energization time (ET). These values are then compared with the data captured by the system to ascertain their accuracy. The DBTDC error and ET error are defined by the following equation:

$$\begin{aligned} E_{DBTDC} &= DBTDC_{sys} - DBTDC_{RCP}, \\ E_{ET} &= ET_{sys} - ET_{RCP}, \end{aligned} \tag{7}$$

Throttle set to maximum at all test points. Test results are shown in Table 6.

Table 6. Accuracy test results of the injection acquisition.

Test Speed (rpm)	DBTDC Error (CAD)	Set ET (ms)	ET Error (ms)
600	−0.072	1.899	0.010
900	−0.098	1.857	0.004
1200	−0.103	1.880	0.004
1500	−0.166	1.871	0.006
1800 *	−0.182	1.710	0.005

* The data are from a real engine, so the maximum test speed is controlled at 1800 rpm.

5. Discussion

In this study, a high-speed signal simulation and acquisition system is designed based on the LabVIEW programming environment and the NI hardware platform. By using the function modules provided by LabVIEW, the system is able to run in FPGA and has compatibility with Veristand. The system shows excellent performance in high-speed signal simulation and acquisition, meets the integration requirements of the power machinery bench for accurate simulation and real-time acquisition of engine position signals, injection and ignition signals, and provides a basic hardware and software environment for performing virtual test tasks. The test results show that the system has high accuracy and stability under different signal modes and test conditions, and the error is within a very small range, which can meet the strict requirements of the power machinery virtual test system for the frequency and accuracy of signal simulation. Especially for high-frequency signals, the system can accurately capture all kinds of complex signals, such as injection and ignition signals, with very high sampling and processing frequencies, greatly improving the authenticity and reliability of virtual testing.

Compared with existing research, the innovation of this system is that it integrates the simulation and acquisition of various types of signals and achieves effective resource utilization and high real-time performance through the optimized design. This design not only improves the integration level of the system, but also effectively reduces the need for test equipment and experimental costs. At the same time, the system's enhanced functions satisfy the need for functional reconfiguration due to changes in test requirements.

However, this study has some limitations. The experimental tests were mainly conducted in a standard indoor environment without considering the influence of real environmental factors such as temperature, humidity, vibration, and noise, and electromagnetic compatibility in complex electrical environments was not considered at this stage. Future research can expand the scope of testing to include different environmental conditions to verify the robustness and reliability of the system. In addition, although the present system is able to handle complex signals efficiently, there is still room for improvement in the response to transient situations, and the accuracy of the system under these conditions deserves further investigation.

Future research could also further improve the efficiency of the system, especially during long run times and high load tests, to optimize its performance in real industrial applications. In addition, with the development of multi-cylinder engines and hybrid systems, the system's functionality should be further extended to support more types of signal simulation and acquisition to meet more complex testing needs. The system can be used not only for virtual testing and calibration, but also for the development and optimization of intelligent control systems to support real-time monitoring and fault diagnosis of power systems.

6. Conclusions

This study proposes a novel system for power machinery virtual testing, capable of real-time simulation and accurate acquisition of key signals in the engine system. Its optimized architecture delivers high-fidelity signal processing, robust scalability, and reliable support for virtual simulation and testing. The experimental results obtained across a range of scenarios demonstrate that the system exhibits high accuracy, stability, and adaptability, particularly in the context of complex injection and ignition signals. Future work will focus on enhancing the system's environmental adaptability and power efficiency, thereby facilitating broader practical applications.

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