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Lateral Fractal Formation by Crystallographic Silicon Micromachining

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Abstract: A novel wafer-scale silicon fractal fabrication method is presented here for forming pyramids only in the lateral direction using the crystal orientation of silicon. Fractals are fabricated in silicon by masking only the corners (corner lithography) of a cavity in silicon with silicon nitride, where the shape is determined by the crystal {111} planes of the silicon. The octahedral cavity shaped by the {111} planes was previously only used for forming octahedral fractals in all directions, but by using a planar silicon dioxide hard-mask on a silicon (100) wafer, the silicon octahedral cavity is "cut in half". This creates a pyramid with sharper edges and vertices at its base than those determined by just the {111} planes. This allows selective corner lithography patterning at the vertices of the base while leaving the apex unpatterned, leading to lateral growing of pyramidal fractals. This selective patterning is shown mathematically and then demonstrated by creating a fractal of four generations, with the initial pyramid being 8 µm and the two final generations being of submicron size.

Keywords: micromachined fractals; corner lithography; submicron; wet-etching; pyramid

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1. Introduction

Fractals consist of broken geometries featuring identical shapes in various scales. In Latin, fractal means broken or fractured and the term was introduced by the mathematician Mandelbrot in 1975 [1]. The concept of fractals has interested many scientists in various fields. In crystalline silicon (Si) micromachining, it has been shown that lateral fractals can be fabricated along preferential crystallographic directions photoelectrochemically with some level of directional control using photoelectrochemical etching [2,3]. However, the fabrication of fractals can be quite labour intensive and complex when making each generation in a controlled manner with respect to orientation and shape. It has been demonstrated that 3D fractals can be engineered in a robust and time-efficient way using corner lithography in combination with anisotropic wet-etching in an auto-multiplying process. The crystallographic nature of Si is used to fabricate smaller features at the concave corners of geometries bounded by the slow etching {111} planes [4].

Corner lithography is a self-aligned wafer-scale technique which was initially developed to fabricate submicron features such as 3D nanowire frames without requiring expensive or low-throughput lithography techniques [5]. It is based on conformal deposition of a layer with thickness t on nonflat templates featuring concave corners with effective thickness $a = \frac{t}{\sin\left(\frac{\alpha}{2}\right)}$, where α is the angle of the relevant planes forming the concave corner. After timed isotropic etching by an amount of $r \geq t$, a defined residual layer with thickness $b = a - r$ will remain in concave corners while the layer is removed from the flat surface and convex corners. This principle is illustrated for two intersecting planes in Figure 1 [6].

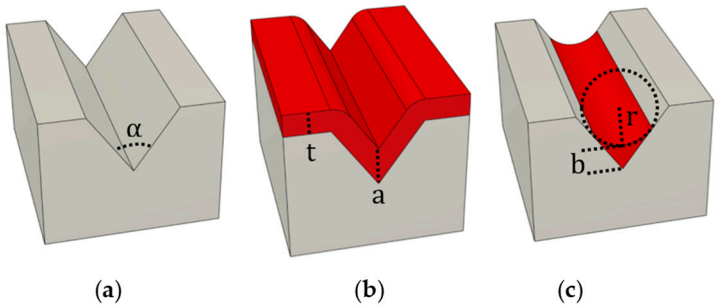


Figure 1. Schematic illustration of the basic principle of corner lithography: (**a**) nonflat substrate with a concave corner with angle α, (**b**) conformal deposition of material with thickness t and effective thickness a in the concave corner and (**c**) timed isotropic etching by amount r leaving a material with thickness b in the concave corner.

The geometry of the residual layer in the concave corners depends on the number of intersecting planes. Two intersecting planes result in a thin residual "wire" and three or more planes in a small residual "dot". This defined residual layer can be well controlled if the structural layer is conformally deposited and etched highly isotropic and selective. It is compatible with micro- and nanomachining, where the initial template defines the exact position and spatial arrangement. This method was further investigated for using it as an inversion mask in combination of local-oxidation-of-silicon (LOCOS) in subsequent fabrication steps [4,5]. A pyramid with tunable nanoapertures close to the tip was fabricated. Furthermore, this process showed to be capable of creating vertical and horizontal suspended nanowires [7].

Corner lithography is used to fabricate octahedral features and fractals [4], 3D nanowires [5,6], 3D nanoapertures at the apex of pyramids [4,5,7], nanoring particles and photonic crystals [8], fluidic components [6], and high-aspect-ratio octahedra and donut-like structures [9]. These structures have been applied in AFM probes [4,6,10], gas permeation [11], and cell trapping devices [6].

Micron-sized 3D fractals formed of self-similar silicon octahedral structures were initially fabricated by means of iterative cycles of anisotropic etching of silicon and corner lithography [4]. Both fractals with holes and fractal networks of wire frames were demonstrated. The fabrication scheme of 3D fractal fabrication is shown in Figure 2.

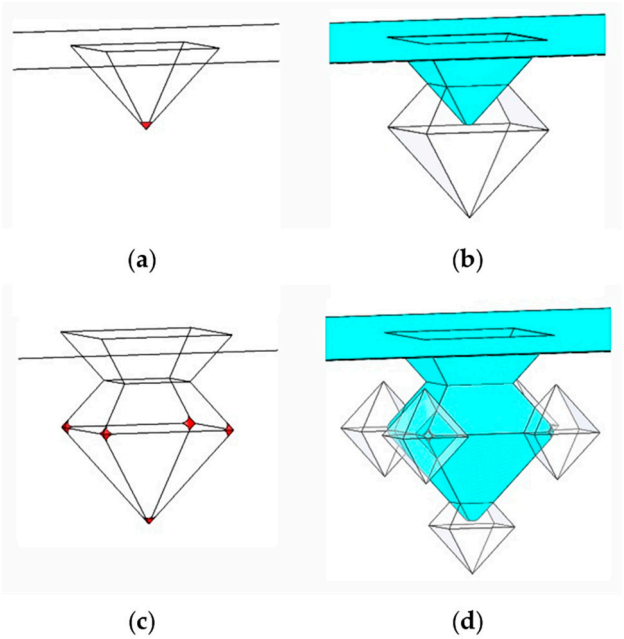
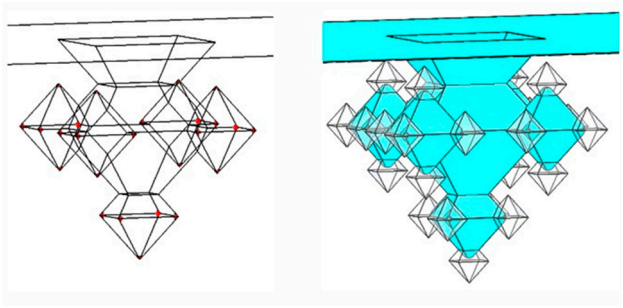


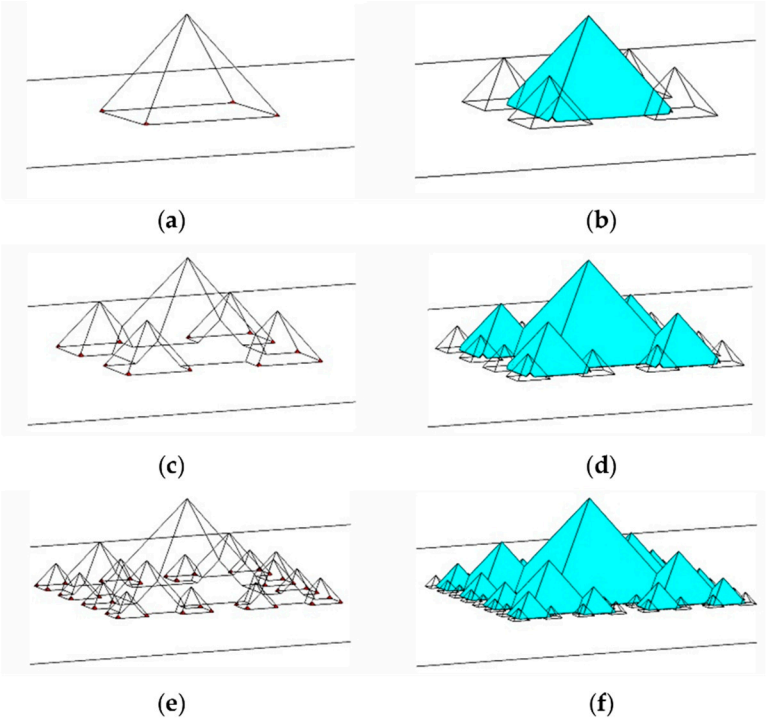
Figure 2. *Cont.*



(**e**) (**f**)

Figure 2. Schematic overview of the formation of 3D fractals using (**a**) inverted pyramid and applying corner lithography followed (**b**) by etching the masking layer and etching silicon to form next generation fractals. The steps are repeated to form second—(**c**,**d**) and third—(**e**,**f**) generation fractals.

This fabrication principle of forming the fractals in all directions can be applied to form fractals in the lateral direction. It is expected that the inverted pyramid under a hard-mask creates a set of sharper convex corners at the vertices compared to the apex, which gives a new degree of control to further process these vertices. The fabrication principle of fractals grown in the lateral direction is schematically shown in Figure 3.



(**a**) (**b**)

(**c**) (**d**)

(**e**) (**f**)

Figure 3. Schematic overview of the formation of fractals in lateral direction using corner lithography (**a**,**c**,**e**) in combination with anisotropic wet-chemical of silicon (**b**,**d**,**f**).

In this paper, the pyramid geometry is theoretically analysed considering corner lithography. This geometry analysis is applied experimentally to show the feasibility of fabricating in-plane fractals.

2. Theory

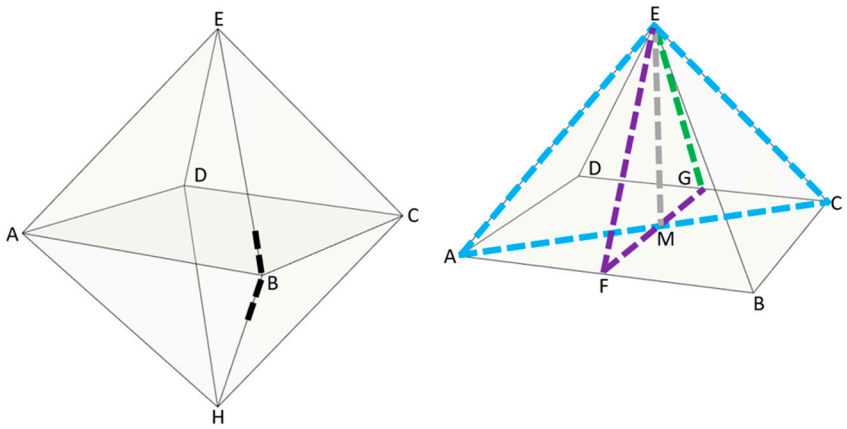
2.1. Calculations Corner Lithography—4 Types of Corners

When etching isotopically, the etching process can be seen as a sum of infinite point sources etching the surfaces, which makes it a rounding step for concave corners [12]. This means that the etched profile on flat surfaces will remain flat, but a corner will create

a partial cylinder or sphere with a radius equal to the etching thickness, as previously demonstrated [5,6]. By combining the initially deposited layer thickness and the etching time, the width of the remaining material or masking layer in the corner can be controlled.

2.1.1. Edges and Vertices

When looking at a basic octahedron, which is defined by the crystalline {111} planes of the Si crystalline lattice (Figure 4), there are two types of corners. *Edges* are the lines where two planes meet, and *vertices* are the points where two or more edges, or 3 or more planes, meet. For an octahedron, all 12 edges have the same angled symmetry, as do the six vertices when the vertices have a smaller angle between opposite planes than at the edges. This means that when an inside-deposited material would be etched from the inside, it takes longer to etch all the material from the vertices than the edges. This allows for several levels of control in corner lithography over selectively addressing corners, as demonstrated by previous work [5,6]. By halving the octahedron, a pyramid is obtained, as shown in Figure 4b. This adds sharper edges and vertices at its base, allowing for a selective corner control of four stages.



(**a**) (**b**)

Figure 4. (**a**) Octahedron as formed by {111} planes in Si. The angle indicated by the black dotted line is, by definition, 90°. (**b**) A pyramid cut from an octahedron. The coloured lines indicate different cross-sections of the pyramid.

2.1.2. Pyramid

A pyramid can be acquired in Si by etching with potassium hydroxide (KOH) through a hole in a SiO_2 hard-mask, resulting in an inverted pyramid (which will be demonstrated in Section 3.2). When looking at the corners of such a pyramid as indicated in Figure 4b, by definition, the corner A, or $\angle EAC$, is 45°. Assuming the pyramid base has a unity width of 1, the total length from A to C, or $\overleftrightarrow{AC}$, is $\sqrt{2}$. From this, it follows that the height of the pyramid $\overleftrightarrow{EM}$ is equal to $\frac{1}{\sqrt{2}}$. The corner F, or $\angle EFG$, is then found by taking the tangent of the purple-grey triangle formed by ΔFEM and is 54.74°. The corner E, or $\angle$GEF, can then simply be found by taking twice $\angle$FEM, which is equal to 70.53°.

The full geometrical derivations of this and the coming section can be found in Supplementary Materials Section S1.

2.1.3. First Corner: Edge A–E, 109.47°

Now, assume conformal deposition where the inside of the pyramid is covered with a layer of thickness t. If you then take a diagonal cross-section over the blue dashed line or through A, C and E, forming ΔACE, the distance from the inside edge of the deposited

layer to the corresponding edge $\overleftrightarrow{AE}$ of the pyramid has a longer distance than the deposited layer thickness, as is illustrated in Figure 5.

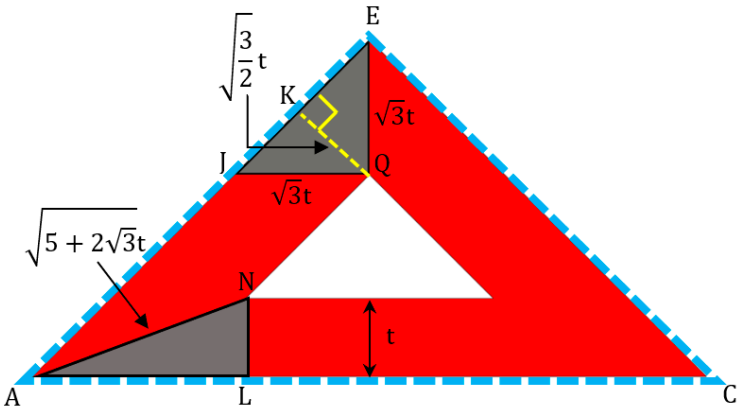


Figure 5. Cross-section of the pyramid over the blue dashed line or through A, C, and E. The grey triangles ΔEQJ and ΔALN are used to calculate the lengths and ratios between the edges.

From here on, the following definitions are used regarding the etching factor (EF) and geometric factor (GF). The EF is defined by the etching distance divided by the deposition thickness of the deposited layer. The GF is the maximum EF needed to completely etch the masking material from a corner.

The total GF from the apex of the pyramid down to the inside top corner of the deposited layer is $\sqrt{3}\,t$, as is shown in the next section. For determining the GF for the $\overleftrightarrow{AE}$ edge, a cross-section through the blue triangle ΔAEC is taken, as shown in Figure 5. When looking at the grey triangle ΔEQJ, the GF is given by the diagonal $\overleftrightarrow{QK}$ perpendicular to the outside edge EJ. The total etching distance or the GF for this edge is given by:

$$\overleftrightarrow{QK} = \sqrt{\frac{3}{2}}t = 1.22\,t \tag{1}$$

The full derivation can be found in Supplementary Materials Section S1.2.

2.1.4. Extra Corner

In theory, when a rectangular base is used instead of a square one, resulting in a hip roof-like structure, the tips of the roof where three planes and edges meet would be slightly sharper than the previously mentioned edge. However, the GF would be only 0.046 longer, resulting in a difference that, in practice, often cannot be effectively used and is not relevant for the process described here. Thus, we do not take it into consideration here. More information about this can be found in Supplementary Materials Section S2.

2.1.5. Second Corner: Vertex E, 70.53°

The next sharpest corner is the centre vertex, or apex of the pyramid $\angle GEF$. To find its GF, a cross-section over the green and purple dashed lines is taken, forming ΔEFG, as shown in Figure 6. Considering the grey triangle ΔEQR, the GF for the apex of the pyramid is given by:

$$\overleftrightarrow{EQ} = \sqrt{3}\,t = 1.73\,t \tag{2}$$

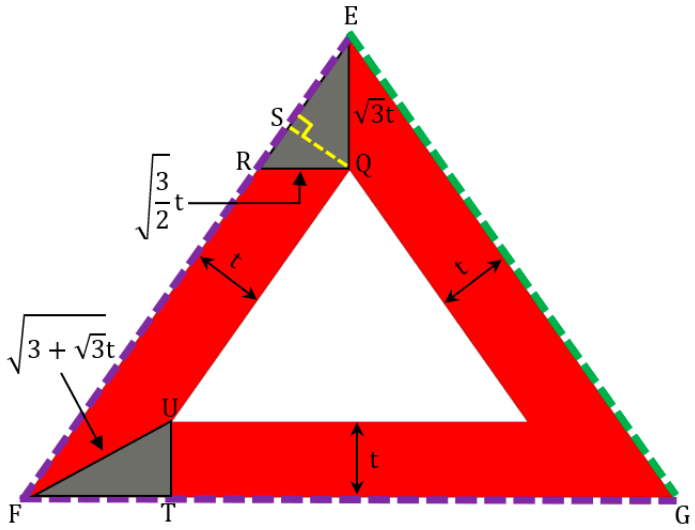


Figure 6. Cross-section of the pyramid over the green and purple dashed line or through F, E and G. The grey triangles ΔEQR and ΔTUF are used to calculate the lengths and ratios between the edges.

The full derivation can be found in Supplementary Materials Section S1.3. Everything up to here has already been demonstrated before within the group [5,6].

2.1.6. Third Corner: Edge A–B, 54.74°

The next sharpest corner is the edge at the base of the pyramid, with the angle at $\overleftrightarrow{AB}$ given by *F* or $\angle EFG$. The etching distance for this edge is given by the hypotenuse $\overleftrightarrow{FU}$ of ΔTUF, as can be seen in Figure 6. The GF for this edge is given by:

$$\overleftrightarrow{FU} = \sqrt{3+\sqrt{3}}\, t = 2.18\, t \tag{3}$$

The full derivation can be found in Supplementary Materials Section S1.4.

2.1.7. Fourth Corner: Vertex A, 45°

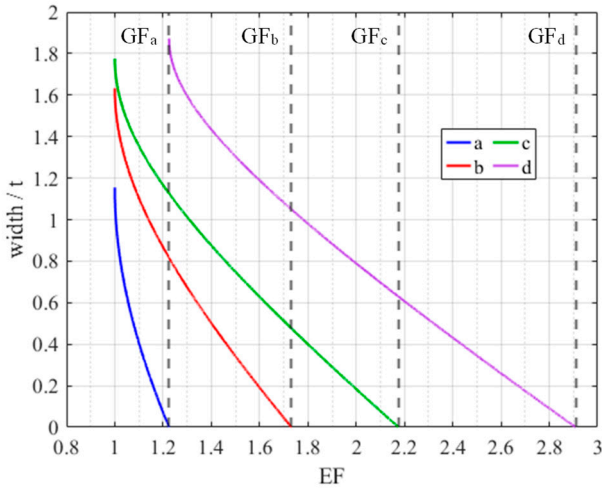
The last remaining and sharpest corners are the vertices at the base of the pyramid $\angle EAC$ (Figure 5). The etching distance for this corner is given by the hypotenuse $\overleftrightarrow{AN}$ in ΔALN. The GF for this vertex is given by:

$$\overleftrightarrow{AN} = \sqrt{5+2\sqrt{3}}\, t = 2.91\, t \tag{4}$$

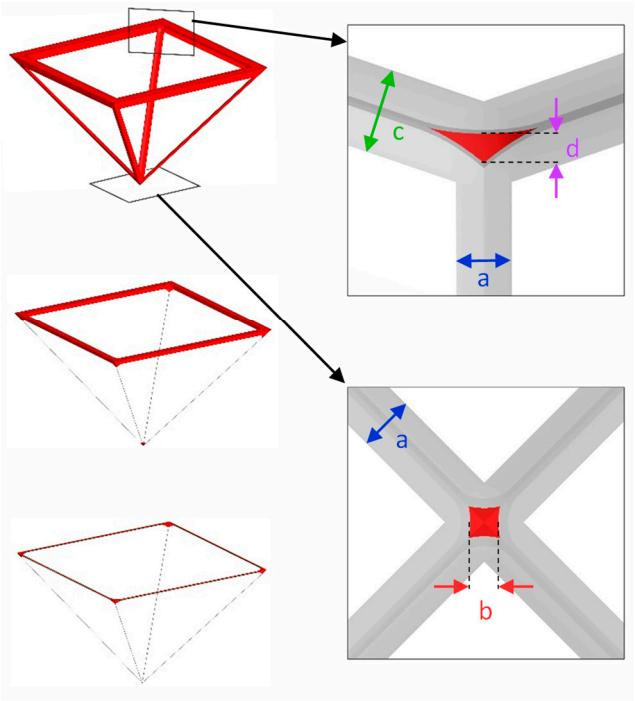
The full derivation can be found in Supplementary Materials Section S1.5. The summary of the different corners and their respective geometric factor can be found in Table 1. Figure 7 shows the width/t vs. the EF for the various edges and corners that are described here.

Table 1. Overview of the corner types and corresponding geometric factor. The letters in the Corner column correspond to those in Figure 7.

Corner		Type	Geometric Factor (GF)
$\overleftrightarrow{AE}$	(a)	Edge	$\sqrt{3/2} = 1.22$
$\angle GEF$	(b)	Vertex	$\sqrt{3} = 1.73$
$\overleftrightarrow{AB}$	(c)	Edge	$\sqrt{3+\sqrt{3}} = 2.18$
$\angle EAC$	(d)	Vertex	$\sqrt{5+2\sqrt{3}} = 2.91$



(**a**)



(**b**)

Figure 7. (**a**) Feature width relative to the deposited layer thickness t vs. the etching factor EF. (**b**) The etched Si_3N_4 frame with on the right the views from inside to the apex perpendicular to its centre.

The used formulae for calculating the width can be found in the Supplementary Materials.

3. Fabrication

3.1. Ingredients

The etching ingredients commonly used to fabricate fractals by means of corner lithography and wet-chemical etching are given in Table 2. The commonly used structural masking layer is stoichiometric silicon nitride (Si_3N_4), which is conformally deposited by means of low-pressure chemical vapour deposition (LPCVD). Si_3N_4 on top of Si substrate can be isotropically and selectively etched in hydrofluoric acid (HF). When Si_3N_4 is used as an inversion masking mask in the LOCOS step, hot phosphoric acid (H_3PO_4) is used to etch Si_3N_4 isotropically and selectively with respect to thermal SiO_2 and Si.

Table 2. Qualitative, relative etching characteristics of used materials in used etchants. X stands for not etching or insignificant etch rates.

Etchants	Si_3N_4	SiO_2	Si
20% KOH at 21 °C	X	X	Good
25% TMAH at 70 °C	X	X	Good
85% H3PO4 at 180 °C	Good	Moderate	Low
85% H3PO4 at 160 °C	Good	Moderate	X
85% H3PO4 at 125 °C	Good	Low	X
1% HF at 17 °C	X	Good	X
50% HF at 17 °C	Moderate	Good	X

When SiO_2 is not used as hard-mask, HF is preferred for etching Si_3N_4 because Si remains undisturbed during etching. However, it has been shown that etching with HF affects the shape of the remaining silicon nitride dot after isotropic timed-topped etching of silicon nitride in V-grooves [5]. Etching in 50% HF gives a "cosine shape" at the interface between the etchant and the silicon nitride, while etching in H_3PO_4 leads to an isotropic profile, as expected. This phenomenon is possibly caused by the growth of a thin oxide layer at the interface during LPCVD, which etches faster in 50% HF with respect to silicon nitride [5].

Potassium hydroxide (KOH) at room temperature is used to etch Si to have well-defined features bounded by the Si{111} planes because of the low etch-rate and thus better control. To selectively etch Si in combination of Si_3N_4 or SiO_2, tetramethyl ammonium hydroxide (TMAH) is usually used because of its high selectivity with respect to these hard-masks and higher etch-rate for the Si{111} planes compared to KOH.

3.2. Process Overview

Here, a summarised version of the fabrication is presented. A full detailed description can be found in Section 3.4.

On a <100> silicon wafer, a thick layer of SiO_2 is grown by thermal oxidation. By means of lithography, photoresist with holes are formed on top and then transferred into SiO_2 hard-mask by wet-etching in buffered hydrofluoric acid (BHF) (Figure 8a). The photoresist is then stripped and the inverted pyramids or first generation (G1) of the fractals are etched in the silicon via the holes in the SiO_2 hard-mask in a potassium hydroxide solution (KOH) where the shape is determined by the slow-etching Si{111} planes (Figure 8b,c).

Sequentially, a layer of about 100 nm of Si_3N_4 is conformally deposited by means of low-pressure chemical vapour deposition (LPCVD) (Figure 8d). This is then etched back in phosphoric acid (H3PO4) where the exact etch-time gives full control over the different levels of corner lithography, such as described before and shown in Figure 8e–h. After etching a factor of 2.2 or depth of 220 nm, only the last vertices or Si_3N_4 are still left (Figures 8h and 9a), and a thermal local oxidation (LOCOS) is performed where the Si_3N_4 dots act as a protecting hard-mask against oxidation (Figure 9b).

After the LOCOS, the Si_3N_4 dots are removed in H_3PO_4, allowing access to the Si at the apices (Figure 9c). This Si is then etched using tetramethylammonium hydroxide (TMAH) (Figure 9d,e). Here, TMAH is used instead of KOH, since it has a higher etch-rate for the Si <111> direction while retaining the higher selectivity of Si over SiO_2 to protect the thin SiO_2 on the walls of the inverted pyramids. This etching results in the formation of the second-generation (G2) fractals, as can be seen in Figure 9d–f.

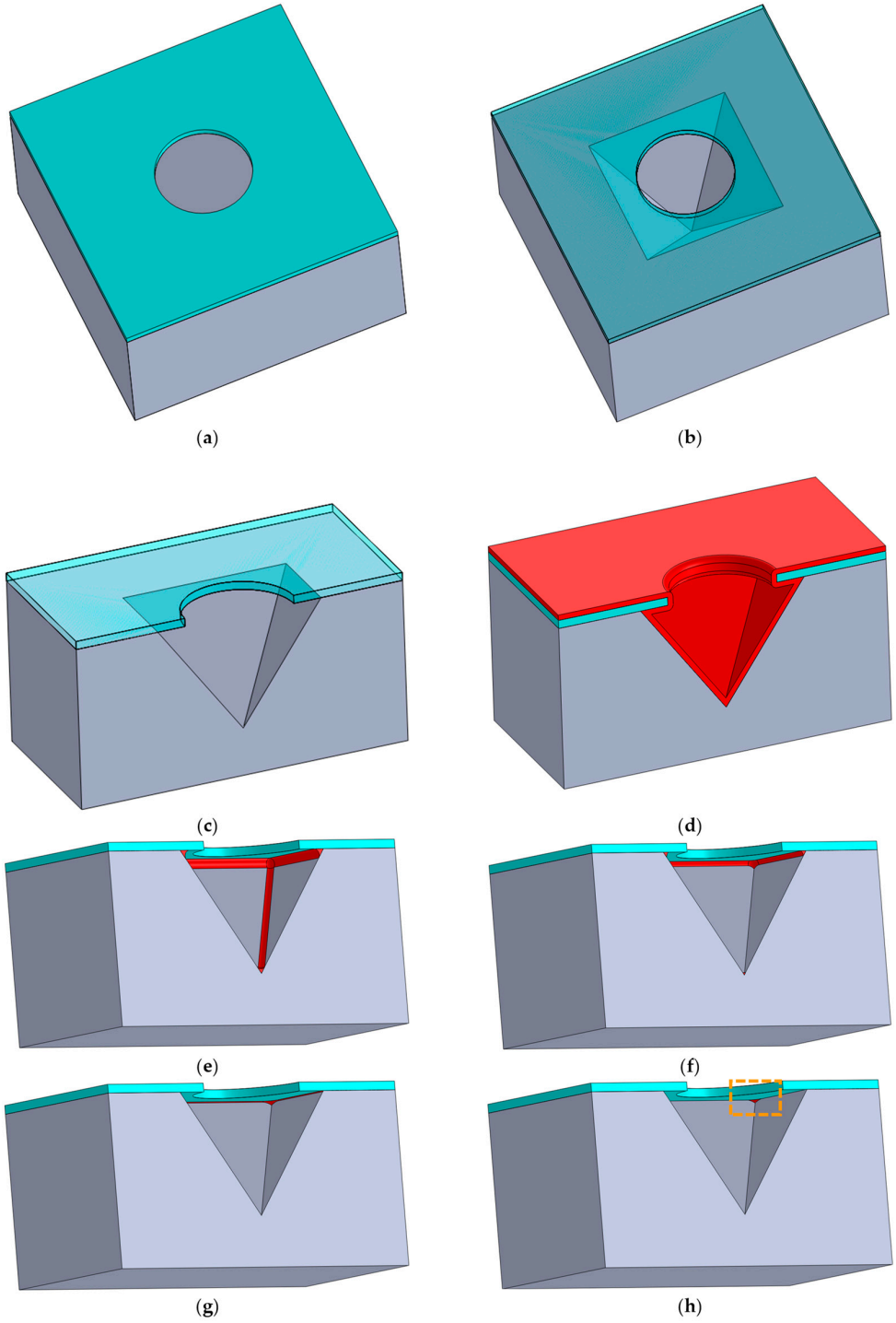


Figure 8. First part of the process flow demonstrating various levels of CL: (**a**) Si (grey) with SiO_2 hard-mask (blue) containing an etched hole. (**b**) Anisotropic etching of an inverted pyramid Si using KOH via the hole in the hard-mask. (**c**–**h**) Cross-sections. (**c**) Etched inverted pyramid. (**d**) Deposition of Si_4N_4 (red) with a thickness t. (**e**) Etching of Si_3N_4 with an etching distance of t or an EF of 1 leaving an Si_3N_4 "wireframe". (**f**) Etching of Si_3N_4 with an EF of 1.35, leaving only a Si_3N_4 "ring" at the base and a nanodot at the apex of the inverted pyramid. (**g**) Etching of Si_3N_4 with an EF of 2, leaving only the Si_3N_4 ring. (**h**) Etching of Si_3N_4 with an EF of 2.2, leaving only nanodots at the vertices of the base of the pyramid. The dashed rectangle indicates the location of the zoom-in of Figure 9.

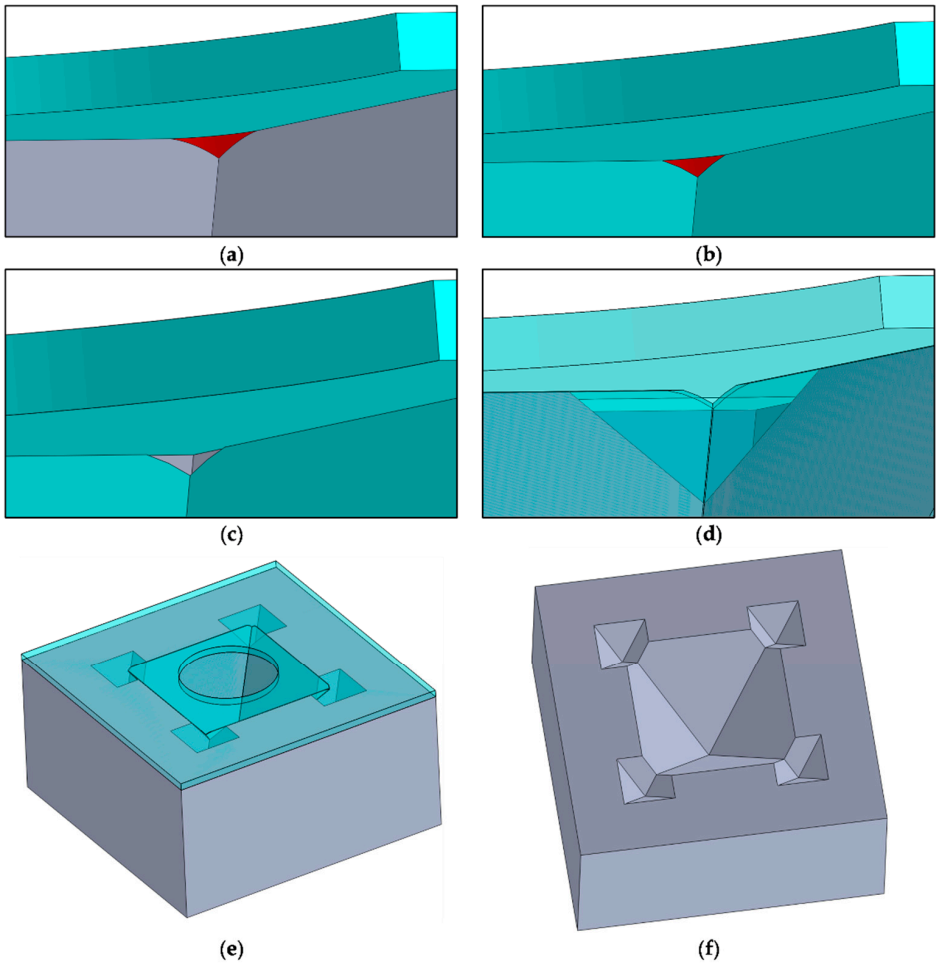


Figure 9. Second part of the process flow demonstrating how to create the G2 fractal: (**a**) Enlarged vertex of the base of the pyramid with Si_3N_4 nanodot (red). (**b**) Vertex with nanodot after LOCOS of the Si (grey). (**c**) Vertex after etching of the nanodot. (**d**) Vertex after etching the Si, creating the G2 fractal. (**e**) Top-view of the G1 and G2 fractal under the SiO_2 (blue) mask. (**f**) Top-view of the G1 and G2 fractal in Si without the planar hard-mask.

For the third generation of fractals (G3), the substrate was cleaned in ozone steam, and the thin SiO_2 layer on the {111} walls of the G1 was stripped in HF. This etching was performed just long enough to remove the SiO_2 on the {111} walls to minimally etch the thick planar SiO_2 hard-mask on top. The process for the formation of G2, as described above, was repeated using an EF of 1.9 for corner lithography.

For the fourth generation of fractals (G4), the process was repeated as described above but while applying corner lithography with an EF of 2.0. After the formation of G4 in TMAH, the substrate was immersed in HF to strip all SiO_2 layers, including the thick planar hard-mask. Subsequently, the substrate was prefurnace-cleaned in ozone steam and dry-oxidised at 1050 °C to grow about 83 nm SiO_2 on Si{111} planes. Finally, the substrate was anodically bonded with a glass wafer, and the silicon was completely etched from the back side in TMAH. The results are thin-walled SiO_2 fractal pyramids on a glass that resemble the ones shown in Figure 3.

3.3. Next Generation Trade-Off

When forming the Si_3N_4 nanodot, there is a trade-off on how big or small the next fractal generation can be. The minimum size and the exact position of the centre of the next generation is determined by the size of the Si_3N_4, dots while the maximum size is determined by the total maximum etching time of the Si in TMAH (also from further

processing) and thus by the thickness of the LOCOS on the {111} planes since this slow-etching SiO_2 mask protects the shape of the previously etched generations. Due to this, generally, a thicker layer of SiO_2 is preferred, but the oxidation of Si results in a layer roughly twice as thick as the consumed Si and thus grows outwards from the Si toward the thick planar SiO_2 hard-mask. Thereby, it can block access to the Si_3N_4 nanodots for etching, so, to allow access, the dots need to be big enough or the LOCOS layer thin enough.

3.4. Process Details

3.4.1. Inverted Pyramid, G1

A <100> Si wafer was thermally wet oxidised with 500 nm of SiO_2 at 1000 °C (120 min—Tempress). By means of lithography (EVG, Olin 907-17, post baked at 120 °C, 30 min), holes were patterned in photoresist and then transferred into the underlying oxide by means of BHF etch (10 min). Inverted pyramids were etched in 25 wt% KOH (75 °C, 10 min—Merck), forming the first generation (G1), followed by RCA-2 cleaning (20 min).

3.4.2. Second Generation, G2

For the second generation, the substrate was prefurnace-cleaned in ozone steam (40 min). Next, 100 nm ± 0.8 nm of Si_3N_4 was deposited in the inverted pyramids by LPCVD (800 °C, 200 mTorr, 22 sccm SiH_2Cl_2, 66 sccm NH_3, 20 min, Tempress). The Si_3N_4 was etched in 85% phosphoric acid (H_3PO_4, 180 °C, 30 min—BASF), i.e., applying corner lithography with an EF of 2.2 or 220 nm, leaving Si_3N_4 only in the apices at the base of the pyramid. A hard-mask on the {111} planes of the G1 pyramid was created by LOCOS using dry oxidation at 900 °C for (90 min—Tempress), creating a layer of 36.3 nm of SiO_2. The formed oxide on top of the Si_3N_4 was then stripped in 1% hydrofluoric acid (HF) (15 s. immersion—Technic). The Si_3N_4 dots were stripped in 85% H_3PO_4 (180 °C, 12 min), and the underlying oxide on top of the Si was etched in 1% HF (15 s). The second-generation (G2) pyramids were then created by anisotropically etching the Si in tetramethyl ammoniumhydroxide (TMAH) (70 °C, 86 min—Merck). The etch rates for Si{100} and Si{111} were 300 nm/min and 13 ± 5 nm/min, respectively. The etch rate of SiO_2 in 25% TMAH at 70 °C was determined to be 0.03 nm/min.

3.4.3. Third Generation, G3

For the third generation (G3) of fractals, the substrate was prefurnace-cleaned in ozone steam (40 min.) Next, the substrate was etched in 1% HF (room temperature, 5 min) to strip SiO_2 completely from the slanted planes of the G2 fractals. Hereafter, corner lithography of Si_3N_4 was carried out with an EF of 1.9 in 85% H_3PO_4 (125 °C, 221 min). The etch-rate of Si_3N_4 and SiO_2 was determined to be 0.80–0.88 nm/min and 0.02 nm/min, respectively. Subsequently, the substrate was prefurnace-cleaned in ozone steam (40 min) and directly transferred to the furnace to perform LOCOS by wet oxidation (900 °C, 1 min). The SiO_2 layer grown on Si{111} and Si{100} was measured (M-2000UI, J.A. Woollam Co., Inc., Lincoln, NE, USA) to be 76.2 ± 1.0 nm and 64.5 ± 1.0 nm, respectively. After LOCOS, the substrate was etched in 1% HF (room temperature, 35 s) to remove the native oxide on top of the Si_3N_4 layer. The etch rate of SiO_2 in 1% HF was determined to be 5.8 nm/min. Next, the remaining Si_3N_4 at the concave corners was etched in 85% H_3PO_4 (125 °C, 84 min), while the slanted planes were protected by SiO_2. The etch rate of Si_3N_4 and SiO_2 in 85% H_3P0_4 solution was determined to be 0.52 nm/min and 0.018 nm/min, respectively, resulting in Si_3N_4/SiO_2 selectivity of about 29. Silicon at the concave corners was exposed for anisotropic etching. Prior to this, the native SiO_2 layer from the Si surface was etched in 1% HF (room temperature, 20 s). The substrate was etched in 25% TMAH (70 °C, 42.5 min.) to form the third-generation fractals at the concave corners of the second generation

3.4.4. Fourth Generation, G4

For the fourth generation (G4) of fractals, the substrate was again prefurnace-cleaned in ozone steam (40 min). The substrate was etched in 1% HF (room temperature, 5 min)

to strip SiO_2 completely from the slanted planes of the previous generation fractals. Next, the substrate was immediately transferred into the furnace to conformally deposit 100 nm ± 0.8 nm Si_3N_4 by means of LPCVD (800 °C, 200 mTorr, 22 sccm SiH_2Cl_2, 66 sccm NH_3, 20 min). Next, corner lithography was carried out to isotropically etch the Si_3N_4 with an EF of 2.0 in 85% H3PO4 (180 °C, 39 min. 20 s). The etch rate of Si_3N_4 was determined to be 5.1 nm/min. Subsequently, the substrate was prefurnace-cleaned in ozone steam (40 min) and directly transferred to the furnace to perform LOCOS by dry oxidation (1100 °C, 4 min). The SiO_2 layer grown on Si{111} and Si{100} was measured (M-2000UI, J.A. Woollam Co., Inc.) to be 25.1 ± 0.3 nm and 22.5 ± 0.3 nm, respectively. After LOCOS, the substrate was etched in 1% HF (room temperature, 30 s) to remove native oxide on top of the Si_3N_4 layer. Next, the remaining Si_3N_4 layer at the concave corners was etched in 85% H3PO4 (125 °C, 120 min), while the slanted planes were protected by SiO_2. The etch rate of Si_3N_4 and SiO_2 in 85% H_3P0_4 solution was determined to be 0.43 nm/min and 0.018 nm/min, respectively, resulting in a Si_3N_4/SiO_2 selectivity of about 24. Silicon at the concave corners was exposed for anisotropic etching. Prior to this, the native SiO_2 layer from the Si surface was etched in 1% HF (room temperature, 20 s). The substrate was etched in 25% TMAH (70 °C, 10 min) to form the G4 fractals at the concave corners of the G3 fractals.

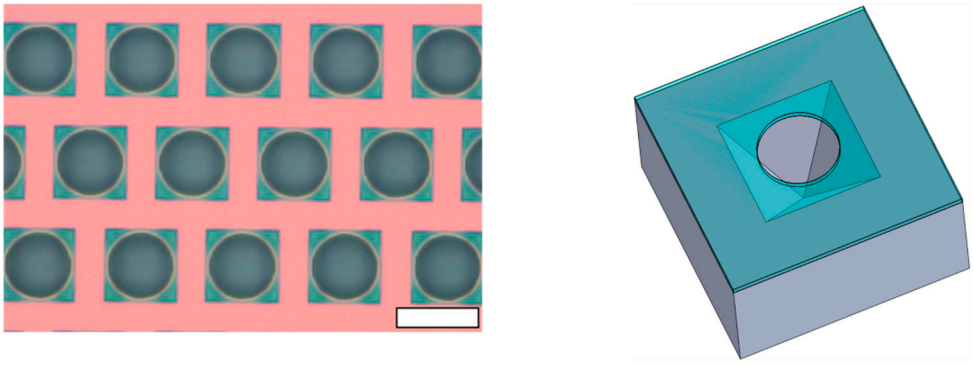
3.4.5. Transfer of Fractals on MEMpax

After the G4 fractal formation, the substrate was etched in 50% HF (room temperature, 60 s) to strip the SiO_2 layer. The substrate was then prefurnace-cleaned in ozone steam (40 min) and directly transferred to the furnace for dry oxidation (1050 °C, 50 min). The grown SiO_2 layer was measured (M-2000UI, J.A. Woollam Co., Inc.) to be 84.4 ± 0.3 nm and 72.8 ± 0.2 nm on Si{111} and Si{100}, respectively. The substrate was anodically bonded with glass substrate (MEMPAX, 500 µm) at 400 °C at 1000V. After anodic bonding, the substrate was etched in BHF to remove SiO_2 from the back side of the silicon wafer. Finally, the silicon from the back side was completely etched in 25% TMAH (90 °C) to obtain SiO_2 fractals bonded on glass.

4. Results and Discussion

4.1. Generation Fractal, G1

The inverted pyramids, or G1 under a SiO_2, were created as described in Section 3. They have a width of about 8 µm and a spacing between them of 3.5 µm or 3.6 µm, depending on the orientation, as can be seen in Figure 10.



(**a**) (**b**)

Figure 10. (**a**) Top-view microscope image of the inverted pyramids etched in Si by anisotropic etching under the SiO_2 hard-mask as shown in the sketch in (**b**) (where the SiO_2 hard-mask is shown in blue). The scale-bar is 10 µm.

4.2. Corner Lithography

Si_3N_4 is conformally deposited in the inverted pyramid and then etched back. As discussed, the inverted pyramid allows for four different levels of control in corner lithography. In Table 3, the multiple stages for corner lithography for only the Si_3N_4 layer under the SiO_2 hard-mask in the Si are illustrated on the left hand, and on the right hand, the corresponding scanning electron microscope (SEM) images from the top on a single corner are shown with the Si_3N_4 frame in the inverted Si pyramid after stripping the SiO_2 hard-mask in BHF. Figure 11 shows the final Si_3N_4 dot under an angle.

Table 3. Left: the etch factor (EF). Middle: sketch of the Si_3N_4 frame under the SiO_2 hard-mask in the Si. Right: top-view SEM images taken from a single corner of the inverted pyramid. The scale-bars are 200 nm.

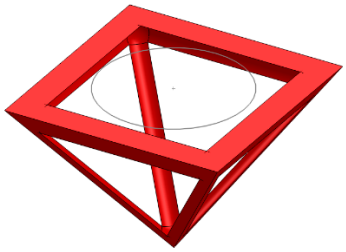
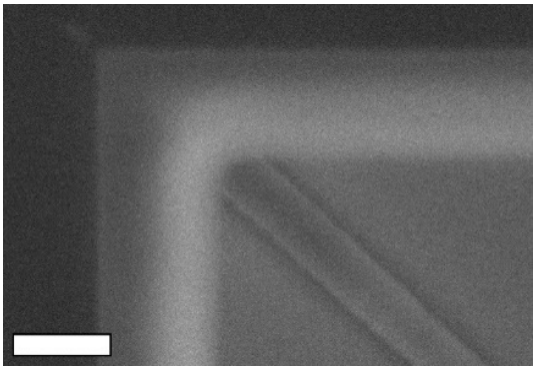
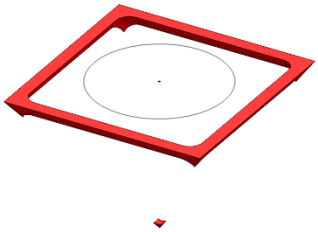
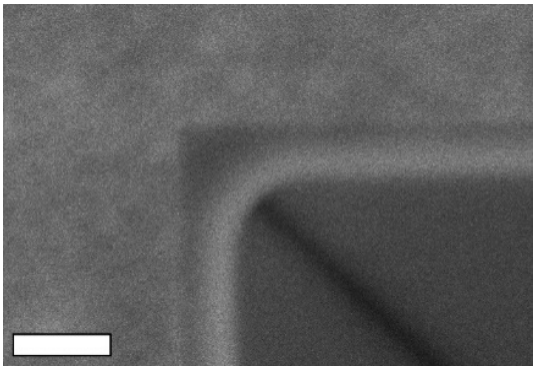
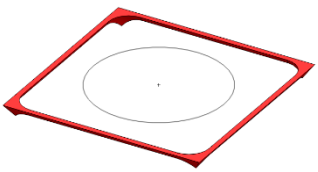
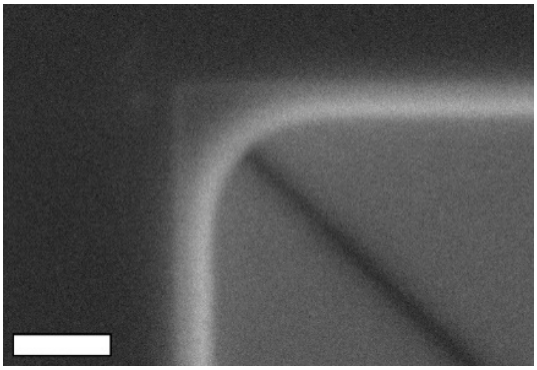
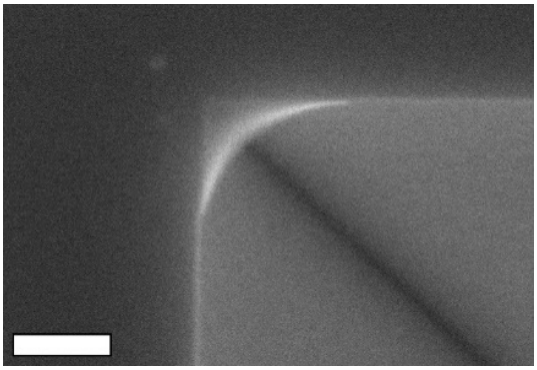
1.0		
1.4		
1.8		

Table 3. *Cont.*

2.2		

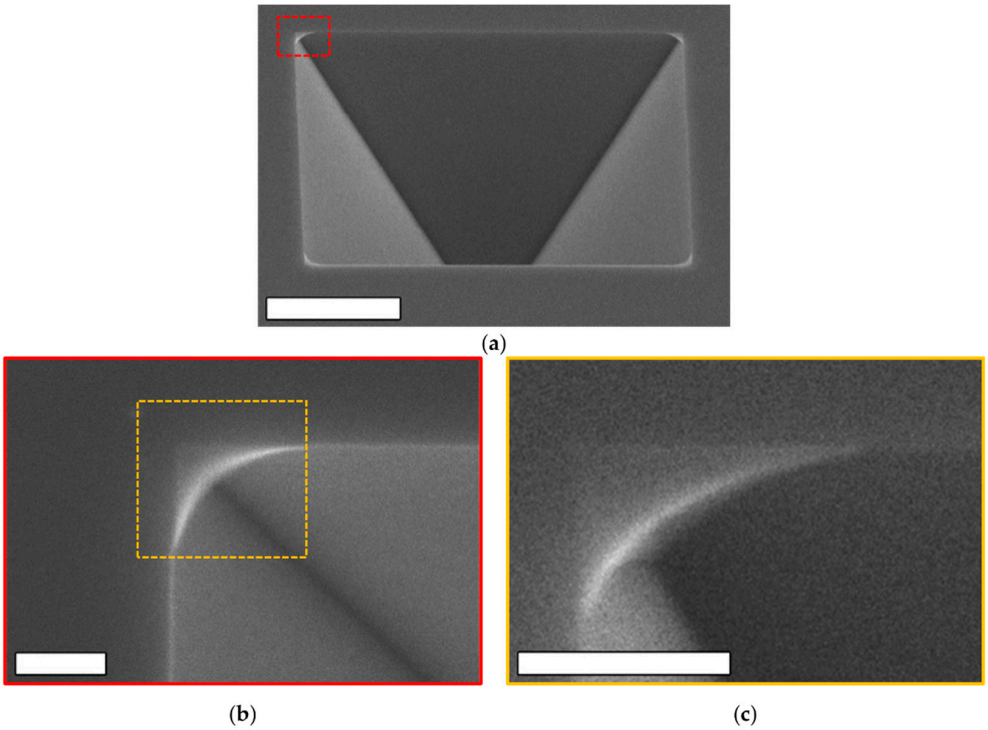


Figure 11. Tilted SEM (**a**–**c**) images of the Si_3N_4 corners of the last stage of the corner lithography. (**b**,**c**) Zoomed-in images at the corner indicated by the dashed rectangles. Scalebars: (**a**) 2 µm and (**b**,**c**) 200 nm.

For all taken SEM images, samples did not have other preparations than the ones mentioned in the text, followed by cleaving the samples for the cross-section images. The images in Table 3, Figures 11–13 were taken using an FEI Sirion HR-SEM, while the images in Figures 14–20 were taken using a JEOL JSM-7610FPlus Field Emission Scanning Electron Microscope. Exact details about the magnification and acceleration voltage for all images can be found in the Supplementary Materials Section S5.

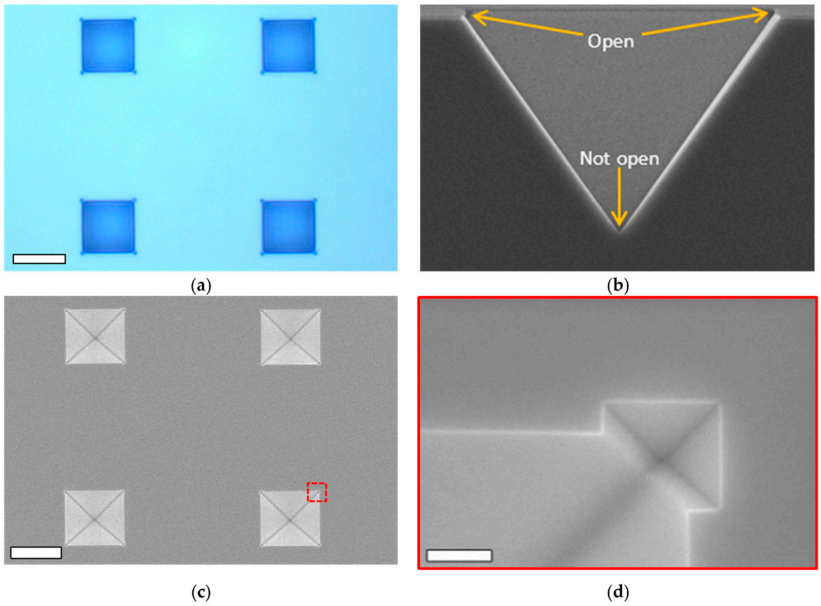


Figure 12. G2 after 5 min of etching in TMAH (25% 70 °C). (**a**) Top-view taken with an optical microscope through the SiO_2 hard-mask. (**b**) SEM image of a cross-section. (**c**) SEM image from the top after stripping the SiO_2 hard-mask in BHF. (**d**) Zoom-in SEM image of the G2 Fractal after stripping the SiO_2 hard-mask in BHF. Enlarged area is indicated in red. Scalebars: (**a**,**c**) 6 µm and (**d**) 200 nm.

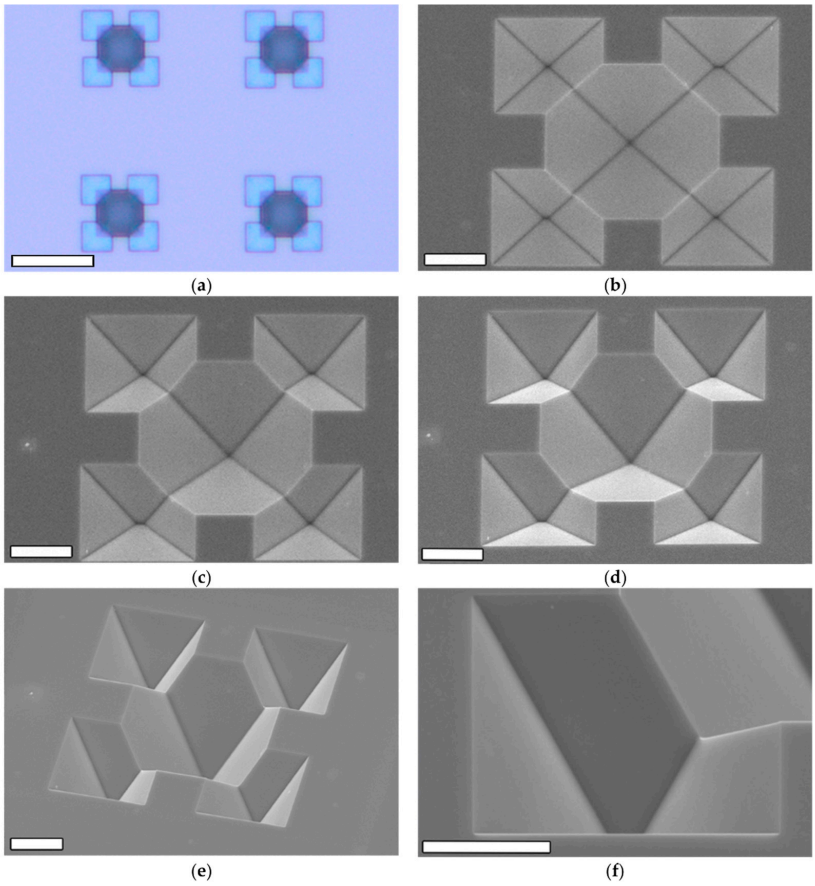


Figure 13. G2 after 125 min of etching in TMAH (25% 70 °C). (**a**) Top-view taken with an optical microscope through the SiO_2 hard-mask. (**b**–**e**) SEM images with a tilt of 0°, 10°, 20°, and 40°, respectively,

with (**e**) also rotated after stripping the SiO_2 hard-mask for taking the images. (**f**) Zoom-in of a G2 of the left bottom corner with a 40° tilt. Scalebars: (**a**) 10 µm and (**b**–**f**) 2 µm.

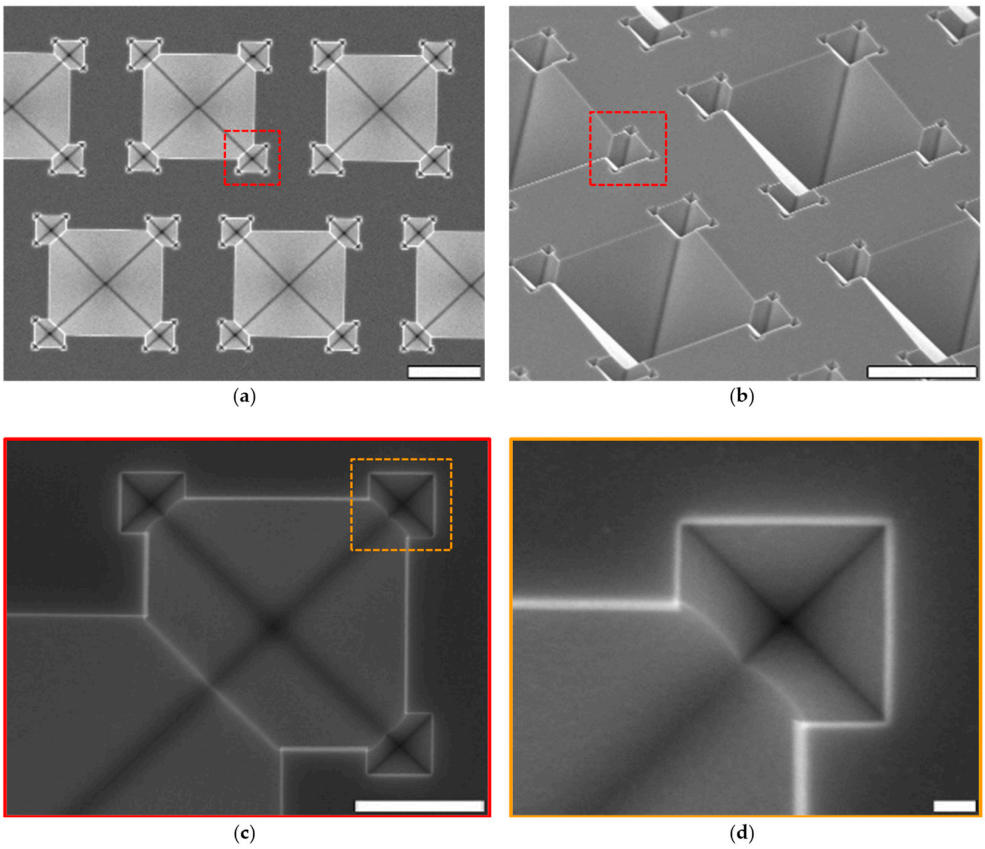


Figure 14. Top-view SEM images (**a**–**d**) of the formation of third generation (G3) fractals after anisotropic etching in TMAH. In (**b**), substrate was 45° tilted. The enlarged areas are indicated by the red and orange dashed lines. Scalebars: (**a**,**b**) 5 µm, (**c**) 1 µm and (**d**) 100 nm.

4.3. Second Generation Fractal, G2

Further processing to fabricate the second generation of fractals was performed as described in the Fabrication section. In Figure 12, the result is shown of a 380 nm wide G2 fractal after etching for 5 min in TMAH (25% 70 °C). It also shows a cross-section showing that only the in-plane vertices were opened and etched through, while the apex of the inverted pyramid was indeed untouched. Before the SEM photography, the SiO_2 hard-mask was removed in BHF, exposing the Si.

Figure 12 also shows the G2 fractal, but after an etching time of 125 min in TMAH (25% 70 °C) creating a square-based flower-like structure with fractals of 5 µm wide. Again, the sample was stripped of the SiO_2 hard-mask in 50% HF before taking the SEM images.

4.4. Third Generation Fractal, G3

The fabrication of the G3 structure was performed as described by repeating the steps for creating the G2 with a width of 2.2 µm. Figure 14 shows the top-view SEM images of the G3 727 nm in width after anisotropic etching of silicon in TMAH and stripping of SiO_2 hard-mask in 50% HF.

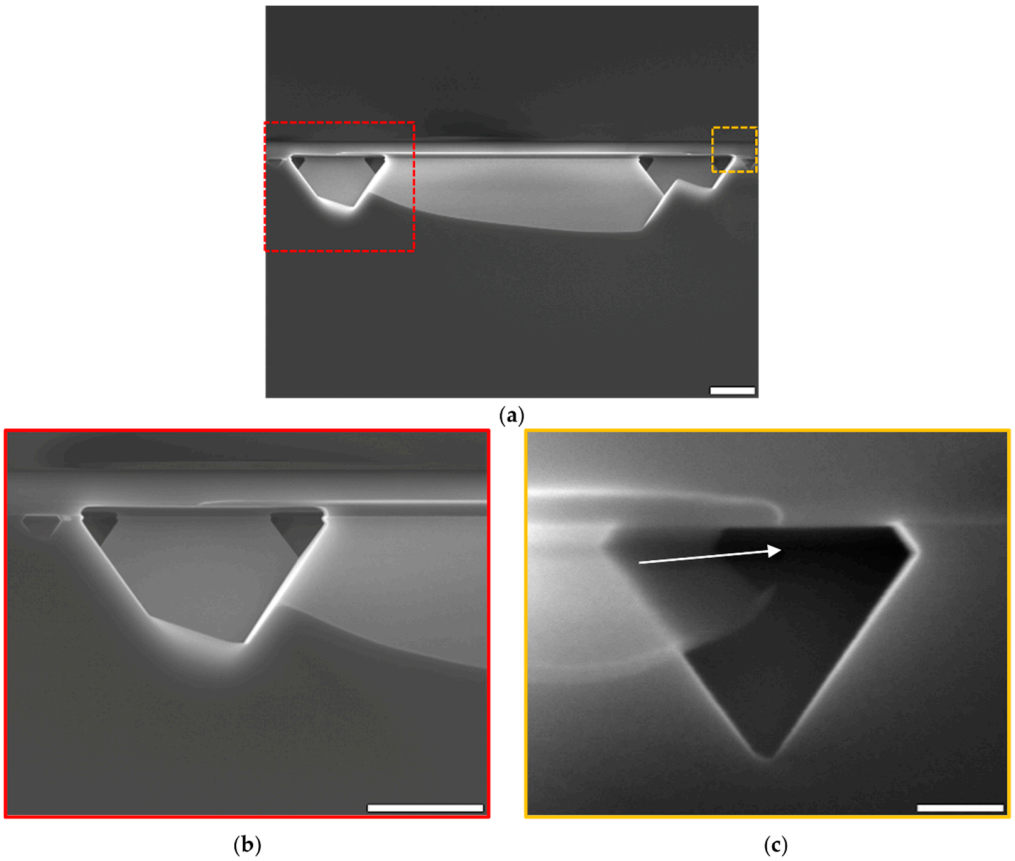


Figure 15. Cross-sectional SEM view of the second (G2), third (G3), and fourth generation (G4) fractals. The cross-section is made by breaking the sample. The diagonal bent lines at the bottom are caused by the break line being not fully parallel to the crystalline lattice for taking the cross-section SEM images. The white arrow in (**c**) indicates in which direction etchants went through the "nozzle" in the apex of the G3 to etch the G4. Enlarged areas are indicated in red and orange dashed lines. Scalebars: (**a**,**b**) 1 µm and (**c**) 100 nm.

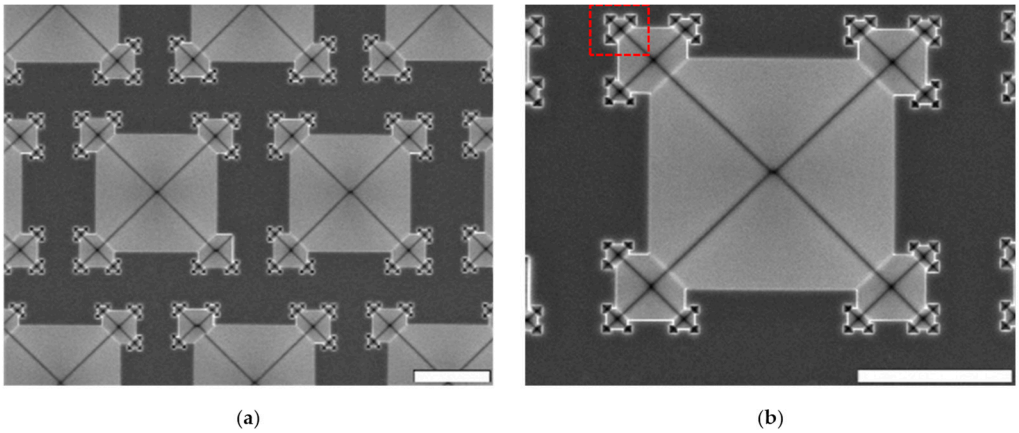
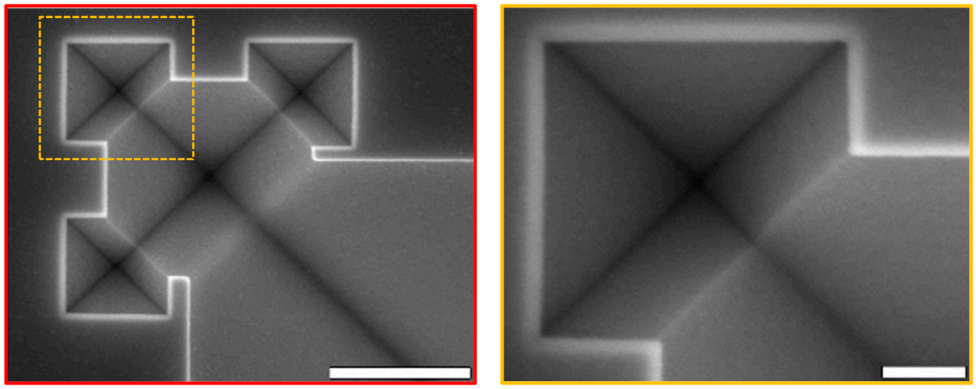
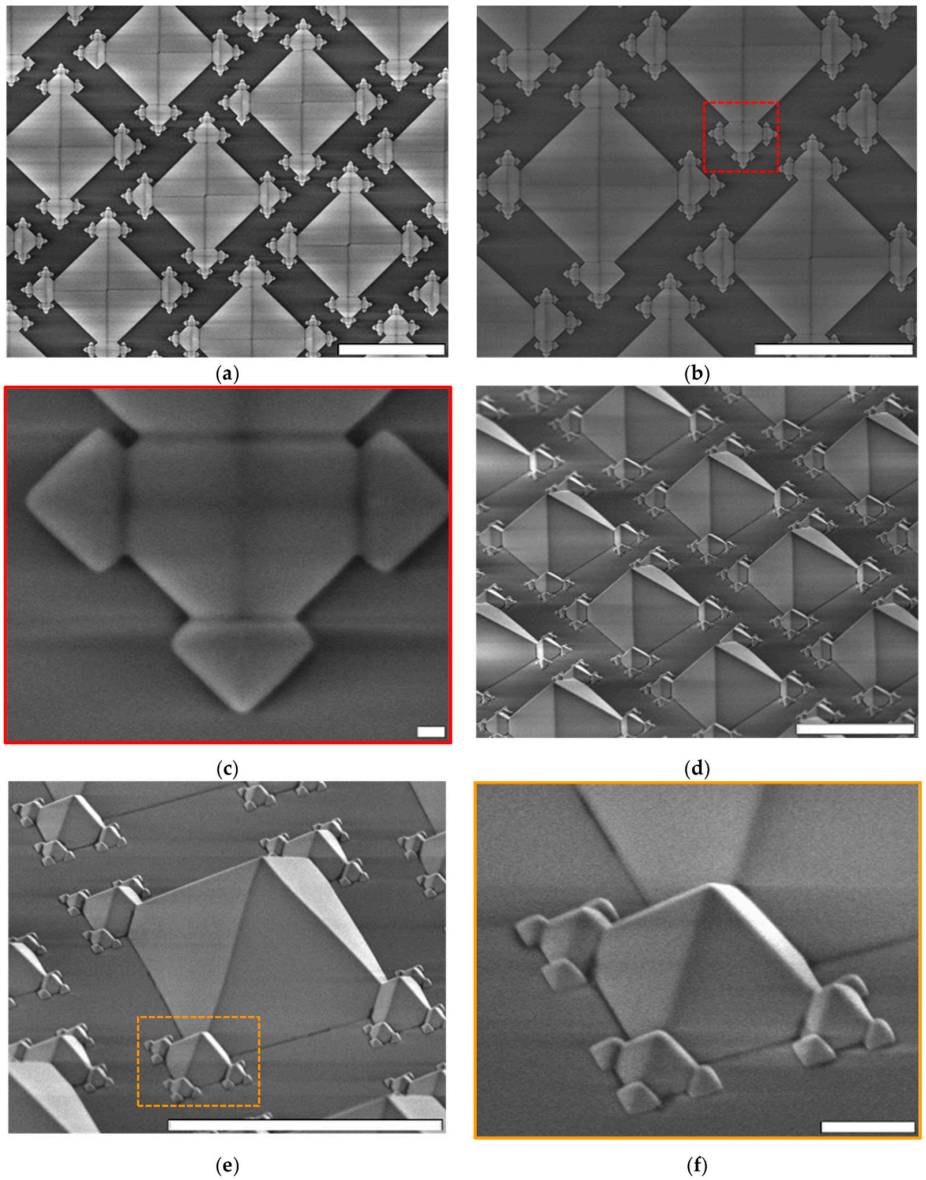


Figure 16. *Cont.*



(**c**) (**d**)

Figure 16. SEM top-view images of the G4 in-plane fractal formation after TMAH and stripping of SiO_2 layer. Enlarged areas are indicated in red and orange dashed lines. Scalebars: (**a**,**b**) 5 µm, (**c**) 500 nm and (**d**) 100 nm.



(**a**) (**b**)

(**c**) (**d**)

(**e**) (**f**)

Figure 17. SEM top-view images (**a**–**f**) of G4 in-plane fractals after final thermal oxidation and anodic bonding and back-side etching in TMAH. (**d**–**f**) Substrate was 45° tilted. Enlarged areas are indicated

in coloured dashed line. The charge-up effect in the SEM image is present due to the nonconductive SiO_2 layer. Enlarged areas are indicated in red and orange dashed lines. Scalebars: (**a**,**b**,**d**,**e**) 10 µm, (**c**) 100 nm and (**f**) 1 µm.

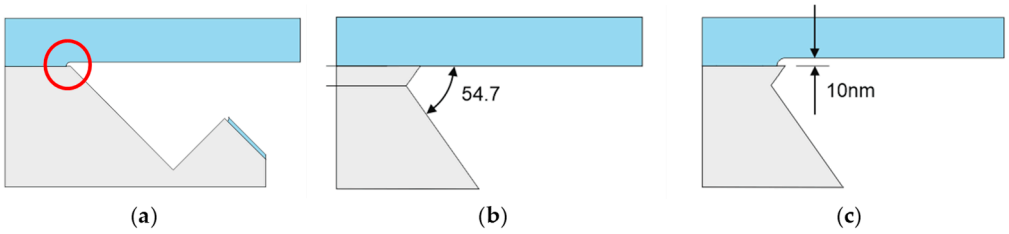


Figure 18. (**a**) Undercutting of the SiO_2 mask (indicated by red circle) after removing the G1 masking layer. (**b**) Formation of extra corner in Si by using TMAH. (**c**) The combined result of both effects.

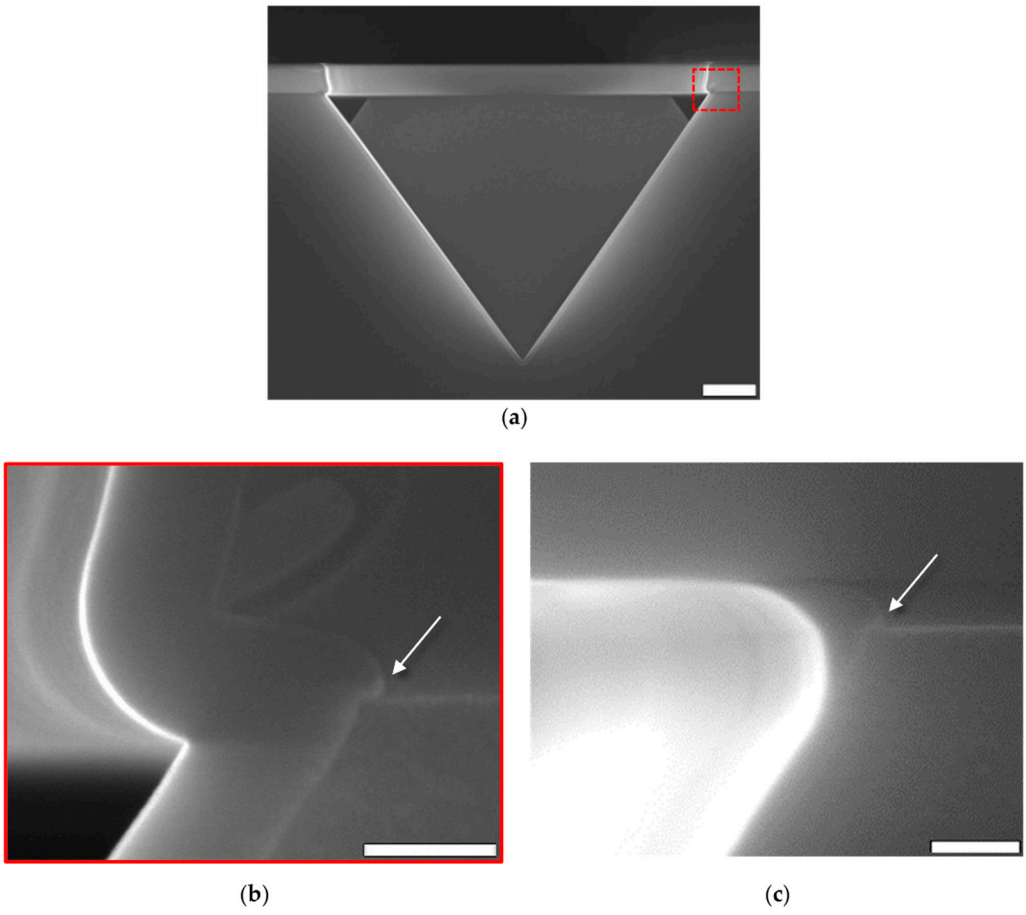
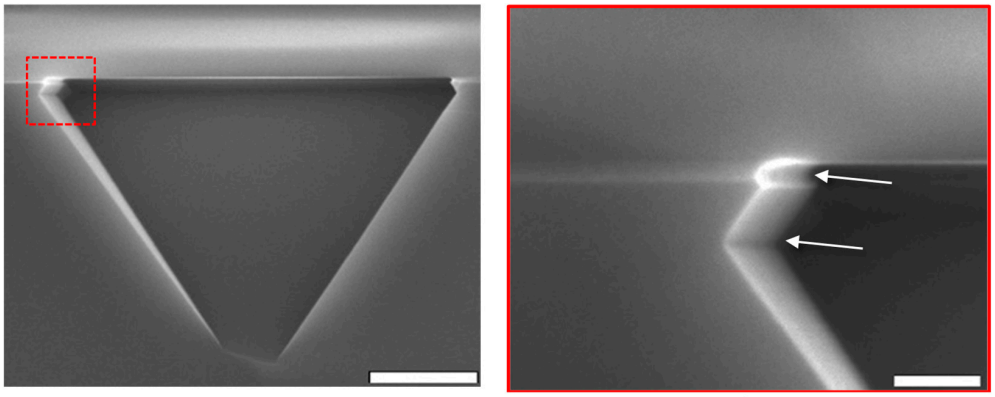


Figure 19. Cross-sectional SEM showing that Si_3N_4 was conformally deposited prior to corner lithography on the G2 (**a**) and (**b**) zoomed section indicated in red also showing the extra etched corners as described. (**c**) is (**b**) after EF of 1.0. The white arrows indicate the undercut of the SiO_2 mask. Scalebars: (**a**) 1 µm and (**b**,**c**) 100 nm.



(**a**) (**b**)

Figure 20. Cross-sectional SEM images showing corner lithography performed with (**a**,**b**) EF 1.9 inside a G3. (**b**) Enlarged zoom-in of the area indicated by the red dashed line. The white arrows indicates the extra corners formed in Si. Scalebars: (**a**) 500 nm and (**b**) 100 nm.

4.5. Fourth Generation Fractal, G4

The fourth generation was created by repeating the steps once more, resulting in a submicron fractal of 386 nm measured from the widest points of the created cavity. A cross-section of the G2, G3 and G4 can be seen in Figure 15. It also shows (the undercut of) the planar SiO_2 hard-mask and, in (c), part of the SiO_2 on the <111> plane of the G3 that form the SiO_2 "nozzle" in the apex. Through this nozzle, the next generation (G4) is etched. The white arrow indicates in which directions the etchant went through the nozzle to etch the G4. Figure 16 shows again the top-view of the inverted pyramids after removal of the SiO_2 hard-mask in 50% HF.

Subsequently, all SiO_2 was stripped in 50% HF, after which everything was dry oxidised. The substrate was then anodically bonded to a glass (MEMpax) wafer, after which all Si of the original substrate was etched in TMAH (25%, 90 °C), leaving only the SiO_2 of the oxidation on top of the MEMpax. The results are hollow SiO_2 fractal pyramids on MEMpax, as can be seen in Figure 17.

4.6. Undercut Mask, Cornered Edges

The attentive reader will have noticed that the final result does not completely resemble the theoretical model due to the etching process. This might be of influence for repeating the process order to create G2, G3 and subsequent fractal structures. If the SiO_2 hard-mask of the G1 pyramid, or any other previous generation, is removed by etching, the original planar top mask will also be partially etched, meaning there is an undercut of the SiO_2, as is illustrated in Figure 18a. Figure 19a,b show the 100 nm Si_3N_4 on the G1 and G2 fractal including the extra etched corners as described. Figure 19c shows the Si_3N_4 after it was etched with an EF of 1. All the corners are still filled with Si_3N_4, while there are none remaining on the Si{111} planes.

After etching the G2 and next generations with TMAH, another side-effect was observed. It was observed that the part of the slope closest to the base of the pyramids does not continue following the <111> direction up to the SiO_2 hard-mask, but goes into the other Si <111> direction, creating a new, less sharp corner and narrow plane with 109.47° and 125.26° corners at the edges instead of the original 54.74° edge, as is illustrated in Figure 18b. The combined effect thus results in a corner significantly different than the expected corners at the bottom of pyramids, as is illustrated Figure 18b.

Figure 20 shows the cross-sectional SEM images corresponding to Figure 18c. Since, at this scale, the extra edges are relatively big compared to the 100 nm of deposited Si_3N_4, it is observed that at an EF of 1.9, all the Si_3N_4 is already etched from the third corner, or $\angle EFG$. In the ideal situation without these extra edges, this would not be fully etched before an EF

of 2.18. However, the apex of the pyramid, $\angle FEG$, is already fully etched at an EF of 1.73, so selective corner lithography on just the third corner would still be possible.

When repeating the steps for creating the G2 to create a G3, these extra corners can prove a problem with the corner lithography when etching very thin layers of Si_3N_4 to go for very small nanodots. The exact details about these corners such as the different EF with which they now would need to be removed and relevance of the thickness of the Si_3N_4 can be found in the Supplementary Materials Section S3. However, when using a relatively thick layer of Si_3N_4 with respect to the dimension of these extra corners, processing can be conducted without any adjustments, and in general, working with a slightly different EF is sufficient to still maintain control over four levels of corner lithography.

4.7. Minimum Size

When producing very small fractals and/or using a relatively thin Si_3N_4 layer for the corner lithography, these added corners will pose a problem. The latter case is also inevitable when going toward very small fractals, since the previous generation will not allow a very thick layer of Si_3N_4 before filling up the connection to the generation before that. Furthermore, to be able to perform corner lithography, the Si_3N_4 dot in the vertex needs to be significantly bigger than the height of the narrow extra plane to still be able to use the sharper base corners. Since the size of this dot also determines the initial starting size for growing the next fractal, this limits the possible minimum size of fractals that can be obtained this way. Realistically, with the fabrication as shown here, the minimum width for the smallest generation would be around 100 nm.

As mentioned before in Section 3.3, there is also a trade-off between the thickness of the LOCOS and the size of the Si_3N_4 dot. Since the SiO_2 protects all already formed fractal generations from the used etchants, it needs to be sufficiently thick, which means the dot needs to be big enough to not be encapsulated. Additionally, for the wafer-scale creation of Si_3N_4 dots in the nanometre range, an extremely high control on conformal precision etching is needed. Combining these factors means that, presently, dots in the order of 10–15 nm can be created. Based on this, realistically, the smallest fractal generations would have a width of 30–40 nm.

4.8. Maximum Size

In addition to minimum size, there is also a limit on the maximum size of the fractals and the total width of the combined generations. Since the fractals have four in-plane growing directions, the maximum size of every next generation is limited by the width of the generation before it. If the edges of the fractal meet during the etching of Si in TMAH, a convex corner of the Si would be exposed. As a result, this direction will etch much faster than the {111} planes and merge the etching fractals, creating a bigger pyramidal cavity over the SiO_2-masked {111} walls of the generation from which it is etched. In practice, this means that every next fractal needs to be at least slightly smaller than its predecessor.

The same limitation for a single next generation also holds for the sum of generations coming from each fractal generation. If every next generation of fractals is small enough not to reach the others of the previous generations, they could still reach each other via the next generation(s) coming from earlier generations, e.g., a 10 μm wide G1 has a G2 set of 8 μm, so 4 μm of space is left between the edges of the G2 before they would touch. However, when the G3 would have a theoretical width of 5 μm, every G3 grown toward an adjacent G2 would reach the G3 grown from that adjacent G2 with a theoretical overlap of 1 μm, thus merging.

5. Conclusions

The creation of an inverted pyramid and in-plane fractal pyramid generations on the vertices was modelled on the bases of using corner lithography. The corner lithography is based on conformal Si_3N_4 deposition and isotropic wet-etching through and under a planar SiO_2 hard-mask and with LOCOS on the uncovered {111} planes of Si.

It was demonstrated that such in-plane fractal replication in Si under a SiO_2 hard-mask can be realised by producing a G1 inverted pyramid that is 8 μm wide. On every in-plane concave corner at the base of the original G1, a G2 fractal pyramid was created with a size of 2.2 μm. This was followed by the next in-plane fractal generation (G3) at the concave corners of the previously newly generated fractal pyramids, with a submicron width of 727 nm wide and, at last, G4 fractal generation of 386 nm wide.

However, some deviations were found at the corners at the base of the pyramids of the G2 and subsequent fractals. Due to the etching of the planar SiO_2 hard-mask during the stripping of the SiO_2 on the {111} planes, an undercut of the planar mask protrudes past the edges of the Si inverted pyramid. This creates an extra cornered edge at the base of the pyramid.

It was also observed that with the formation of the G2 and subsequent fractals, the fractals were not a perfect pyramid anymore. At the base, another corner was formed by the <111> planes going in the reverse direction, effectively creating a narrow plane of two edges under angles of 109.47° and 125.26° instead of the original 54.74° edge. The shape of these fractals is still mostly pyramidal but looks more as if the octahedron was cut in two a little bit past the edge instead of on the edge.

For the fractals formations as shown here, these two extra corners did not prove a problem and they do not present a problem for further replication when using sufficiently thick Si_3N_4 layers for the corner lithography. Additionally, for the shown use-case with Si_3N_4 layer thickness in the same order of magnitude as these corners, they limit the EF window for selectively choosing which corner to use for the next step in corner lithography, but there is still a sufficient range of EF to select the desired step.

Due to these extra corners, there is a limit on the minimum achievable size of a fractal with the current fabrication techniques. Since the Si_3N_4 dot is the initiator of the next generation, that generation will be bigger than this dot, while this dot needs to be significantly bigger than the deviations caused by the extra corners for the corner lithography to work. Furthermore, there is the earlier-mentioned trade-off between the thickness of the LOCOS on the {111} planes as a masking later and the needed size of the Si_3N_4 dot to still be accessible for the etchants. At the moment, our fabrication methods allow us to make fractal generations down to 100 nm when starting with a G1 of several micrometres.

The maximum size of the fractals is limited too, but by the size of the previous generation. In principle, a fractal cannot be bigger than its previous generation since then the etches during the etching will meet, resulting in an even bigger pyramid at the location of the previous generation. This also goes for the sum of multiple generations that can never go wider than any previous generation, since then the latest generations would merge.

By combining all these factors, a theoretical maximum number of generations can be thought of, assuming a starting G1 base of 10 μm and that a next generation will only be half the size of its predecessor. Additionally, taking into account that with the current fabrication the minimum size is limited to about 100 nm, a total of six more generations can be created where the G7 will have a width of 156 nm.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/fractalfract7020202/s1, The supplementary materials contains derivations of the formulae used in the theory section, the effect of mask undercutting, extra corner created by TMAH, and details of SEM parameters used.

Author Contributions: Conceptualisation, J.W.B., L.J.K. and N.R.T.; methodology, J.W.B. and L.J.K.; validation, J.W.B., L.J.K., N.R.T. and Y.P.; formal analysis, J.W.B. and L.J.K.; investigation, J.W.B. and L.J.K.; writing—original draft preparation, J.W.B., L.J.K. and Y.P.; writing—review and editing, J.W.B., L.J.K., N.R.T. and Y.P.; visualisation, J.W.B.; supervision, J.W.B. and N.R.T. All authors have read and agreed to the published version of the manuscript.

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