


Article

An Overview of the CMS High Granularity Calorimeter [†]

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Abstract: Calorimetry at the High Luminosity LHC (HL-LHC) faces many challenges, particularly in the forward direction, such as radiation tolerance and large in-time event pileup. To meet these challenges, the CMS Collaboration is preparing to replace its current endcap calorimeters from the HL-LHC era with a high-granularity calorimeter (HGCAL), featuring an unprecedented transverse and longitudinal segmentation, for both the electromagnetic and hadronic compartments, with 5D information (space–time–energy) read out. The proposed design uses silicon sensors for the electromagnetic section (with fluences above 10^{16} n_{eq}/cm^2) and high-irradiation regions (with fluences above 10^{14} n_{eq}/cm^2) of the hadronic section, while in the low-irradiation regions of the hadronic section, plastic scintillator tiles equipped with on-tile silicon photomultipliers (SiPMs) are used. Full HGCAL will have approximately 6 million silicon sensor channels and about 280 thousand channels of scintillator tiles. This will allow for particle-flow-type calorimetry, where the fine structure of showers can be measured and used to enhance particle identification, energy resolution and pileup rejection. In this overview we present the ideas behind HGCAL, the current status of the project, results of the beam tests and the challenges that lie ahead.

Keywords: front-end electronics for detector readout; radiation-hard electronics; silicon detectors; performance of high-energy physics detectors; data acquisition systems

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1. Introduction

The HL-LHC at CERN will operate at an instantaneous luminosity of 5×10^{34} $\text{cm}^{-2}\text{s}^{-1}$ or higher and is expected to record ten times more data than the LHC. This increase in luminosity will cause detector components to be exposed to extreme radiation levels. Moreover, due to the increased luminosity, we expect up to 200 collisions per bunch crossing, which presents a significant challenge for mitigating overlapping events (pile-up). To address this, the CMS experiment [1,2] will upgrade several components of its detector, including the introduction of a new High-Granularity Calorimeter (HGCAL) [3]. It will replace the current endcap calorimeters. HGCAL must achieve a ~ 30 ps timing resolution to mitigate pile-up and maintain a robust physics performance after an integrated luminosity of 3000 fb^{-1} , where in the innermost region, the total ionizing dose will reach 2 MGy and the total neutron fluence will be 10^{16} n_{eq}/cm^2 .

HGCAL is a high-precision sampling calorimeter composed of silicon and scintillator modules, arranged across 47 active layers with over 6 million channels. In the electromagnetic section, the silicon modules are interleaved with copper, copper–tungsten, and lead absorbers. The silicon sensors are segmented into hexagonal cells, with a cell size of 0.5 cm^2 in the innermost region and 1.2 cm^2 in the outer regions. The hadronic section features silicon sensors in high-radiation areas, while plastic scintillator tiles are used in regions of lower radiation. The hadronic calorimeter is equipped with steel absorbers. To

minimize leakage currents in the silicon sensors and SiPMs, the entire calorimeter is maintained at $-35\text{ }^{\circ}\text{C}$. This highly segmented design enables detailed measurements of both the transverse and longitudinal shower profiles, as well as precise timing information, aiding in pile-up mitigation and enhancing the event reconstruction performance. A schematic representation of HGCAL design in the longitudinal cross section in the upper half of one endcap is shown in Figure 1.

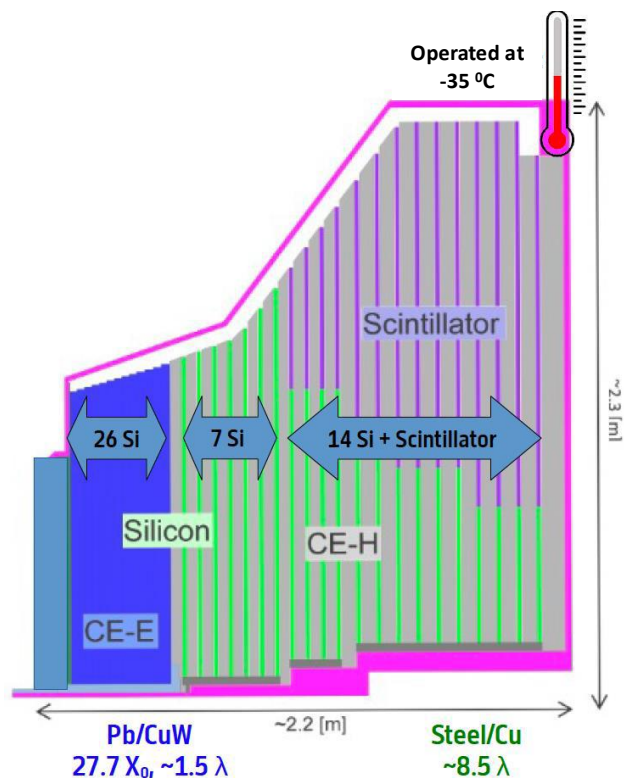


Figure 1. Schematic layout with key parameters of HGCAL design in the longitudinal cross section in the upper half of one endcap.

The total power required for the front-end (FE) electronics is approximately 110 kW per endcap. FE electronics requires 1.2 V for analog and digital, and 2.5 V for optical transmission electronics. The power is fed to the silicon and scintillator modules through FE-printed circuit boards (PCBs) that also host HGCAL application specific integrated circuits (ASICs).

Section 2 describes the active elements. Section 3 gives an overview of the electronics systems and Section 4 outlines the results of the tests performed in the laboratory and with particle beams, and the status of the reconstruction software development.

2. Active Elements

HGCAL is instrumented with two types of active elements: silicon sensors covering an area of 620 m^2 and small plastic scintillator tiles covering an area of 370 m^2 .

2.1. Silicon Sensors and Silicon Modules

The HGCAL silicon sensors are fabricated on 8 inch wafers. They are hexagonal in shape. The choice of the hexagonal geometry is motivated to maximize the use of the circular wafer area. There are three different active silicon sensor thicknesses (120, 200, and $300\text{ }\mu\text{m}$) optimized for regions of different radiation levels. Sensors are segmented into cells and read out individually. The 200 and $300\text{ }\mu\text{m}$ thick sensors contain 192 cells each with $1.2\text{ cm}^2/\text{cell}$, while the $120\text{-}\mu\text{m}$ thick sensors contain 432 cells with $0.5\text{ cm}^2/\text{cell}$. The

physically thinned p-type float zone silicon wafers are the line substrate material for the 200 and 300 μm thick sensors, while P-type epitaxial wafer is the line substrate material for the 120- μm sensors. A comprehensive irradiation campaign was performed to optimize sensor design choices and parameters [4–9].

There are four components in a silicon module: a PCB with embedded electronics, a silicon sensor, a Kapton isolating foil, and a baseplate for mechanical support. HGAL will have about 26,000 silicon modules. Six module assembly centres (MACs) will be responsible for their assembly. Each MAC will be able to produce up to 24 modules per day. The assembly and testing procedures are being established at the MACs [10].

2.2. Scintillators and Scintillator Tile Modules

Two types of scintillator material are considered for the hadronic section: polyvinyltoluene-based (PVT) and polystyrene-based (PS). Based on cost, performance, and ease of assembly, the cast and machined PVT-based scintillators will be used in the front, and injection molded PS-based scintillators will be used for the rest of the hadronic section.

The SiPM-on-tile technology, pioneered by the CALICE Collaboration [11,12], is identified as the most cost-effective solution. This technology utilizes direct detection of light from the scintillator tile by a SiPM that collects the light through a dimple in the surface of the tile. The dimple equalizes the response across the tile, and reflective wrapping maximizes light collection. The hadronic section contains 280,000 channels with tile sizes from 4 to 30 cm^2 , and the SiPM area ranges from 2 to 4 mm^2 .

3. Electronics Overview

The HGAL readout, trigger, and control system uses a combination of custom and commercial parts. Some of the custom parts are specific to HGAL, and some are common in other CERN projects.

3.1. Front-End Electronics

FE electronics digitizes the silicon sensor and SiPM signals, provides a high-precision time-of-arrival measurement, and transmits the digitized data to the data acquisition (DAQ) back-end (BE) electronics. It also computes, for every bunch crossing, the digital sums of neighbouring cells (2×2 cells in the case of the 1.2 cm^2 silicon pads and 3×3 cells in the case of the 0.5 cm^2 silicon pads) to build trigger primitives. The custom HGAL Readout Chip (HGCROC) measures the charge and time-of-arrival at 40 MHz. The HGCROC requirements are extremely challenging: a high dynamic range from a few fC to 10 pC, low noise of about 2000 electrons, high precision timing information of 30 ps for pileup mitigation, and low power consumption of 15 mW/channel. HGCROC will also face a harsh radiation environment, up to 300 MRad. HGCROC has 72 channels of analog low noise and high gain preamplifier and shapers, and a 10-bit 40 MHz successive-approximation analog-to-digital converter (SAR ADC), which provides the charge measurement over the linear range of the preamplifier. In the saturation range of the preamplifier, a discriminator and time-to-digital converter (TDC) provide the charge information over a 200 ns dynamic range using 50 ps binning. A fast discriminator and TDC provide timing information to 25 ps precision. Both charge and timing information are kept in a memory waiting for a Level1-accept (L1A). At a bunch crossing rate of 40 MHz, data corresponding to (4 or 9) adjacent channels are sent out to participate in the generation of trigger primitives. As part of the ongoing development and testing of HGAL electronics, the performance of the HGCROC prototype in terms of the signal-over-noise ratio, charge, and timing, as well as radiation qualification with total ionizing dose, and single-event effects, has been studied [13]. The data are transmitted to the custom concentrator ASIC, ECON-D via

1.28 Gb/s electrical links where they are zero suppressed. Digital sums of 4 or 9 adjacent channels (depending on the sensor granularity) are computed by HGCROC. These sums are transmitted for every bunch crossing from the HGCROC to a different custom concentrator ASIC, ECON-T, via separate 1.28 Gb/s electrical links to be used for the formation of trigger primitives. The ECON-D aggregates, formats, and serialises the data at the L1 average frequency of up to 750 kHz. For the trigger path, ECON-T selects the trigger sums of interest, aggregates and formats their data in packets, and stores them in a First-in-First-out (FIFO) buffer. These data are sent within a defined latency to the trigger primitive generator (TPG) electronics, using separate optical links. Therefore, ECON-D and ECON-T act as hubs, receiving up to 12 1.28 Gb/s electrical links from the HGCROCs and serializing the corresponding data, trigger and L1A readout, and outputs at the same rate. They are connected to the BE electronics via a bi-directional link using low-power gigabit transceivers (lpGBTs) and are coupled to a slow control adapter ASIC (SCA) [14] and versatile transceiver plus (VTRx+) [15]—all three developed for HEP experiments. The fast control links will run at 320 Mb/s and the slow control links will use the I²C protocol at 1 Mb/s. The optical transmission is performed through VTRx+ optoelectronics transceivers.

The PCB layouts for the FE electronics were optimized for the board shapes and the number of optical links, as required by the data rates. For high-density silicon modules, the ECONs are mounted directly on one PCB, the Wagon board, while the lpGBTs and VTRx+ are located on a different PCB, the Engine board. In contrast, for silicon low-density modules, ECONs are mounted on mezzanine boards, separate from the Wagon board. For scintillator modules, the ECONs, lpGBT, and VTRx+ components are all mounted on the same motherboard. The Wagon boards are connected to the Engine boards with miniature connectors [16,17]. The lpGBTs use the forward error correction (FEC5) protocol [18] for the data path. The total average data volume for the whole HGCAL is around 2.5 MByte per event, which scales approximately linearly with the average pileup. At an L1A rate of 750 kHz, this corresponds to an average data rate from the FE electronics of 15 Tb/s. For the trigger path, the total average rate of trigger cell data will be 1.25 Mbit per bunch crossing, or 50 Tb/s. The total number of 10.24 Gb/s lpGBT links from FE electronics is about 10,000 for both DAQ, and TPG BE electronics. A schematic representation of the HGCAL FE readout, trigger, and control chain is shown in Figure 2.

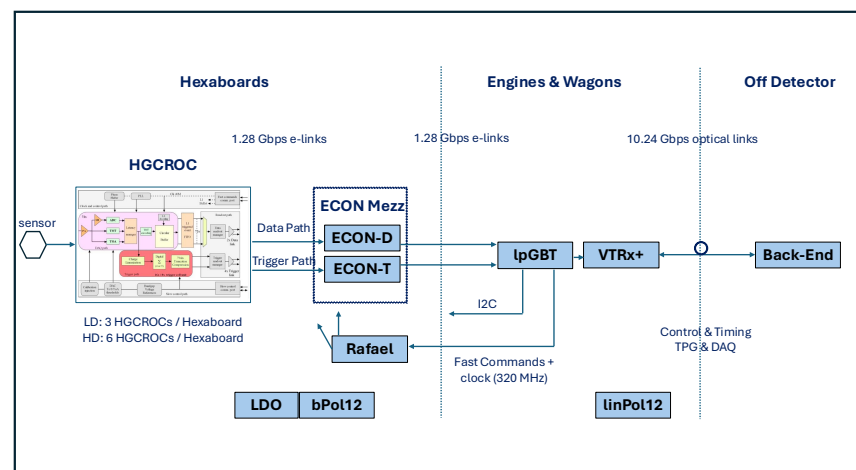


Figure 2. Schematic representation and key components of the CMS HGCAL FE readout, trigger, and control chain.

3.2. Back-End Electronics

BE electronics consist of the DAQ and TPG systems, which are implemented in the advanced telecommunications computing architecture (ATCA) [19] format. The systems

consist of common CMS ‘Serenity’ boards [20] housed in ATCA crates, with DAQ and timing hub (DTH) ATCA boards [21] also in these crates so as to provide the central DAQ and timing systems interface. The DAQ system consists of ATCA boards containing one high-end Field Programmable Gate Array (FPGA) with sufficient bandwidth to drive 108 links in both directions to and from FE electronics, and a further 12 optical links to and from a DTH in the same crate. The links from and to the FE electronics will run at 10.24 Gb/s and 2.56 Gb/s, respectively. The links to the DTH board will run at 25 Gb/s. The FPGA on these boards will handle and process the data, with the required buffering, event building, front-end emulation, and monitoring implemented in firmware. The TPG system has two tasks: to form 3D clusters from trigger cells, and to form the overall energy map from the coarse granularity HGCROC energy sums.

3.3. Control and Safety Systems

The HGCAL detector control system (DCS) is the main interface to turn HGCAL on and off in a safe and controlled fashion and it provides all status information (power system, cooling system, gas system, temperature, etc.). It is based on the supervisory control and data acquisition chosen at LHC. The HGCAL detector safety system (DSS) is based on industrial programmable logical controllers (PLCs) [22]. HGCAL DSS will constantly monitor the temperature and humidity inside the HGCAL volume, including the interfaces, and will have access to all status information of the CO₂ cooling and dry gas system. Passive temperature sensors inside the HGCAL cryostat will be directly connected to the PLCs. A dedicated sniffer system will pump gas from the volumes via several pipes towards the service cavern, where the gas is analyzed by commercial high-precision dew-point meters.

4. The Beam Tests Results and System Validation

The validation of the HGCAL system has been ongoing with measurements in the laboratories using particle beams. Major test campaigns have taken place since 2018. A large system consisting of an electromagnetic and a hadronic section made of multiple layers of silicon modules equipped with HGCROC early prototypes, complemented by a section of SiPM-on-tile prototypes were used in 2018. In 2021, prototype 8 inch modules were tested for the first time. In 2023, the full readout chain was implemented with a small system. All campaigns were carried out at beamline facilities at CERN with high-purity electron and pion beams of energy ranging from 20 to 300 GeV.

The 2018 campaign focused on the performance of the prototype electronics, shown in Figure 3. The stability of noise and pedestals, calibration with MIPs, as well as timing, energy linearity, and resolution for electrons and pions were examined. The energy response of the electromagnetic section was found to be linear within $\pm 1.5\%$ for electron beams above 50 GeV, and its resolution is within the physics target. The timing resolution measured with electromagnetic showers is within 30 ps and improves to 16 ps at higher energies. The performance of the hadronic section also meets the physics target. The description of the systems and results of the tests with particle beams can be found in [10,23–28].

The 2023 campaign focused on validation of data transmission, quality, and system stability over near final readout chain elements. Both trigger and DAQ paths were employed at 100 kHz for days, and the data quality was monitored. This represents a major milestone as this was the first full vertical system integration in a test beam. The test beam data were also used to validate the 3D clustering algorithm of the HGCAL particle reconstruction framework [29].

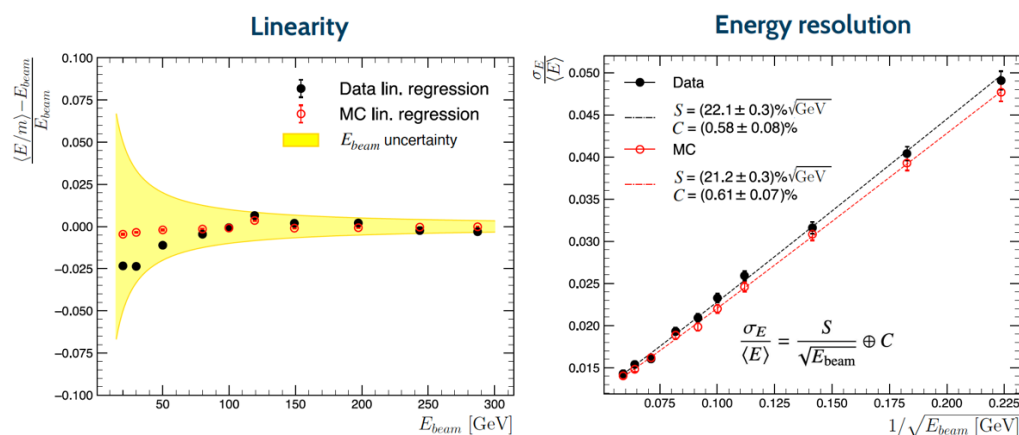


Figure 3. Energy linearity (left) and resolution (right) as a function of incoming electron beam energy measured in 2018 campaign.

5. Conclusions

The CMS endcap calorimeters will be replaced with a high-granularity calorimeter equipped with silicon sensors and highly segmented scintillators. The readout, trigger, and control chains use state-of-art electronics developed for HGCAL and other CMS upgrade projects. The HGCAL electronics design has been evolving with feedback from benchtop and beam tests. A reconstruction framework is being developed to fully exploit the exceptional granularity and precision timing. System integration and validation are progressing, and the readout chain will be further exercised in upcoming test beam campaigns. Mass production of cassettes and modules is planned for 2025, representing a crucial step towards full deployment.

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