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Effects of Temperature on the Fracture Response of EMC-Si Interface Found in Multilayer Semiconductor Components

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Abstract: Despite the fact that temperature is an important condition that affects the behavior of material interfaces used in integrated circuits (ICs), such as the case for epoxy molding compound (EMC) and silicon (Si), this has not been thoroughly studied. To fill this gap, the present work aims to examine the fracture of the bi-material interfaces in multilayered semiconductor components and, more specifically, the EMC-Si, through the experimental quasi-static mode I fracture experiments conducted at different temperatures. The experiments were followed by numerical simulations using cohesive zone modeling (CZM) implemented using Abaqus. Simulation results were aimed at matching experimental data using an inverse CZM approach to determine cohesive properties such as initial stiffness and maximum traction. Experimental results revealed temperature-dependent variations in fracture behavior, with low temperature (−20 °C) showing a decrease in stiffness with values around 650 MPa/mm and a maximum tensile strength of 48 MPa; high temperature (100 °C) revealed a maximum traction and stiffness of 120 MPa and 1200 MPa/mm, respectively. A possible explanation for the results obtained at high temperatures is that temperature changes cause a significant redistribution of residual stresses in the sample and at the interfaces, reducing the stiffness at lower temperatures.

Keywords: semiconductor; cohesive zone modeling; bi-material interface; quasi-static test; silicon

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1. Introduction

Over the past decades, microelectronic devices and semiconductors have become an immeasurably important part of our daily lives. The industry responsible for manufacturing these devices is driven by three fundamental objectives: enhancing reliability, reducing costs, and minimizing the size of microprocessors.

Research in semiconductors began to intensify in the 20th century with the emergence of modern electronics. The discovery and development of semiconductors as essential materials for the manufacturing of electronic devices, such as transistors and ICs, spurred a series of studies to understand the physical and chemical properties of these materials [1]. Advances in nanotechnology and microelectronics have sparked a growing interest in the study of interfaces between different layers in semiconductor components. Commercial solutions incorporating these technologies are becoming increasingly prevalent across industries such as electronics, photonics, and energy. Companies like Henkel and Dow offer thermal interface materials (TIMs) that use bi-material interfaces to improve heat

dissipation in electronic devices. Solar cell manufacturers explore bi-material interfaces to improve light absorption and charge transport in photovoltaic devices. The precise control of the material interfaces significantly enhances device performance and functionality, paving the way for next-generation electronic technologies.

Among different types of bi-material interfaces found in semiconductor devices, the analysis of the EMC-Si interface has been relatively limited. Schlottig et al. [2] investigated the interfacial fracture toughness of the epoxy molding compound (EMC) to silicon interface using the Mixed Mode Chisel setup (MMC). They identified thermal residual stresses, induced during the cooling process, as the most critical parameter impacting the energy release rate and mode mix angle when interpreting fracture data of the EMC/Si interface. Oh et al. [3] developed an adhesion shear test jig to measure the adhesion strength of the EMC/Si chip interface at high temperatures (200 °C). This temperature was selected due to the potential occurrence of interfacial failure in semiconductor packages during the reflow process, which exceeds 200 °C. Conversion et al. [4] employed ANSYS simulation software to undertake a thermomechanical analysis of adhesion forces at the interface between EMC (epoxy molding compound) and Si (silicon) chips, as well as the relationship between maximum shear stress and principal stress. The findings indicate that a mismatch in the coefficient of thermal expansion (CTE) between the EMC and Si chip results in a progressive increase in both shear stress and principal stress. This escalating stress ultimately surpasses the adhesion force of the EMC/Si chip interface, leading to inevitable interfacial delamination.

Xiao [5] investigated the delamination of the EMC and copper interface using a bi-material two-layer beam structure. In this study, EMC and copper were bonded to create a mixed-mode bending test, allowing for an assessment of the delamination toughness of the EMC-Cu interface. The study revealed that residual stresses had a considerable impact on the crack tip singularity and the interface toughness between EMC and copper. Additionally, Sadeghinia [6] examined the effects of moisture, temperature, and mode mixity on the interfacial fracture toughness of the EMC–copper interface. The study concluded that residual stresses play a significant role in promoting delamination at the EMC–copper interface in microelectronic components. Poshtan et al. [7], by performing a Miniaturized Sub-Critical Bending (MSCB) test, demonstrated that interfacial crack propagation is the dominant failure mode, with MC remaining contaminants observed on the Load Frame (LF) surface. They stated that the amount of these embedded particles is influenced by temperature, surface roughness, and mode mixity. Due to the significantly different testing conditions and sample types, a direct comparison of all the results is not feasible. However, a recent review paper has attempted to address this by normalizing the parameters, enabling a comparative analysis of the results obtained in various studies [8]. Fan et al. [9] utilized Atomic Force Microscopy (AFM) to investigate the cohesion between EMC and copper (EMC-Cu), while Khan [10] focused on the adhesion between transferred graphene and silicon. As the results show, adhesion varies significantly with changes in the graphene used. The values found for the interface of silicon and graphene are very similar to the Mode I fracture energy (G_{Ic}) found for the interface of EMC and copper, as Samet and Woodruff [11] showed. Wang et al. [12] assessed interfacial fracture toughness in flip-chip packages and bi-material systems. The results show a value of 0.02 N/mm for the fracture toughness under Mode II loading conditions. Krieger et al. [13] analyzed the mixed-mode fracture of EMC–copper using the CZM approach, and Raghavan et al. [14] developed a framework based on the cohesive zone modeling approach to investigate interfacial delamination in sub-micron-thick layers. However, none of these studies have examined the behavior of the EMC-Si interface across varying temperatures. Consequently, this paper

seeks to address this specific research gap by investigating the temperature-dependent characteristics of the EMC-Si interface.

The properties of some materials, such as EMC, that are commonly employed to protect and shield other fragile components from exterior conditions like heat, moisture, shocks, etc., and silicon, one of the main materials used in microprocessors, have been thoroughly investigated due to their vast array of applications, yet there has not been much focus on studying the interfaces of these two materials when utilized in a semiconductor. The lack of sufficient knowledge about how these interfacial properties change with environmental factors, mainly temperature, poses significant challenges. This can lead to problems because any damage at the interface may simply result in the initiation and subsequent propagation of cracks through the component. Therefore, studying and analyzing the variation in interface properties of these two materials with different temperatures is an important barrier that needs to be taken in order to achieve further development of new products and ideas. Because, as products get more sophisticated, the interaction between some of the most common materials used in this sector turns into a pivotal aspect in making new ideas come to life.

This paper aims to analyze crack propagation at the EMC-Si bi-material interface under diverse temperatures and study interfacial damage evolution by determining the interfacial cohesive contact characteristics of the examined bi-material interface. These characteristics are essential for designers and engineers to forecast interface strength and durability, especially under Mode I (tensile or opening mode) loading conditions. Therefore, the cohesive zone model was essential to simulate the interfacial failure of the joint.

2. Materials and Methods

2.1. Design and Geometry

This study focused on the EMC-Si interface. EMC and silicon are typically joined through a process that involves the application of heat and pressure during the molding process [15,16]. The EMC, which consists of thermosetting epoxy polymers, is deposited on the silicon wafer, allowing it to cure and create a strong adhesive bond between the two materials. This bond is crucial for the reliability of electronic packages, helping to prevent void formation and interface delamination. Figure 1 is a technical illustration of the wafer's layers; the specimen also comprises an inbuilt gold layer that serves as a pre-crack to facilitate crack propagation along the bi-material interface during the DCB (double cantilever beam) quasi-static tests.

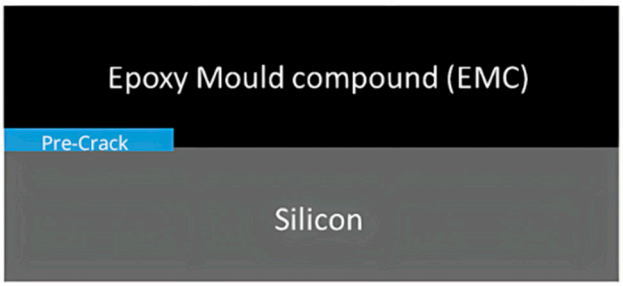

Figure 1. Schematic representation of the tested specimens.

In consideration of the DCB testing setup in universal testing machines, the width and length dimensions have been thoughtfully pre-selected to ensure compatibility, and the holes incorporated into the steel bars serve the purpose of applying load to the wafers via loading pins. The technical dimensions of the DCB and the loading pin reference point can be seen in Figure 2.

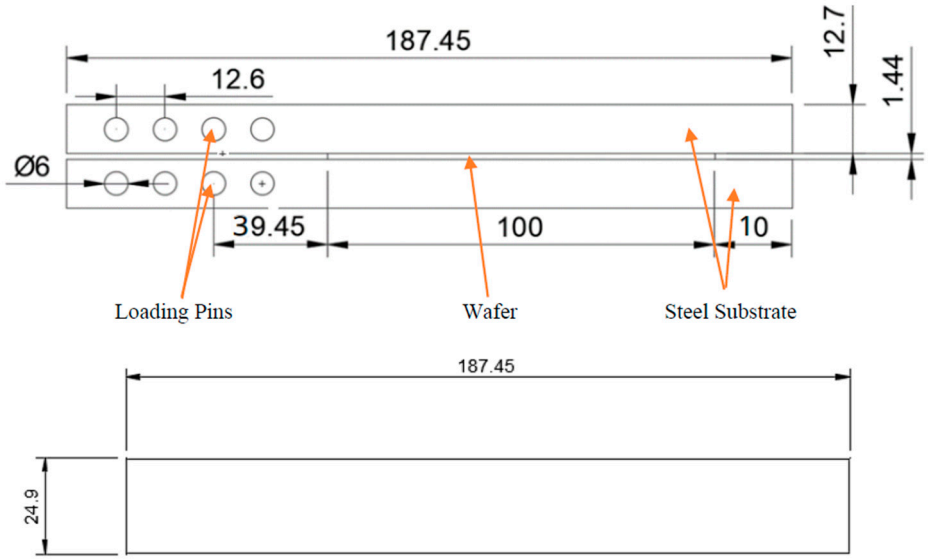

Figure 2. Illustration of the dimensions of the DCB (all dimensions are in mm).

2.2. Materials

The relevant mechanical properties of EMC and silicon are given in Table 1. It should be noted that silicon exhibits anisotropic behavior [17]; the possible values of Young's modulus (E) for silicon range from 130 to 188 GPa [18]. For silicon in the <100> crystallographic direction, the Young's modulus is typically around 130 GPa [19]. This value is commonly used in simulations and approximations, especially in contexts where a simplified model is appropriate to describe the mechanical behavior of the material. Among the materials comprising the wafers, silicon is the most common material to be found in semiconductors, with its ultra-high purity single crystal structure and very brittle characteristics, which play a critical role in the operation of computers, smartphones, and various other electronic gadgets. Another advantage of using a semiconductor, such as silicon, is that at low temperatures the electrons are held in place by covalent bonds, acting as insulators. However, at higher temperatures, these electrons gain enough energy to break free from their bonds and move about the crystal lattice, allowing conduction to occur.

On the opposite side, EMC is essentially a ductile glass-fiber-reinforced epoxy made of silica, hardener, epoxy resin, and, optionally, other fillers and additives that play a vital role in protecting circuits on semiconductor devices from moisture, heat, and shock. It can, not only enhance the reliability of the component by minimizing the impact of electromagnetic interference (EMI) from external sources but also play a vital role in packaging semiconductor devices, where their interaction with silicon significantly influences the structural integrity of these components [20,21].

Table 1. List of material properties [22,23].

Materials	Ultimate Tensile Strength (MPa)	Poisson's Ratio	Young's Modulus (GPa)
Silicon	165	0.28	130
EMC	90	0.38	24
Steel PM300	1020	0.33	210

Changes in temperature and humidity can influence the interfacial strength [24]. Moreover, adding a very thin layer of a different material may contribute to a better interface contact and, thus, a higher G_{Ic}. The reason behind choosing gold as a pre-crack material is because it is an inert material and has a low bonding strength with silicon and

EMC; this way, the chemical reactions that may occur between silicon or EMC and gold can be neglected.

It is important to note that when the wafers are produced, EMC and silicon are merged at high temperatures. During the curing and cooling processes, the materials may warp, resulting in residual stresses that must be considered. Introducing an initial defect such as a pre-crack minimizes the chance of peak loads prior to delamination.

Two different adhesives were used. One for testing at room and low temperature, Scotch Weld 163-2K (3M, Saint Paul, MN, USA), and another one for high temperature, Delo Monopox AD286 (DELO, Windach, Germany). This was necessary due to the loss of mechanical properties with high temperatures of the first adhesive. The parameters for both adhesives were given by the producer and can be seen in Table 2.

Table 2. Adhesive properties.

Adhesive	Tensile Strength [MPa]	Poisson's Ratio	Young's Modulus [GPa]
Delo Monopox AD286	64	-	3.8
Scotch Weld 163-2	48.3	0.34	1.1

According to the literature, silicon properties' variation with temperature can be ignored [25]. As for the EMC, the variation in its properties with temperature relies heavily on its composition. EMC is a composite made with epoxy and fillers, and if, for instance, its ratio changes from producer to producer, it is hard to tell how the variation in its properties with temperature may occur [21,26]. Although there is strong evidence that with higher temperatures, EMC's Young's modulus decreases, this variation did not significantly affect the numeric simulations.

2.3. Manufacturing Process

The manufacturing process starts with surface preparation of the steel bars and wafer surfaces. The first step is sandblasting the steel bars. This technique enhances surface roughness while deeply eliminating and cleaning contaminants and leftovers, guaranteeing this way superior adhesion. Then, spare sand and dust are then removed from the steel bars with the aid of compressed air and afterward cleaned with acetone.

The preparation of the wafer starts by applying 800-grit sandpaper at 45° angles. The surfaces are then cleaned with acetone and followed by a plasma treatment of 6 s on each face. This process enhances the surface energy of the EMC by approximately 200%, facilitating the application of the adhesive in them and, also, a better adhesion to the steel substrates [20]. After this, two layers of tape are applied to the sides of the wafer to prevent any excess adhesive from flowing out and to bind the interface at the sides.

Following the preparation of the bar and the wafer, it is necessary to use a mold to regulate the alignment of the DCBs and the applied pressure during the curing process (Figure 3). The adhesive is then manually applied. The curing process is carried out at a temperature of 120 °C for 90 min with the use of three 1 kg masses that are placed on the top aluminum plate along the length of the wafer.

The mold consists of two aluminum plates with small holes designed for inserting pins to secure the DCBs in position. Nevertheless, given the short length of the steel bars employed in the DCB assembly, it is imperative to incorporate spacers behind them to ensure a snug fit onto the mold. Not only that, but tapes also (with the wafer height) were positioned on the extremities of the wafer to ensure a more compact fit of the weights during the curing process.

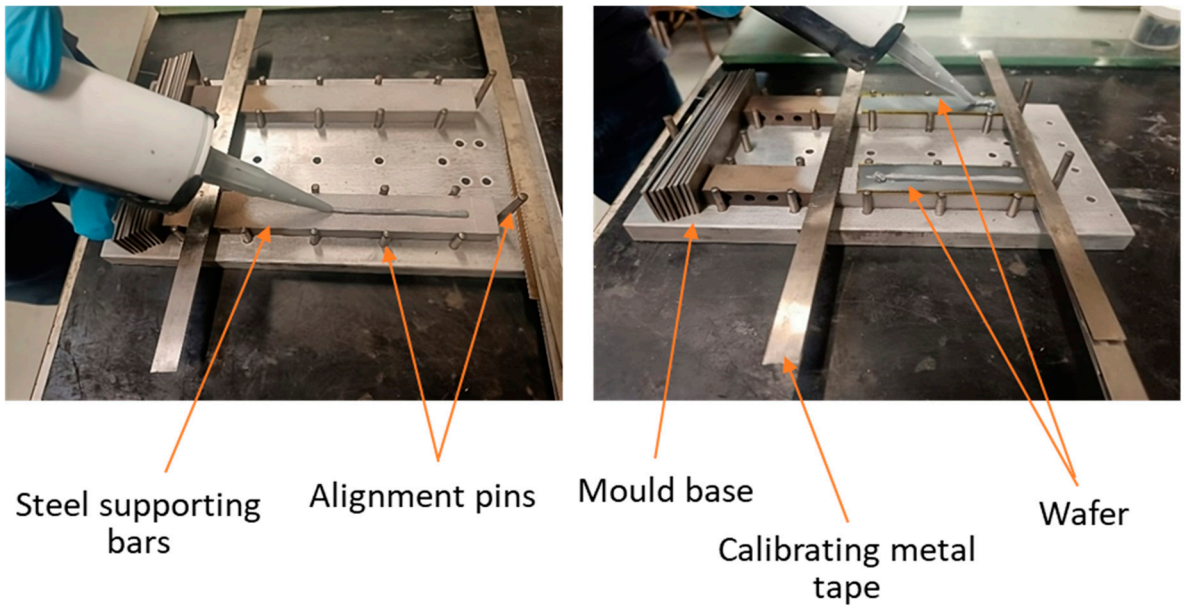

Figure 3. DBC joint in the mold and application of adhesive.

2.4. Test Procedure

After completing all the steps mentioned and removing the tape and eventual excess adhesive covering the edges of the wafer, the DCB joints will be tested under three different conditions: room temperature (around 23 °C), low temperature (−20 °C), and high temperature (100 °C). It should be noted that all tests are conducted at a relative humidity of 50% to 60%. This variation in the relative humidity has a negligible impact on the results.

During the room temperature and low-temperature testing procedures, the INSTRON 8801 (INSTRON, Norwood, MA, USA) machine was used, and the displacement rate for the tests was set at 0.2 mm/min. The load was applied using a Mode I loading technique throughout the test. For both low- and high-temperature testing, a thermocouple (see Figure 4) was used to measure the temperature accurately during the test. By placing the thermocouple on the specimen or within the testing apparatus, it is possible to monitor temperature changes accurately and adjust as needed to maintain the desired testing conditions.

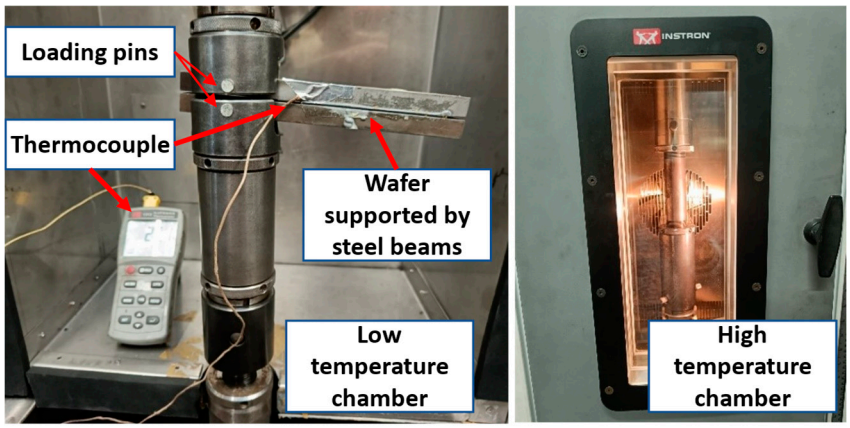

Figure 4. Testing procedure under low and high temperatures.

The machine's retrieved data were treated using the Compliance-Based Beam Method (CBBM). This method assists in discerning the energy release rate of a crack without requiring direct measurement of its size during testing.

Instead, the compliance (C) of the specimen is used to calculate an equivalent crack length (a_{eq}) using Equation (1). This equivalent crack length is then utilized in Equation (2) to determine the critical fracture energy. Equation (2) includes various parameters such as the modulus of the specimen (G), the flexural modulus (E_f), which is obtained from Equation (3), the load (P), the thickness of the substrate (h), and the width of the specimen (B) [20,22].

This method relies exclusively on the joint's compliance, which is ascertained by measuring the load (P) and displacement (δ) values during the experiment. By utilizing this compliance, it becomes possible to estimate both the equivalent crack length (a_{eq}) and the critical fracture energy (G_{Ic}) with a high degree of accuracy. CBBM's superiority to classical methods stems from its consideration of the fracture process zone (FPZ) (located ahead of the crack tip), which can greatly impact the fracture behavior of adhesive joints. The FPZ is a critical area at the crack tip where complex interactions, such as micro-cracking and plastic deformation, significantly affect the material's response to loading. The energy dissipated within this zone must be accounted for when evaluating fracture toughness, particularly for ductile adhesives that exhibit considerable deformation during crack propagation. The FPZ influences the overall fracture toughness by absorbing energy. This absorption is paramount in preventing catastrophic failure and can lead to an increase in the effective fracture energy measured by tests using the CBBM. The method's flexibility allows for adjustments to the calculated elastic modulus to account for the differing energy dissipation patterns in varying adhesives and joint configurations, thereby enhancing accuracy [27].

$$C = \frac{\delta}{P} = \frac{8{a_{eq}}^3}{bh^3E_f} + \frac{12a_{eq}}{5Gbh}. \tag{1}$$

$$G_{Ic} = \frac{6P}{B^2h}\left(\frac{2{a_{eq}}^2}{h^2E_f} + \frac{1}{5G}\right). \tag{2}$$

$$E_f = \left(C_0 - \frac{12(a_0 + |\Delta|)}{5Gbh} + \frac{1}{5G}\right)^{-1}\frac{8(a_0 + |\Delta|)^3}{bh^3}. \tag{3}$$

The flexural modulus represents the stress concentration around the crack tip and is affected by the substrate dimensions (h and b), the initial crack length (a_0), the adherent shear modulus (G), and the initial compliance (C_0). C in Equation (1) is calculated by the ratio of displacement (δ) to the applied load (P). A correction factor for the crack length (Δ) is applied and determined by Equation (4)

$$\Delta = h\sqrt{\frac{E\left(3 - 2\frac{\tau}{1+\tau}\right)^2}{11G}}. \tag{4}$$

$$\tau = \frac{1.18E}{G}. \tag{5}$$

To accurately interpret the experimental values, it is important to have a numerical model that defines how the crack propagates. The interaction between silicon and EMC is influenced by the stiffness coefficients, maximum traction, and fracture energy of the interfaces. Since the value of G_{Ic} is already known, an inverse approach was used to determine the stiffness and maximum traction. This involved testing different values for the two parameters and analyzing the resulting load–displacement curve. The final values for maximum traction and initial stiffness were determined when the experimental and numerical load–displacement curves matched.

All these parameters are important for a CZM analysis, which has been widely used for modeling crack propagation through interfaces. This technique works on the basis that there is a unified surface where damage can occur and spread.

2.5. Numerical Simulation

From the experimental values retrieved from the quasi-static tests, an iterative process using an inverse CZM approach was employed. The simulation tried to match the load–displacement curves obtained experimentally by manipulating the values for initial stiffness and maximum traction.

2.5.1. Cohesive Behavior

Cohesive elements are designed to simulate crack growth and cohesive behavior within a homogeneous material. However, they may not capture the intricacies of interface failure in the EMC-Si bi-material system. Accordingly, cohesive surface or cohesive contact is the best choice for our specific application, since it provided a more robust solution for the observed failure mechanisms. This approach assumes the existence of a cohesive surface through which the damage will initiate and propagate through.

CZM is a model that uses the cohesive law to predict the behavior of materials under fracture while regarding fracture formation as a gradual phenomenon (see Figure 5a), where the crack propagation is resisted by cohesive tractions. The interface exhibits varying degrees of damage along its length, with the crack tip showing the most severe damage, as indicated by higher values in Figure 5a. The damage decreases for points farther from the crack tip, eventually reaching zero. The damage index ranges from 0 (no damage) far from the crack tip to 1 (complete failure) at the crack tip. Figure 5a also demonstrates that traction on the crack surfaces is lowest near the crack tip and increases with distance from the crack tip. The traction-separation curve in cohesive contact represents the cohesive forces and energy dissipation at the bi-material interface between two adjacent surfaces that are modeled as a distinct region with its own material properties and behavior.

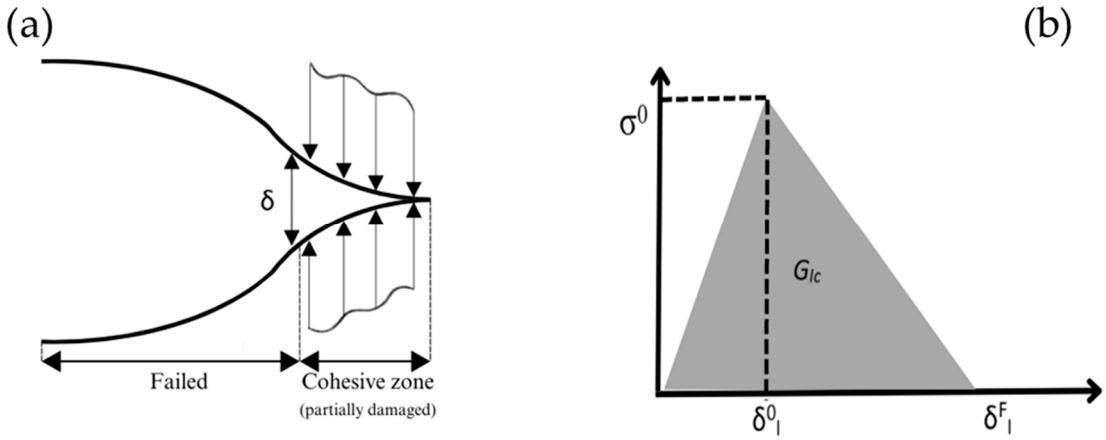

Figure 5. (**a**) CZM visual approach and (**b**) CZM traction separation curve.

Three parameters are required to conduct a triangular CZM analysis (Figure 5b): fracture energy, initial stiffness, and maximum traction. The G_{Ic} was obtained experimentally; as for the other two, an inverse cohesive contact method was utilized, where values for maximum nominal stress and initial stiffness were applied until the numerical and experimental load–displacement curves matched.

The slope of the initial segment ($\delta < \delta^0{}_I$) indicates the typical cohesive stiffness, while σ_0 represents the maximum traction in this model. When $\delta^0{}_I$ is reached, damage begins at

0 and progresses until it reaches 1 at $\delta^F{}_I$. At this point, tension decreases to zero, indicating the absence of interactions between the contacting surfaces.

The damage gradually spreads along the bi-material interface, affecting each point to varying degrees. Notably, the damage at the crack tip is more severe, with higher values observed. However, as one moves away from this location, the level of damage decreases and may even reach zero. The damage index ranges from 0 (indicating no damage) for points far from the crack tip to 1 (indicating complete element failure) for the crack tip itself.

2.5.2. Numerical Model

The dimensions used for both the wafer and the steel bars are the ones mentioned in the previous section, with the exception for the adhesive thickness, which was added to the simulation with a value of 0.15 mm (on both sides). The modeled bonded joint, as well as the different zones of the part, can be seen in Figure 6.

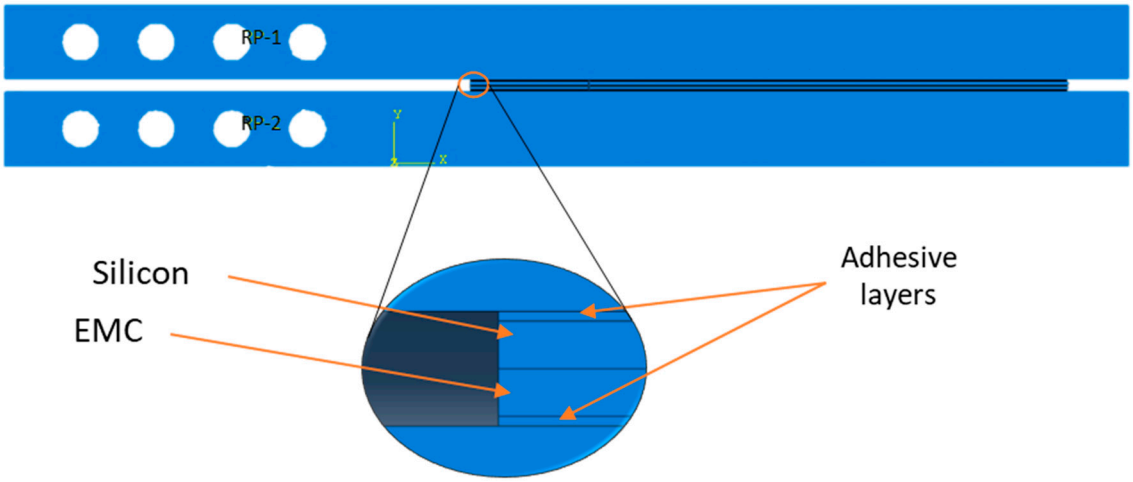

Figure 6. DCB assembly and different parts (wafer).

The selected simulation method was quasi-static analysis, and considering the geometric configuration, it is imperative to establish interactions among the manufactured components to ensure a precise simulation of DCB's behavior on Abaqus software (2021). Empirical tests have revealed crack propagation occurring between the silicon and EMC interface. Hence, a cohesive zone model was used to define the damage path along these interfaces.

Three constraints, more specifically two couplings (RP-1 and RP-2) and the fixed tip, had to be defined. The two couplings in the center of the holes of the DCB, the second ones from right to left, simulate the place where the vertical load was applied during the experimental tests. Moreover, all the interfaces, except the EMC-Si surface, were tied together, as can be seen in Figure 7.

To simulate the displacement applied through the loading pins, the y-axis displacement was set to 1.5 mm, while the other two axes were not constrained. The simple support only had the y-axis displacement constrained. These conditions restrict the model's y-directional movement and bottom bar rotations. A visual representation of each boundary condition in the DCB can be seen in Figure 7.

To better simulate the pre-crack, a frictionless contact was added for the first 2 cm (pre-crack length) of the wafer geometry, as shown in Figure 7. The CZM contact properties were then defined for the EMC-Si interface, more specifically the G_{Ic} and the viscosity coefficient, and the other two parameters, the elasticity module and the shear tension, were estimated to begin the inverse cohesive approach.

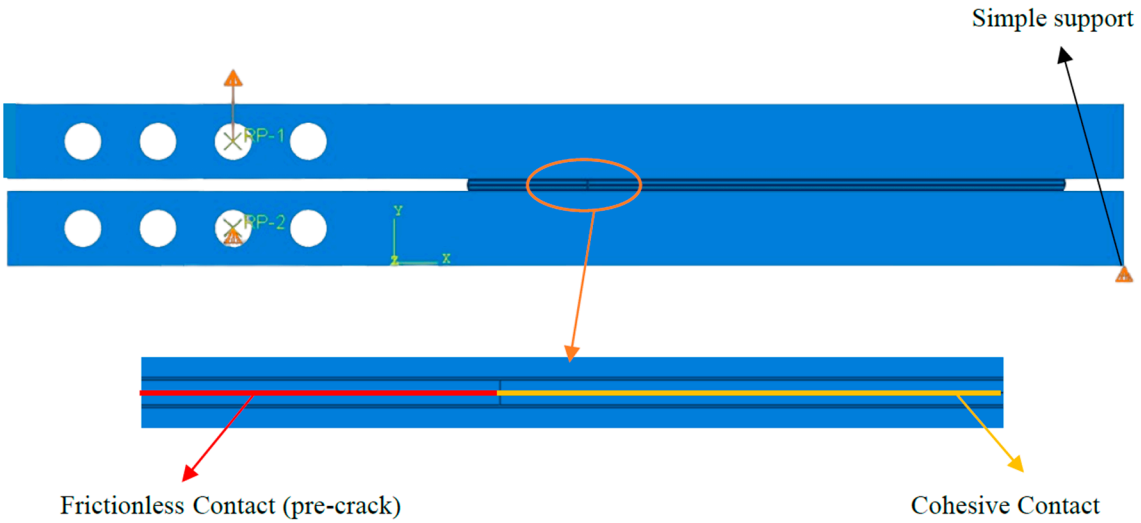

Figure 7. Loading and boundary conditions (the load was applied to RP-1 while RP-2 was simply supported.

In order to obtain a simple but refined mesh, a global mesh with a medium density of 0.1 mm was applied in the entire wafer, and a local mesh with a maximum element size of 3 mm and a minimum element size of 0.1 mm was used along the steel bars. The DCB's mesh geometry can be observed in Figure 8. All the mesh element types are 4-node bilinear plane stress.

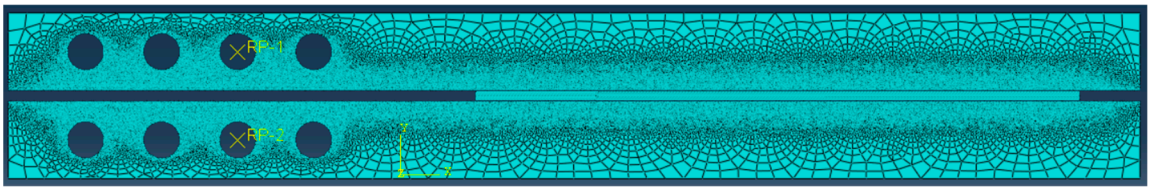

Figure 8. Mesh configuration.

As mentioned before, it is needed to develop a cohesive law that can accurately predict damage propagation; an iterative approach was utilized. This involved determining the values of the cohesive zone properties that would yield a similar curve to the experimental one. The final values were determined once the curves matched each other. The same procedure was used for the other temperatures.

3. Results and Discussion

3.1. Failure Mode

Considering the experimental results, it was discovered that the crack did not always propagate exclusively at the bi-material interface but instead partially or entirely through another layer of the tested wafer. Consequently, the results may vary according to their corresponding failure mechanisms, which include interfacial failure (when the crack propagated through the bi-material interface), silicon failure (when the crack extended into the silicon layer of the wafer), and mixed failure (when the crack simultaneously propagated through the bi-material interface and the silicon layer); see Figure 9. It is worth noting that the weakest part of the joint is the one to which the crack will extend.

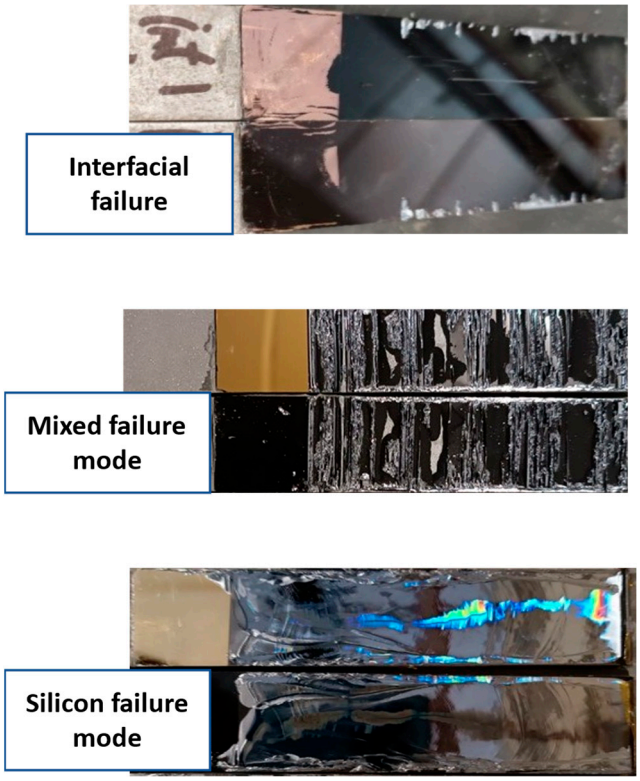

Figure 9. Different types of failure modes in wafers.

According to Oh et al. [3], interfacial failure is due to low EMC/Si interfacial adhesion strength. They concluded that plasma treatment could significantly enhance the adhesion strength of the EMC/Si chip interface by removing the contamination and forming the functional groups like carboxylic acids on the surface of the Si chip. These carboxylic acid functional groups can improve the interfacial adhesion by reacting chemically with the epoxy and thus providing a mechanism of interfacial bridging through the formation of covalent bonds, leading to better adhesion strength.

Xiao et al. [28] confirmed that the failure path of delaminated EMC/Cu samples depends on the loading mode mixture, environmental conditions, and surface roughness. Their analysis of various delaminated specimens revealed three scenarios. First, chunks of molding compound remained on the leadframe surface, with heights up to several tens of micrometers. These chunks contained less filler than the bulk molding compound, and their distribution depended on the load mixture and temperature conditions, leading to holes in the EMC counterparts. In the second scenario, cracking occurred at texture features on the leadframe surface, where deep trenches were filled with sheared-off molding compound. The third scenario involved clean detachment of the EMC from the leadframe surface.

According to Tian et al. [16], the entry of H_2O and O_2 through polymer-based epoxy plastic sealers or polyimide (PI) layers can lead to corrosion and oxidation reactions. These reactions, combined with pre-existing thermal stresses, result in hybrid delamination failures at the interface. They suggest that addressing delamination failures can be achieved through two primary methods: enhancing production process technology or altering the structure or material of the device package.

Schlottig et al. [2] observed that kinking cracks in the silicon material were primarily caused by flaws in the silicon strip flanks. They emphasized the importance of careful handling of this part of the sample during the preparation steps to avoid pre-damage. The flaws were predominantly found at the flanks of prototype samples, resulting in cracks in every experiment.

3.2. Experimental Results

All three testing temperatures revealed an interfacial failure mode during the initial moments of testing. However, under low temperature, crack propagation across the wafer displayed a mixed mode failure after 8 mm of interfacial failure. This last phase, characterized by the unpredictability of the crack show, has not been subject to study. The quasi-static Mode I experimental results for the three temperatures are shown in Figure 10.

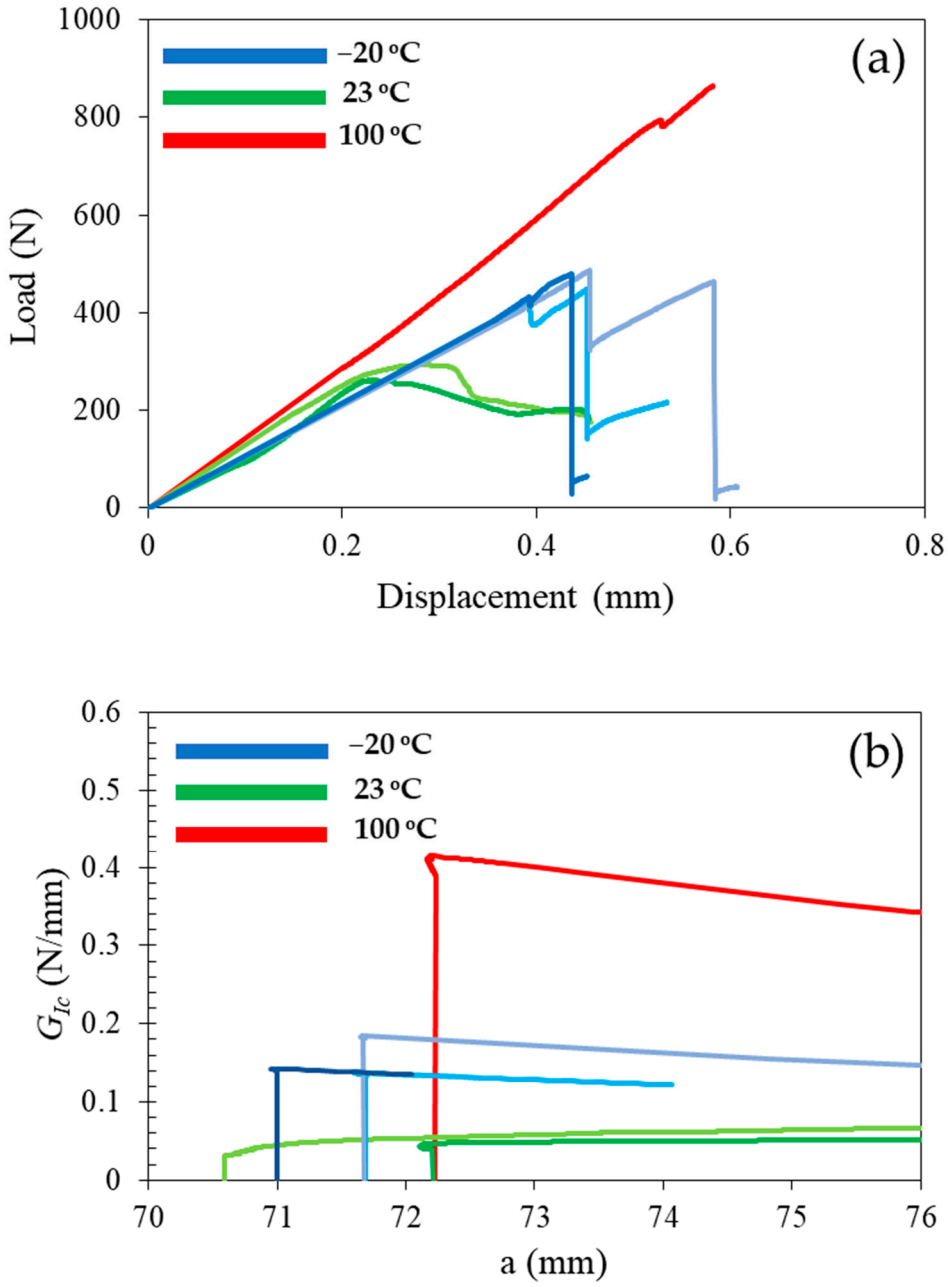

Figure 10. Comparison of (**a**) the experimental load–displacement curves and (**b**) the experimental R-curves at the respective temperatures.

The experimental results shown in Figure 10a,b are load–displacement and R-curves for six specimens at three different temperatures. As for Table 3, the results presented for the room temperature are a mean of two tests carried out during the experimental procedures; the low temperature values shown were obtained from a mean of three experimental tests conducted, and for high temperature, only one result was obtained.

Table 3. Comparison of the interfacial properties at different temperatures.

	G_{Ic} (N/mm)	Failure Mode
Room Temperature (23 °C)	0.05 ± 0.001	Interfacial
Low Temperature (−20 °C)	0.13 ± 0.005	Interfacial
High Temperature (100 °C)	0.37	Interfacial

It is important to notice that the value of the parameters for the room temperature curve is lower than that of the other curves. Theoretically, there must be a correlation between the variation in values from low to high temperatures. This anomaly can be explained by the residual stresses that are significantly changed by changing the testing temperature. This factor affects the behavior of the wafer and the tested joint. Defining loading conditions is often not straightforward because stresses can be introduced throughout the processing history. Typically, the constituents are stress-free at the processing temperature, but chemical stressors like migration, oxidation, or polymerization can still occur at this stage [29]. These residual stresses are usually compounded by stresses induced by thermal mismatches during cooling from the processing temperature or environmental temperature fluctuations, as well as time-dependent properties such as Young's modulus (because of the viscoelastic behavior of EMC) [29]. At low temperatures, materials typically exhibit increased stiffness and reduced ductility. The differences in thermal contraction rates between the polymer matrix (EMC) and the silicon layer lead to higher locked-in residual stresses [5,30,31]. In addition to this, the residual stress induced in the previous steps of wafer production and DCB manufacturing is also re-distributed by changing the testing temperature. At 23 °C, there is some degree of molecular mobility within the polymer matrix, allowing for partial relaxation of the previously induced residual stresses. However, this relaxation may still be insufficient to significantly improve energy absorption during fracture due to the material's inherent properties at this temperature. Room temperature behavior can be influenced by competing effects; while some residual stresses may be relieved, the low toughness of the polymer at this operational range may not facilitate effective energy dissipation, resulting in the lowest measured G_{Ic} observed in the experiments. The stress distribution might still manifest as tension at the crack tip, which could make the material more susceptible to crack propagation at this temperature, further lowering the fracture energy. At elevated temperatures, the polymer matrix experiences significant thermal activation. The molecular mobility increases, allowing for the redistribution and relaxation of residual stresses. This thermally driven process helps mitigate the tensile stresses that may have been present at lower temperatures. As a result of stress relaxation, the material can undergo larger deformations before fracturing, leading to an increase in the energy absorption capability. The fracture energy observed at this temperature stands at G_{Ic} = 0.37 N/mm, reflecting a significant enhancement in toughness.

3.3. Numerical vs. Experimental Results

- Room Temperature

The numerical simulation for the room temperature curve gave us a good approximation, with a maximum experimental load of 260 N and a fracture energy of 0.051 N/mm, as can be seen in Figure 11. The CZM parameters obtained were 720 MPa/mm for the initial stiffness and a maximum tensile strength of 31 MPa.

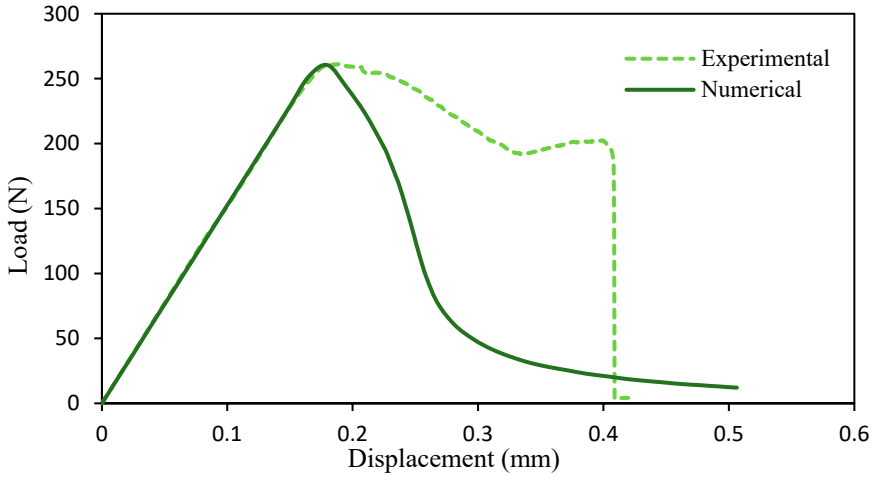

Figure 11. Comparison of numerical and experimental load–displacement curves at room temperature.

As observed in Figure 12, the decline in value for the numerical G_{Ic} happens after its peak. The explanation for this phenomenon resides in the numerical load–displacement curve format. In contrast with the experimental load–displacement curve, the numerical curve presents the steepest decline in maximum load after its peak. This can possibly be explained because mixed failure in crack propagation occurs after an initial interfacial failure. The CZM model describes only crack propagation between a bi-material interface (EMC-Si).

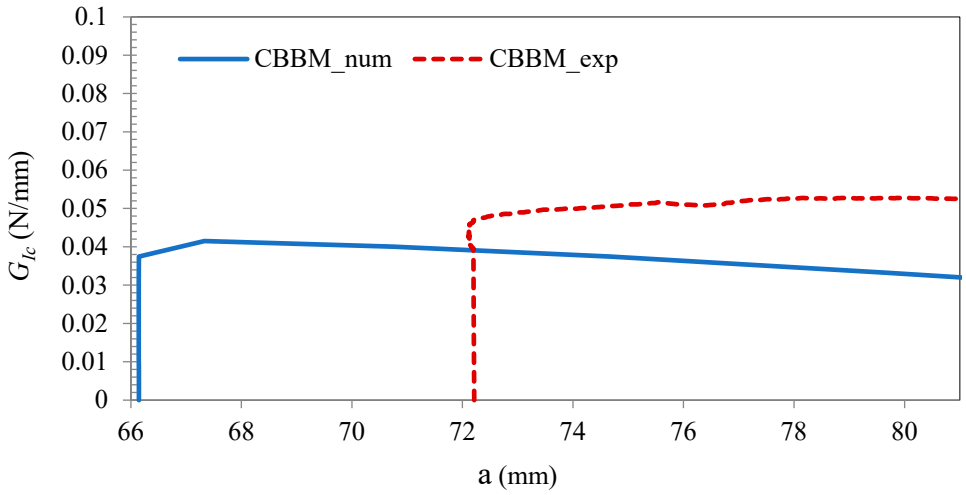

Figure 12. Comparison of numerical and experimental R-curves for the EMC-Si interface (Room temperature).

- Low Temperature

For the tested configurations at low temperature (−20 °C), after damage initiation, the initial crack propagation, after peak loads, shows a relatively abrupt reduction in load. The first peak of maximum load sits around 420 N (Figure 13), and the CZM parameters obtained were 650 MPa/mm for the initial stiffness and a maximum tensile strength of around 48 MPa. The R-curves are shown in Figure 14.

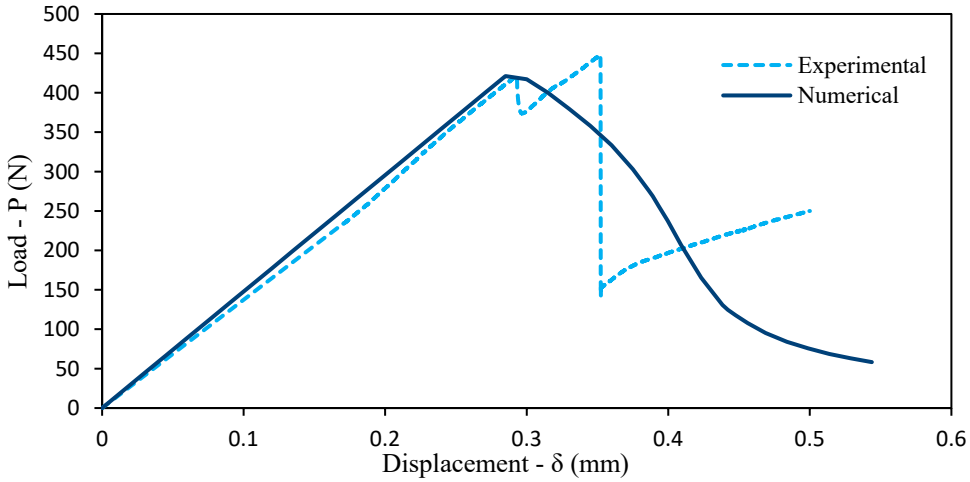

Figure 13. Comparison of numerical and experimental load–displacement curves at low temperature.

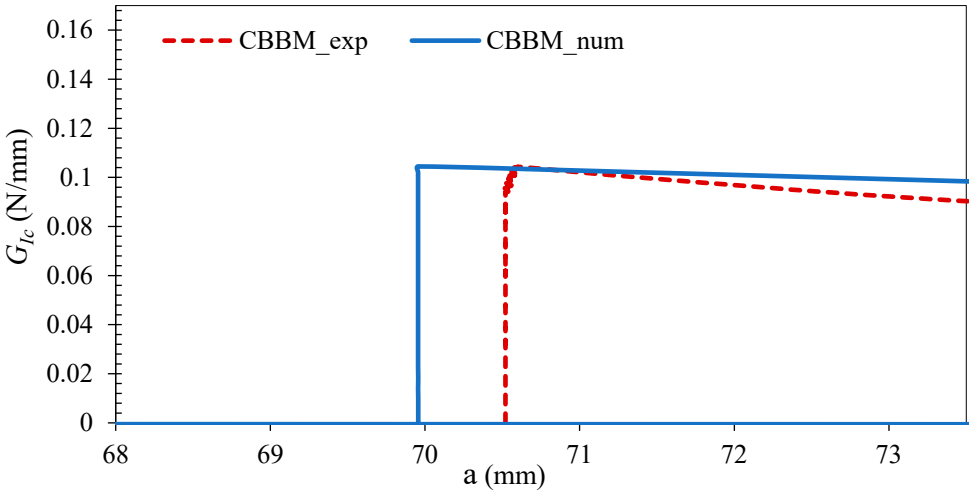

Figure 14. Comparison of numerical and experimental R-curves for the EMC-Si interface (low temperature).

- High Temperature

At high temperature (100 °C), a maximum load of around 850 N with a fracture energy of 0.37 N/mm can be observed (Figure 15). For the CZM parameters, an initial stiffness of 1200 MPa/mm and a maximum tensile strength of 120 MPa.

Given that wafers are assembled at high temperatures and are composed of a different range of materials, each with different coefficients of thermal expansion, there are stresses distributed through these specimens, which can alter the properties of the interface. This can impact the results obtained; for example, it is possible that at lower temperatures these stresses contribute to an easier delamination, allowing one to achieve lower mechanical properties at low temperatures than at higher temperatures.

It should also be considered that since wafer manufacturing is carried out at high temperatures, the redistribution of thermal stresses can play a great influence on the variability of results of low vs. high temperature testing. It is important to highlight that T_g of the epoxy can vary significantly within a range based on different curing conditions and formulations, typically measured between 120 °C and 190 °C for various epoxy systems [2,8,28]. The high-temperature conditions tested are close but still below the T_g of the EMC. This also may affect the results at high temperature. In EMC interfaces, interfacial strength only exhibits a significant decrease after reaching a testing temperature of around 150 °C [8]. This can be attributed to the glass transition temperature (T_g) of the EMC, which causes the

EMC to shift from a hard and glassy state to a soft and rubbery state, accompanied by a significant decrease in Young's modulus (up to 90% decrease), leading to a considerable loss of interfacial adhesion strength.

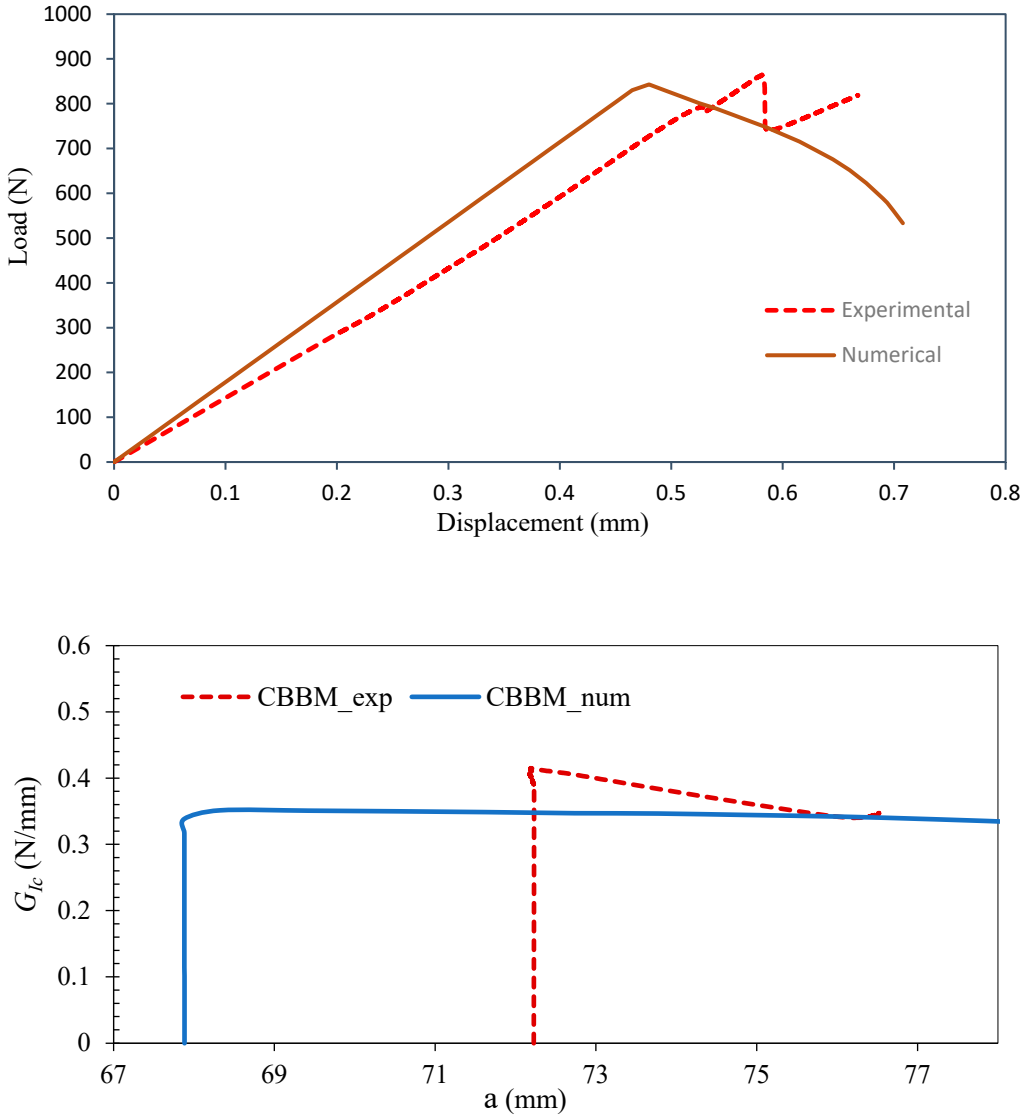

Figure 15. Comparison of numerical and experimental load–displacement and R-curves at high temperature (100 °C).

The numerical results were, as mentioned before, obtained from the iterative process that employed the inverse CZM approach, and the values presented in Table 4 are representative of the last iteration.

Table 4. Numerical simulation parameters.

	Initial Stiffness (MPa/mm)	**G_{Ic} (N/mm)**	**Max. Tensile Strength (MPa)**
Room Temperature (23 °C)	720	0.051	31
Low Temperature (−20 °C)	650	0.13	48
High Temperature (100 °C)	1200	0.37	120

4. Conclusions

In this study, crack propagation and interfacial failure at the EMC-Si bi-material interface under varying temperatures were analyzed using experimental and numerical approaches. The study was driven by the imperative need to enhance understanding of material interfaces at different service temperatures crucial to the semiconductor industry's development. Through experimental mode I fracture tests, valuable data on fracture energy and crack propagation behavior under different temperature conditions was obtained. The results showed significant temperature-dependent variations in fracture behavior, highlighting the complex interactions of thermal and mechanical stresses at the bi-material interface.

Additionally, numerical simulations using CZM allowed for a deeper understanding of damage propagation and interface behavior. By employing an inverse contact CZM approach, numerical simulations were matched with experimental data, determining this way the cohesive properties of the interface under study. For room temperature testing, the results showed an initial cohesive stiffness of 720 MPa/mm and a maximum traction of 31 MPa. For low temperature, these parameters are 650 MPa/mm and 48 MPa for the stiffness and traction, respectively. And last, for high-temperature testing, the findings were 1200 MPa/mm for the initial stiffness and 120 MPa for the maximum traction. As the results show, a linear relationship of fracture energy with temperature was not observed, as the fracture energy at room temperature was lower than at low and high temperatures. It should be noted that thermal stresses in the tested wafers may significantly contribute to the failure mechanism and mechanical properties.

Understanding the behavior of bi-material interfaces is crucial for optimizing the design and durability of microelectronic devices, which play pivotal roles in various sectors, including health, communication, security, and education. Still further analysis is required to better understand the interaction effects of thermal and mechanical stresses on the fracture response of such bi-material interfaces.

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