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Review

A Review of Techniques to Enhance an Amplifier's Performance Using Resistive Local Common Mode Feedback

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Abstract: A review of some of the most common applications of the resistive local common mode feedback technique to enhance amplifier's performance is presented. It is shown that this simple technique offers essential improvement in open loop gain, gain-bandwidth product, slew rate, common mode rejection ratio, power supply rejection ratio, etc. This is achieved without increasing power dissipation or supply voltage requirements and with small additional silicon area and circuit complexity. It is also shown that it is especially appropriate to improve amplifiers' performance in current fine-line submicrometer CMOS technology. Some of the applications discussed are GB enhanced, class AB and super class AB operational amplifiers, gain boosted op-amps, bulk-driven circuits, sample and hold circuits and power management circuits, among others.

Keywords: analog circuits; class AB amplifiers; fine line CMOS technology; resistive local common mode feedback

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1. Introduction

The differential amplifier is used as the input stage of most op-amps. Figure 1a–c show differential pairs loaded with conventional resistive loads, diode-connected and high impedance current source active loads, respectively. For $V_{i+} = V_{id}/2$ and $V_{i-} = -V_{id}/2$, $V_{od} = V_a - V_b$ the differential voltage gain $A_d = V_{od}/V_{id}$ is given by $A_d = g_{m1} R_L$ where R_L is the effective load resistance. In Figure 1a $R_L = R||r_{o1}||r_{o2} = R'$. For Figure 1b $R_L = [1/(g_{m2}||r_{o1}||r_{o2})] \approx 1/g_{m2}$ and $A_d \approx [(k_n/k_p)(W/L)_1/(W/L)_2]^{1/2}$. For Figure 1c the load is $R_L = r_{o1}||r_{o2}$ and the gain $A_d \approx g_{m1} r_o/2 \approx A_{int}/2$, where g_m denotes the small signal transconductance gain, r_o the output resistance, k_n and k_p the transconductance parameters of PMOS and NMOS transistors, respectively, and $A_{int} = g_m r_o$ the intrinsic gain of the MOS transistor. A_{int} is in the range from 25 to 50 in current fine-line CMOS technology. Increasing R in Figure 1a allows to increase the gain at the expense of a higher quiescent drop $V_R = I_B R$ caused by the bias current I_{BIAS} in the load resistors R. This drop limits the maximum value of R and also limits the maximum gain that can be achieved from this circuit to values well below the intrinsic gain. In current technologies, this limitation is especially severe due to the sub-volt supply voltages $V_{supply} < 1V$ used. The gain of Figure 1b is usually limited to values below 5 since it is proportional to the square root of the ratio $(W/L)_1/(W/L)_2$ and large gain values require very large transistor ratios. The gain of the circuit of Figure 1b can be boosted using positive feedback (using transistors M2pf and M2Ppf shown in red). In this case, the gain is given by $A_d = g_{m1}/(g_{m2} - g_{m2pf})$. In practice, A_d is kept below 8–10 in order to prevent the circuit to perform as a latch because values of g_{m2pf} very close to g_{m2} manufacturing tolerances can result in $g_{m2pf} > g_{m2}$ which causes positive feedback to dominate and the circuit to perform as a latch. The circuit of Figure 1c has a gain of $A_d = A_{int}/2$. The cascoded version of Figure 1c (not shown in Figure 1) can offer much higher gain (by a factor of A_{int}) but it is difficult to use in

modern technology since, as indicated above, sub-volt supply voltages prevent utilization of cascode transistors, especially in the output amplifier's stage. The circuit of Figure 1c requires a control voltage V_x to generate quiescent currents in I_{M2}, I_{M2P} that accurately match the bias currents $I_a = I_b = I_{BIAS}$ in transistors M1, M1P (otherwise nodes a and b would easily go into saturation causing the amplifier to be non-functional). This is only possible if the circuit is part of an op-amp with global negative feedback or if it is used as a standalone amplifier, in which case, an additional, relatively complex, control circuit is required.

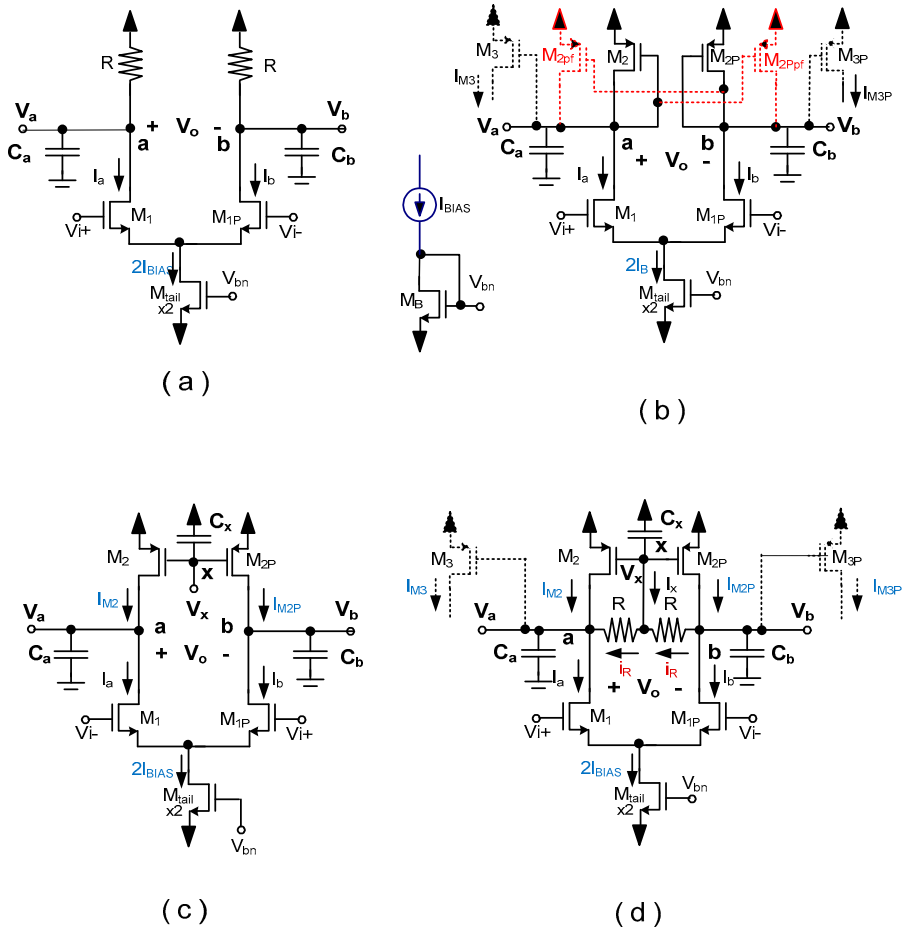


Figure 1. (**a**) Conventional differential pair with resistive load. (**b**) Differential pair with diode-connected load and optional positive feedback load (**c**) Differential pair with current source active loads (**d**) Differential pair with resistive local common mode feedback load. This is a figure. Schemes follow the same formatting.

2. Differential Pair with Resistive Local Common Mode Feedback

In this section, we discuss in detail the operation of the differential pair with resistive local common feedback of Figure 1d and compare its performance characteristics with those of the circuit of Figure 1b.

2.1. Operation under Quiescent Conditions ($V_{i+} = V_{i-} = 0$)

This is illustrated in Figure 2a. Based on symmetry considerations it can be seen that resistors R have zero current ($I_R = 0$). Since no quiescent drop is found across these resistors transistors M2 and M2P behave as diode-connected transistors and the quiescent voltages V_{aQ}, V_{bQ} and V_{xQ} have all equal values $V_{aQ} = V_{bQ} = V_{DD} - V_{SGQ2}$, where V_{SGQ2} is the quiescent source-gate voltage of M2, M2P. Transistors M3 and M3P have a quiescent current $I_{D3Q} = MI_{BIAS}$ (assuming $(W/L)_3 = M(W/L)_2$). Notice that, as opposed to the circuit of

Figure 1a, R can have arbitrarily large values since given that no quiescent current flows through R its value does not affect the value of the quiescent voltages V_{aQ}, V_{bQ} and of the quiescent currents in M3, M3P.

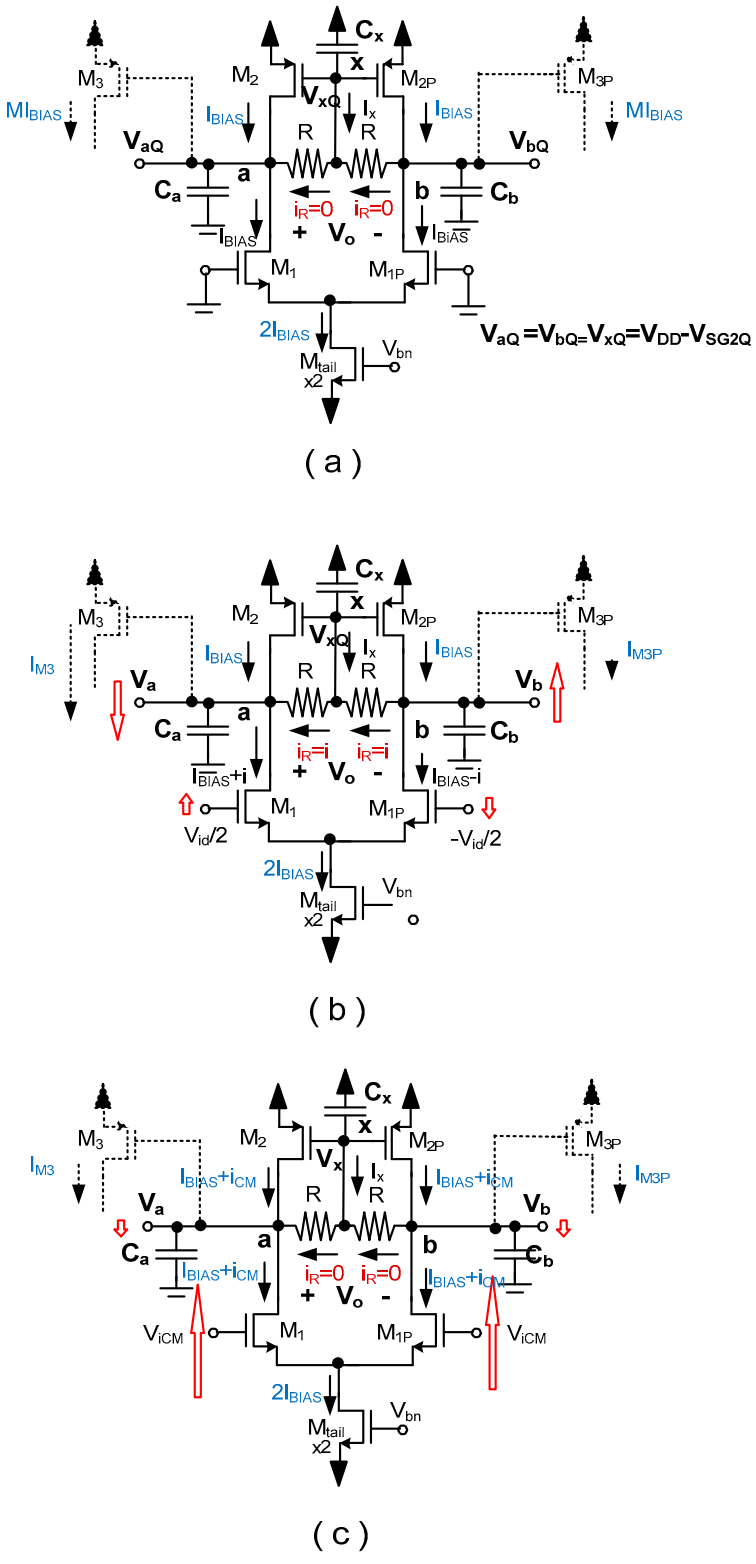


Figure 2. Operation of differential pair with RLCMFB: (**a**) Quiescent operation. (**b**) Operation with complementary differential inputs. (**c**) Operation with common mode inputs.

2.2. Differential Operation

The differential operation is illustrated in Figure 2b. Upon application of complementary differential input signals $V_{i+} = V_{id}/2$, $V_{i-} = -V_{id}/2$ equal but opposite AC signal currents $i = g_m V_{id}(t)/2$ are generated in M1 and M1P so that $i_A = I_{BIAS} + i$, $i_B = I_{BIAS} - i$. The signal currents "i" flow through resistors R generating complementary voltage changes $v_A = V_{aQ} - iR$, $v_B = V_{bQ} + iR$. The currents in M2, M2P, and the voltage V_x remain constant with their quiescent value: IM2 = IM2P = I_{BIAS}, $V_{xQ} = V_{DD} - V_{SGQ2.}$ It can be seen that node x behaves as a signal ground for differential signals. The effective load for differential signals is $R' = R||r_{o1}||r_{o2}$. The poles for differential signals at nodes a,b are given by $\omega_{pa,b} = 1/(R'C_{a,b})$ where $C_{a,b} = C_{gd2} + C_{gd1} + C_{gs3}$ are the parasitic capacitances at nodes a, b. The maximum value of R′ for R >> ro1, ro2 is given by $R' \approx r_{o1}||r_{o2}$. The gain A_d for differential signals is given by $A_d = V_o/V_{id} = g_{m1}R'$ (where $V_o = V_a - V_b$) and its maximum value (for R >> ro1||ro2) is given by $A_{dmax} = A_{int}/2$. This is similar to the gain of the high impedance active loaded circuit of Figure 1c. In practice, R can be used to set a compromise between the differential gain and the poles $\omega_{pa,b}$ at nodes a and b. Notice that C_{GS2} does not contribute to $C_{a,b}$ and with the drastic reduction of feature sizes in modern CMOS technologies parasitic capacitances $C_{a,b}$ are so small (in the 10 s of fF range) that the poles $\omega_{pa,b}$ remain at relatively high frequencies (MHz) even for large R′ values for $R >> r_{o1}||r_{o2}$ in which case $\omega_{pa,b} = 2/(r_o C_{a,b})$. For large R′ values voltages $V_{a,b}$ are subject to large negative variations $\Delta V_{a,bpeak} = -\Delta I_B R'$ which lead to large peak currents in M3, M3P, that can be much larger than the bias current I_{BIAS} (approximately by a factor of $K = (MI_{BIAS}R'/V_{DSSat})^2$ where $V_{Dssat} = V_{GS} - V_{TH}$ is the drain–source saturation voltage of M3, M3P). This feature allows, besides relatively high gain, improved gain-bandwidth and CMRR, also efficient class AB operation in amplifiers where the circuit of Figure 1d is used. This is shown in the following section.

2.3. Common Mode Operation

This is illustrated in Figure 2c. Upon application of common mode input signals $V_{i+}(t) = V_{i-}(t) = V_{icm}(t)$ and based again on symmetry considerations the currents I_R in R have zero value and the currents in M1, M1P acquire a small signal common mode component i_{cm}: where $i_{cm} \approx V_{cm}/2r_{otail}$. The load resistance for common mode signals is $R'_{cm} \approx 1/g_{m2}$; therefore, the voltages at nodes V_a, V_b and V_x are all equal and subject to very small variations $v_{acm} = v_{bcm} = v_{Xcm} = i_{cm}(1/g_{m2})$. The common mode gain at nodes a,b is then given by $A_{cma,b} = v_{a,bcm}/v_{cm} = \approx 1/(2\ g_{m2}r_{otail})$. If the output is taken differentially: $V_{ocm} = V_{oacm} - V_{obcm}$ the common mode gain is given by $A_{cm} = V_{ocm}/V_{icm} \approx [\Delta(1/g_{m2})/(2r_{otail})]$. Where $\Delta(1/g_{m2}) = (1/g_{m2}) - (1/g_{m2P})$ is the mismatch error in the values of $1/g_{m2}$ and $1/g_{m2P}$. Typically, using adequate analog layout techniques, mismatch errors $\Delta(1/g_{m2})$ are approximately two orders of magnitude smaller than $1/g_{m2}$: $\Delta(1/g_{m2}) \sim 0.01(1/g_{m2}) \approx 1/(100 g_{m2})$ which leads to $A_{cm} \sim 1/(200\ g_{m2}r_{otail})$. The common mode rejection ratio for the circuit of Figure 1d is very high and approximately given by $CMRR = A_d/A_{cm} = 100\ (g_{m1}R')(2\ g_{m2}r_{otail})$. The circuits of Figure 1a–c, have all the same load for common mode and for differential signals, and their common mode rejection ratio is given by $CMRR = (g_{m1}2r_{otail})/(\Delta R'/R') \sim 200\ g_{m1}r_{otail}$ or $CMRR \sim 200A_{int.}$ It can be seen that CMRR is a factor of $K_{enh} = g_{m1}R'$ higher for the RLCMFB circuit of Figure 1d than for the circuits of Figure 1a–c. The poles for common mode signals at nodes a, b in the circuit of Figure 1d are high-frequency poles given by $\omega_{pcma,b} = g_{m2}/C_{a,b}$. In Section 3, it is shown that this same improvement factor K_{enh} is achieved for GB, the open loop gain A_{ol} and the small and large signal figures of merit of OTAs where the circuit of Figure 1d is used as the input stage.

2.4. Some Remarks on the Operation of the Circuit of Figure 1d

The above discussion can be summarized by stating that in the circuit of Figure 1d, the load and poles for common mode signals and differential signals are very different. For common mode signals the load is low and has a value $R'_{cm} = (1/g_{m2})$ while the load for

differential signals can be high $R' = R||ro1||ro2$. For high R values, the differential gain A_d can take values close to the intrinsic gain while common mode signals have close to unity gain much lower than for the circuits of Figure 1a,c. In current CMOS technologies the poles $\omega_{pa,b}$ at nodes a, b for differential signals are medium-high frequency poles (~MHz) and for common mode signals the poles at nodes a,b are high-frequency poles. In the circuits of Figure 1a–c the load R' and the poles $\omega_{pa,b}$ for differential and common mode signals are the same $\omega_{pa,b}=1/(R'C_{a,b})$. For this reason, the CMRR of the circuit of Figure 1d is a factor of K_{enh} higher than for the circuits of Figure 1a–1c as will be shown in the next section.

Another important point to notice is that since no quiescent current flows in resistors R, their value does not affect the quiescent voltages V_{aQ}, V_{bQ} and it does not limit the peak swing at the output nodes a, b. The quiescent current in the output branch transistors, M3 and M3P, is accurately determined by the quiescent voltages V_{aQ}, V_{bQ} and has a value $I_{D3Q} = MI_{BIAS}$ independent of the value of R. The peak swing in the negative direction of voltages V_a and V_b is given by $\Delta va = -2I_BR'$. This can generate very large peak currents I_{M3PK} (much higher than the bias current I_{BIAS}) in transistors M3 and M3P driven by V_a and V_b. In order to save silicon area, as discussed in [1], resistors R can be implemented with transistors in triode mode which has the advantage of making them programmable.

3. Comparison of Non-Cascoded Conventional and Resistive Local Common Mode Feedback OTAs

Figure 3a shows a non-cascoded OTA using a conventional three-mirror architecture where the input stage corresponds to the circuit of Figure 1b. Figure 3b shows an OTA with the RLCMFB input stage of Figure 1d. This circuit was reported originally in [1]. As mentioned in Section 1, cascode transistors are usually avoided (especially in the output stage of an OTA) due to severe output swing limitations in current CMOS technologies that use sub-volt supplies (unless transistors operate in subthreshold). As discussed below, the lack of cascode transistors leads to very low open loop gain for the circuit of Figure 3a. It is shown in this section that resistive local common mode feedback boosts essentially the open loop gain, the gain-bandwidth product, the slew rate, CMRR and PSRR of OTAs allowing sufficient phase margin (greater than 50°) if phase lead compensation is used. Both OTAs of Figure 3 have a dominant pole at the output node $\omega_{pout} = 1/((r_{o3}||r_{o4})C_L)$ even with relatively low C_L values. The open loop gain of the conventional OTA of Figure 3a is given by $A_{ol} = (g_{m1}g_{m3}/g_{m2})\, r_{o3}||r_{o4} \approx g_m r_o/2 = A_{int}/2$ which is only on the order of 10 to 25 (20–28 dB). Its gain-bandwidth product (in rad/s) is given by $GB = A_{ol}\omega_{pout} = (g_{m1}/C_L)\,(g_{m3}/g_{m2}) = Mg_{m1}/C_L$ where $M = g_{m3}/g_{m2}$. The poles $\omega_{pa,b}$ at nodes a and b of the circuit of Figure 3a are given by $\omega_{pa,b} = g_{m2}/C_{a,b}$. These are high-frequency poles. For the common case $C_L >> C_{a,b}$ the poles $\omega_{pa,b}$ satisfy the condition $\omega_{pa,b} >> GB$ and the conventional OTA of Figure 3a has a phase margin close to 90º without compensation. The RLCMFB OTA of Figure 3b has an open loop gain $A_{ol} = g_{m1}R'g_{m3}r_{o3}||r_{o4} = g_{m1}R'A_{int}/2 = K_{enh}A_{int}/2$ where $K_{enh} = g_mR'$ is the gain enhancement factor introduced by the RLCMFB input stage and that for $R' >> r_{o1}||r_{o2}$ takes a value $K_{enh} = g_{m1}r_{o1}||r_{o2} = A_{int}/2$. It has a gain-bandwidth product $GB = K_{enh}\, g_{m3}/C_L$ which is also a factor of K_{enh} larger than the GB of the circuit of Figure 3a. Even for values $R' >> r_{o1}||r_{o2}$ for which maximum K_{enh} is achieved, the poles at nodes a, b given by $\omega_{pa,b} = 2/(r_oC_{a,b})$, have values that for the typical load capacitances $C_L >> C_{a,b}$ are close to GB in modern CMOS technologies. If necessary, their phase shift at the unity gain frequency can be partially compensated using phase lead compensation. This uses just a resistor R_s in series with the output terminal that introduces a left s-plane zero with value $\omega_z = 1/(R_sC_L)$ in the open loop gain. The phase of the zero subtracts from the phase of poles $\omega_{pa,b}$ at the unity gain frequency allowing sufficient phase margins PM > 50°.

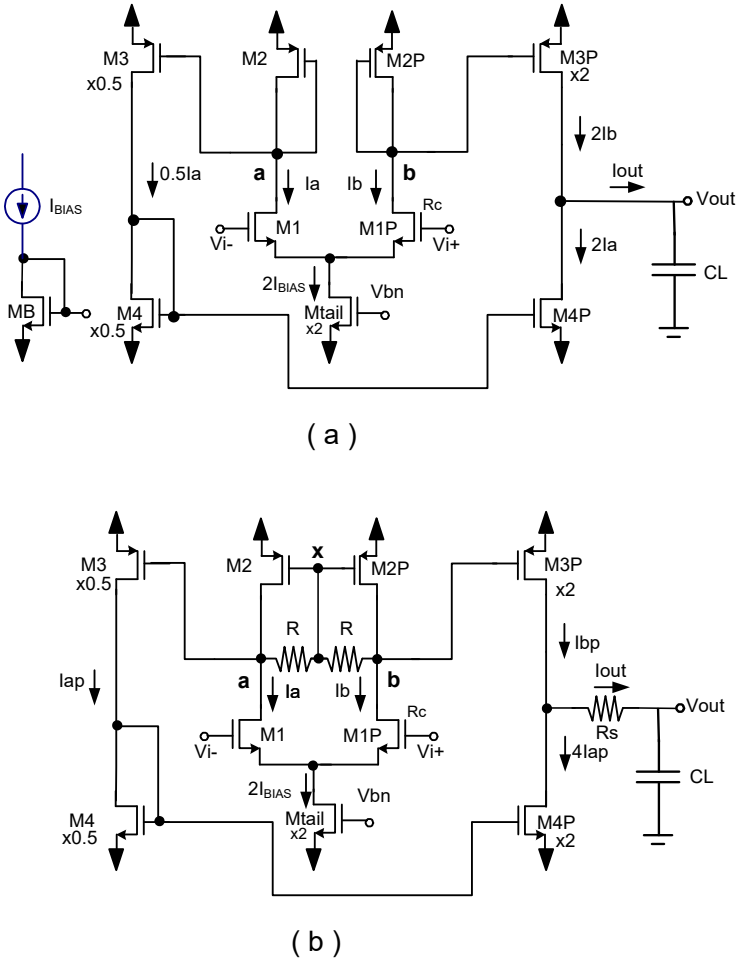


Figure 3. One stage non-cascoded OTAS. (**a**) Conventional three current mirror OTA. (**b**) OTA with resistive local common mode feedback in input stage.

Summary

In current CMOS technologies, the open loop gain and GB are enhanced by the factor K_{enh} by utilization of RLCMFB and even for large K_{enh} values it is possible to obtain sufficient phase margin using phase lead compensation. Miller (or two-stage) op-amps have a GB characterized by GB = g_{m1}/C_c (in rad/s) where C_c is the Miller compensation capacitor that in a typical design is selected with a value $C_c = C_L$ in which case GB = g_{m1}/C_L. Notice that the OTA of Figure 3b has also a GB enhanced by the same factor K_{enh} with respect to the conventional Miller op-amp. The CMRR of the OTAs of Figure 3 corresponds approximately to CMRR = $(g_{m1}2r_{otail})/(\Delta R'/R')$~$200(g_{m1}R')(g_{m2}r_{otail})$ for the circuit of Figure 3b and CMRR~200 $g_{m1}r_{otail}$ for the circuit of Figure 3a. It can be seen that CMRR is also a factor of K_{enh} higher for the circuit of Figure 3b than for the circuit of Figure 3a. Table 1 summarizes expressions for the performance characteristics of the OTAs in Figure 3.

Table 1. Basic performance characteristics of OTAs of Figure 3.

Parameter Expression	Conventional OTA of Figure 3a	OTA with RLCMFB of Figure 3b
A_{ol} (V/V)	$(g_{m1}g_{m3}/g_{m2})\ r_{o3}\|\|r_{o4}$~$A_{int}/2$	$g_{m1}R'g_{m3}\ (r_{o3}\|\|r_{o4})$~$(A_{int}/2)2$
GB (rad/s)	$(g_{m1}/C_L)\ (g_{m3}/g_{m2})$~$g_m/CL$	$g_{m1}R'g_{m3}/C_L)$~$A_{int}g_m/C_L$
SR (V/s)	$2I_{BIAS}/C_L$	$MI_{BIAS}(I_{BIAS}R/V_{DSSa}t)^2/C_L$
CMRR	~200 $g_{m1}r_{otail}$	~$200(g_{m1}R')(g_{m2}r_{otail})$

Figure 4 shows simulations of the open loop response of the OTAs of Figure 3 in 130 nm CMOS technology with C_L = 5pF, dual supply voltages $V_{DD} = -V_{SS}$ = 0.6 V, I_{BIAS} = 5 µA, R = 600 kΩ, R_s = 0.4 kΩ, W/L = 5/0.26 (µm/µm) for NMOS transistors and PMOS transistors. Tail and output transistors Mtail, M3P and M4P are scaled by a factor of k = 2, the left branch transistors, M3 and M4, are scaled by a factor of k = 0.5. It can be seen that the open loop gain and phase margin of the conventional OTA have values A_{olcnv} = 27 dB and PM_{cnv} = 90.8°, the OTA with RLCMFB of Figure 3b has enhanced open loop gain $A_{olRLCMFB}$ = 50.3 dB and a phase margin PM_{RLCMFB} = 62.2°. The open loop gain of the RLCMFB OTA is 23.1 dB higher than for the conventional OTA (a factor of 14.1 in magnitude). The dominant (output) pole for both OTAs (determined by C_L) has a value of f_{pout} = 380.2 kHz. The unity gain frequencies of the conventional and RLCMFB OTAs are at 8.77 MHz and 72.4 MHz (a factor of 8.32 higher). Notice that due to the utilization of phase lead compensation with R_s, the RLCMFB OTA of Figure 3b has approximately a one pole open loop response shifted upwards with respect to the response of the conventional OTA, and for this reason, open loop gain and unity gain enhancement factors are similar (11.4 and 8.9, respectively).

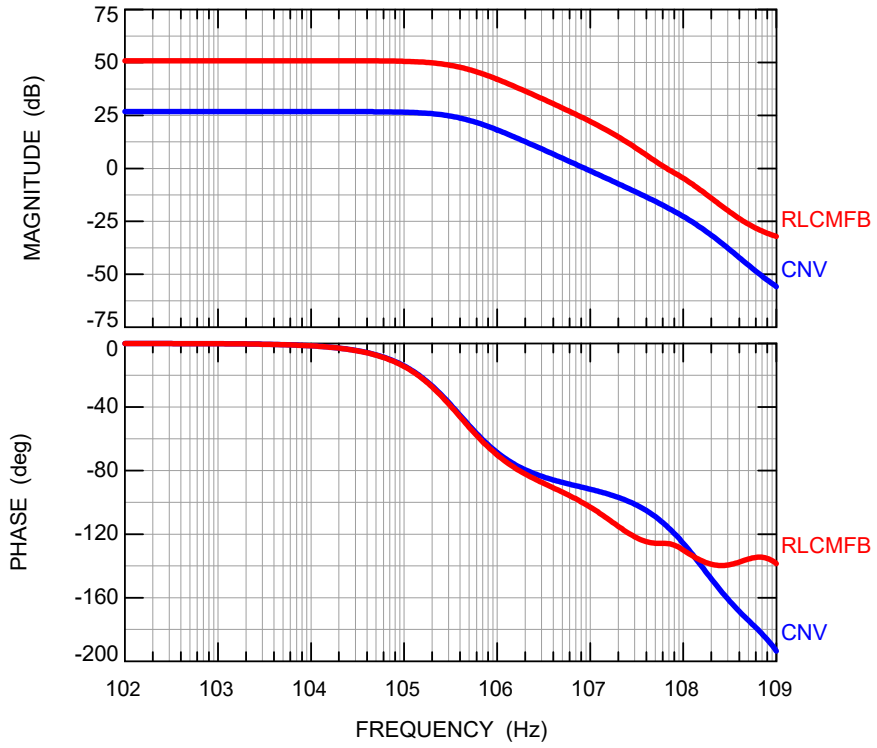


Figure 4. Open loop response AC responses of circuits of Figure 3.

Figure 5 shows simulations of the closed loop voltage follower response. The bandwidths of the conventional and RLCMFB OTAs are 8.3 MHz and 72.4 MHz, respectively.

Figure 6 shows the transient pulse response (output voltages and load currents) of the circuits of Figure 3. The peak positive/peak negative load currents of the conventional and RLCMFB OTAs are 32/23 µA and 357/352 µA, respectively. The corresponding positive and negative slew rates are 71.4/70.4 V/µs and 6.4/4.6 V/µs, respectively. The SR of the RLCMFB OTA is approximately symmetrical and almost two orders of magnitude (a factor of 76.5) larger than the SR of the conventional OTA. Simulations of CMRR, positive and negative PSRR shown in Figures 7–9 below were performed by introducing 2% mismatches in the W/L of M2 and M2P and in the R and W/L values.

Figure 7 shows the frequency response of CMRR of the circuits of Figure 3. It can be seen that the conventional and RLCMFB OTAs have CMRR values of 54 dB and 80 dB,

respectively. Notice that the RLCMFB OTA shows an improvement of 26 dB in CMRR with respect to the conventional OTA.

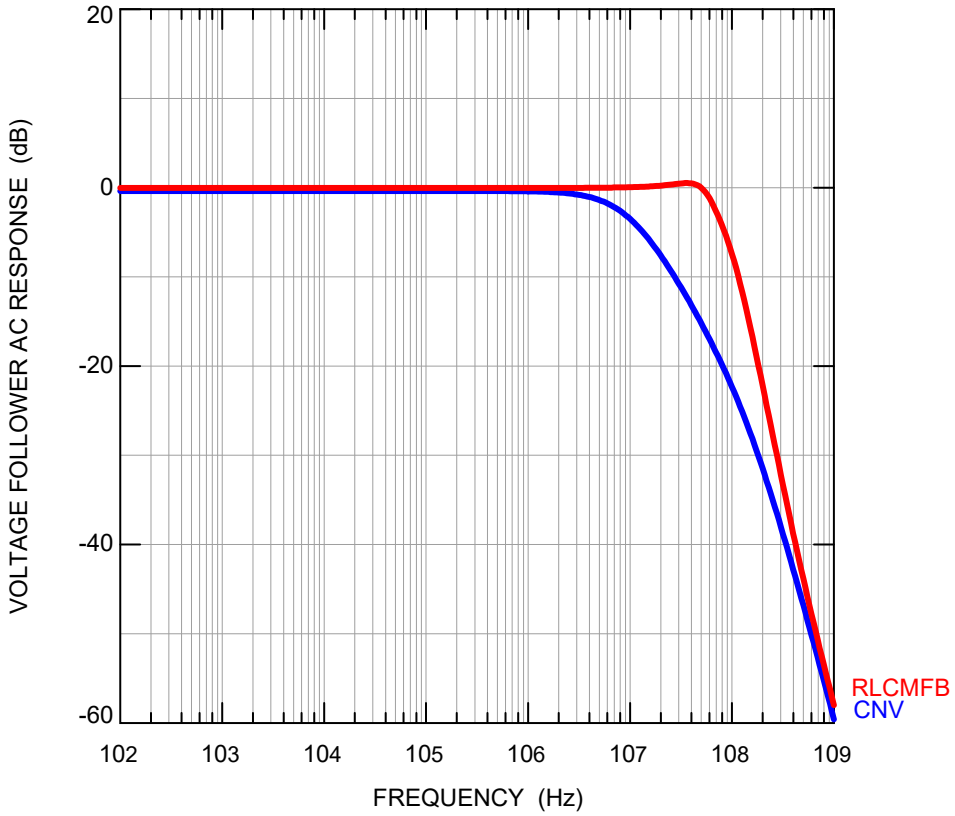


Figure 5. Voltage follower AC responses of circuits of Figure 3.

Figure 8 shows the positive PSRR (with respect to VDD) of the circuits of Figure 3. The conventional OTA has a PSRR+ of 54.1 dB which is 20.2 dB lower than the PSRR+ of the RLCMFB OTA with a PSRR+ of 74.3 dB.

Figure 9 shows the negative PSRR of the circuits of Figure 3. The conventional OTA and RLCMFB OTAs have a negative PSRR− of 28 dB and 51.8 dB, respectively. The negative PSRR− enhancement of the RLCMFB OTA is 23.8 db in this case.

Table 2 shows a comparison of the performance characteristics of the conventional OTA and the RLCMFB OTA of Figures 3a and 3b, respectively. It can be seen that the RLCMFB has essentially improved performance over the conventional OTA. Table 3 shows a comparison of the performance characteristics of the RLCMFB OTA of Figure 3b to the OTAS literature. It can be seen that the circuit of Figure 3b has higher small signal, large signal and global figures of merit (FOM_{SS}, FOM_{LS} and FOM_{GLB}) than all other OTAS in Table 2 and also than the conventional OTA.

Table 2. Comparison of performance characteristics of OTAs of Figure 3.

	Conventional OTA Figure 3a	**RLCMFB OTA Figure 3b**
C_L (pF), R_s(kΩ)	5 pf, 0	5 pF, 0.4
W/L PMOS, and NMOS (μm/μm)	5/0.26	5/0.26
V_{os} (mV)	−12.4	0.9
A_{ol} (dB)	27.2	50.3
PM (°)	90.8	62.2

Table 2. *Cont.*

	Conventional OTA Figure 3a	**RLCMFB OTA Figure 3b**
P_{diss} (uW)	30	30
f_{pout} (MHz)	0.3802	0.3802
f_u (MHz)	8.7	72.4
P_{dis}(uW)	30	30
BW_{VF}	8.3	75.9
GB (MHz)	8.7	124
SR+/SR− (V/µs)	6.4/4.6	71.4/70.4
CMRR (dB)	54	80
PSRR+ (dB)	54.1	74.3
PSRR− (dB)	28	51.8
Input noise at 1kHz $nV/(Hz)^{1/2}$	26	20
I_{outPk+}/I_{outpk-} µA	32/23	357/352
FOM_{SS} (MHz pF/µW)	1.45	12.1
FOM_{LS} (V/µs)pF/µW	0.77	11.7

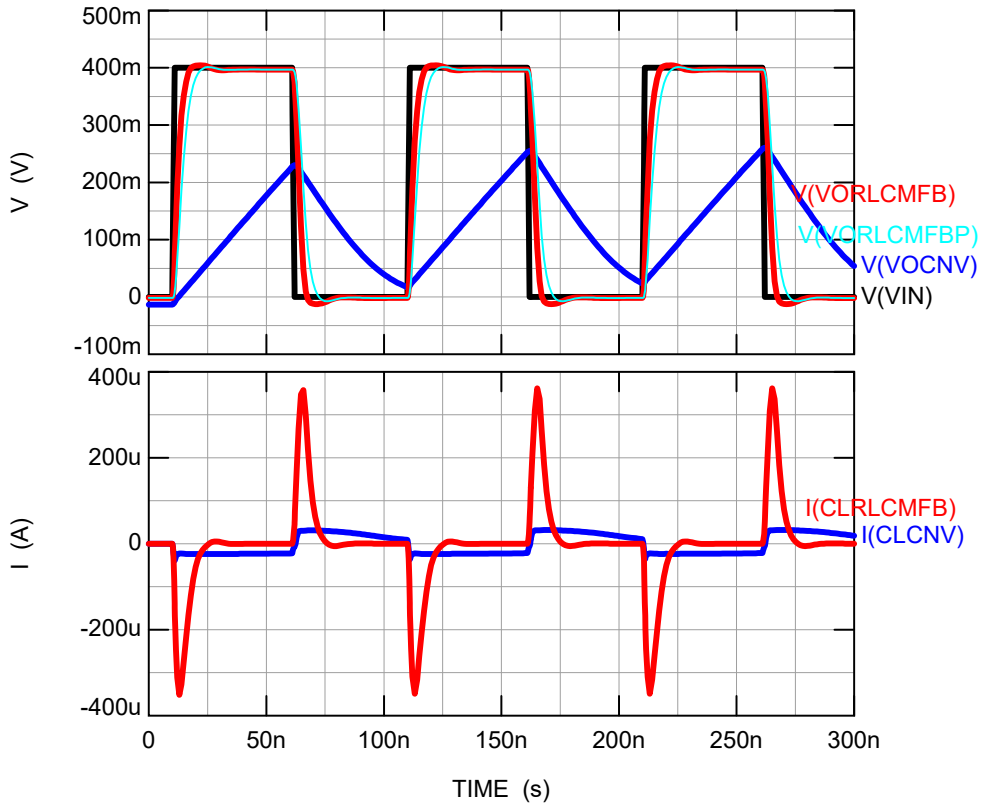


Figure 6. Transient response of circuits of Figure 3. Top: input and output voltages, bottom: output currents.

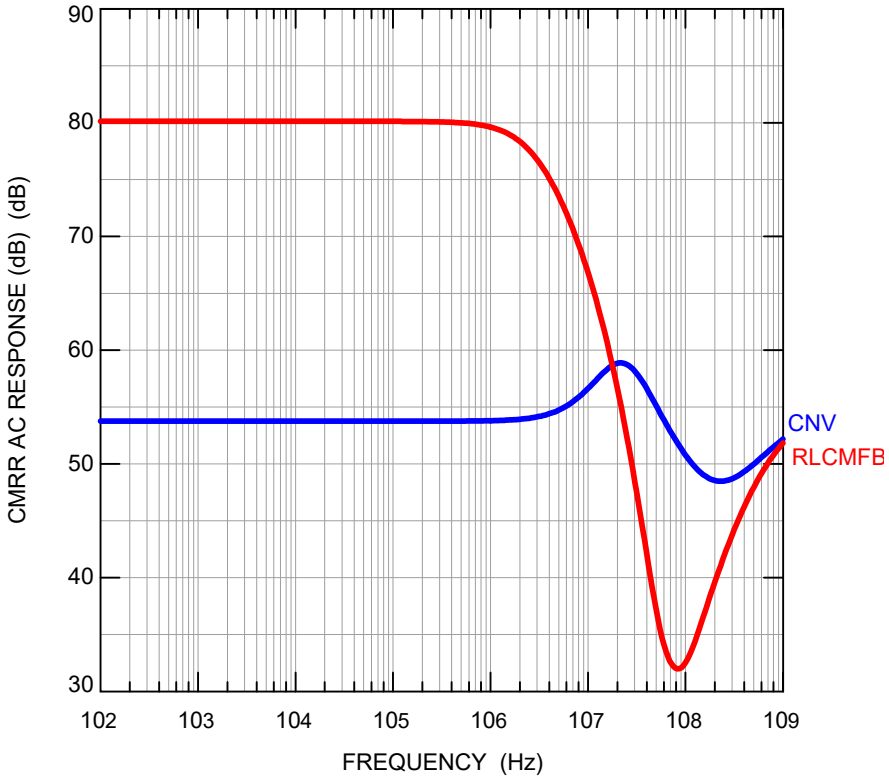


Figure 7. CMRR response of circuits of Figure 3.

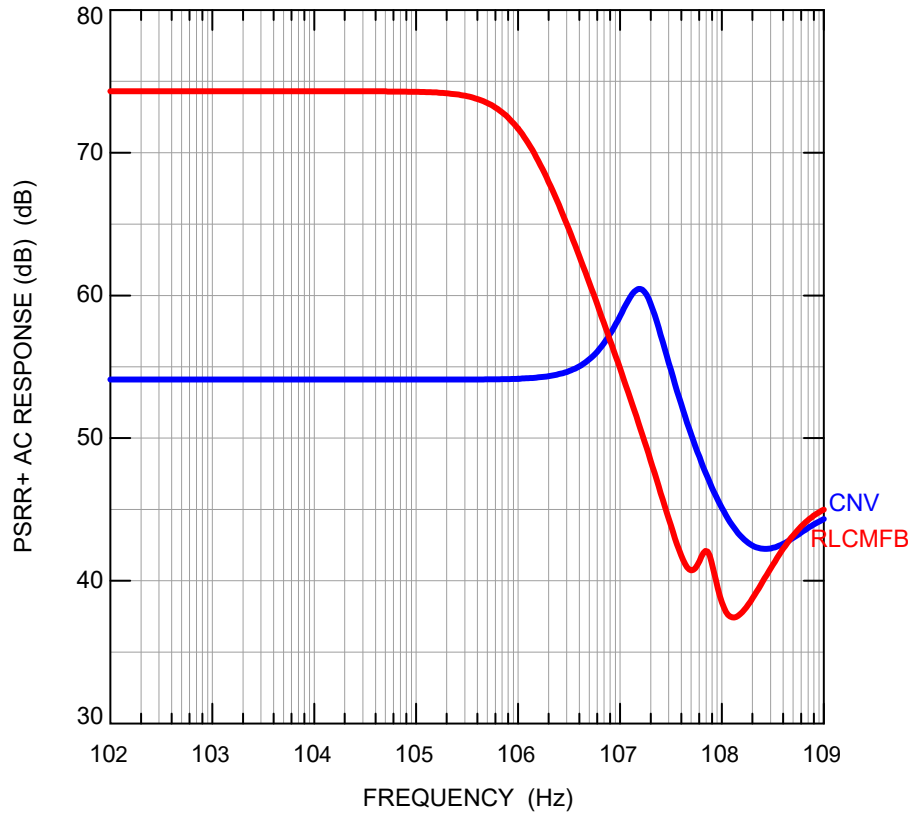


Figure 8. Positive PSRR of circuits of Figure 3.

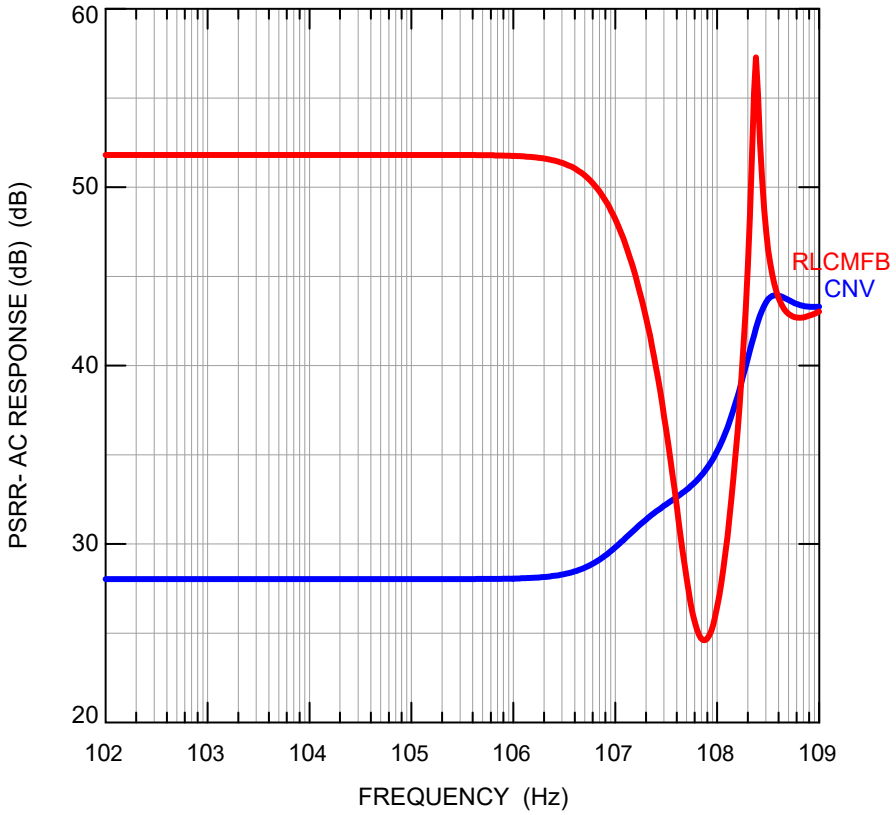


Figure 9. Negative PSRR of the circuits of Figure 3.

Table 3. Comparison of performance characteristics of OTA of Figure 3b to other OTAS in the literature.

Parameters	**[2] 2017**	**[3] 2019**	**[4] 2019**	**[5] 2020**	**[6] 2020**	**[7] 2021**	**OTA with RLCMFB of Figure 3b**
CMOS process (nm)	180	180	180	180	180	180	130
Vsupply (V)	0.5	1.2	1.8	1.8	1.8	1.8	1.2
ItotQ (μA)	7.9	700	530	260	-	400	22.5
C_L (pF)	1	10	5	5.6	8	18	5
Aol (dB)	50	75	105.5	90.1	68	73.4	50.3
GB (MHz)	16.6	185	231.7	157	172.5	224	72.4
PM (degree)	72	71	53	62.1	48.7	69	62.2
SR+/SR− (V/μs)	4.25	99	13.2	64	212	110	71.4/70.4
FOM_{SS} (MHz pF/μW)	4.2	2.2	1.21	1.87	1.21	5.6	12.1
FOM_{LS} ((V/μs)pF/μW)	1.076	1.17	0.007	0.76	0.34	2.75	11.7
$FOM_{GLB} = (FOM_{LS}FOM_{SS})^{1/2}$	2.12	1.61	0.09	1.19	0.64	4	11.9

In [8–47] various applications of the resistive local common mode feedback technique to enhance circuit's performance have been reported. Some of these applicatoins are discussed with detail in Sections 4–6 below.

4. Super Class AB OTAs

The minimum of the positive and negative peak output currents determine the slew rate which is a measure of the large signal speed of an OTA while the gain-bandwidth

product is a measure of the OTA speed for small signals. Both of them are important. There are situations where an OTA loaded with a large capacitance and/or low load resistance (that require large peak load currents) has a high bandwidth but it can handle only very small amplitude signals within its bandwidth because the slew rate, is very small. Super class AB OTAs can handle situations where an OTA is required to operate with large C_L and/or low R_L values (that require large peak output currents) with large amplitude within the full bandwidth of the OTA and maintaining a low quiescent power dissipation. In this section, we discuss the implementation of super class AB OTAs with enhanced open loop gain and GB using the combined effect of both gain and SR enhancement achieved with RLCMFB in conjunction with current boosting provided by a class AB differential pair. Several super class AB OTA architectures have been reported in [10–14,20,30–32,37,41]. They are characterized by very high current efficiency CE = I_{outpk}/I_{BIAS} (defined here as the ratio of the peak output current, I_{outpk} to the bias current I_{BIAS}) and by very large signal figures of merit FOM_{LS}. Some of the reported structures have low open loop gain in current CMOS technologies but this limitation can be overcome by implementing them with RLCMFB. They deliver output load currents that can be 2 to 3 orders of magnitude larger than the bias current I_{BIAS} and do not rely on the utilization of inverters connected to the output terminal (inverters at the output terminals have been used to achieve very large transient output currents. They are turned on when the op-amp is slewing but they can introduce spikes and distortion. Figure 10c shows a super class AB OTA derived from the RLCMFB OTA of Figure 3b by using a class AB differential pair according to the scheme reported in [48]. This is performed by replacing the tail current source Mtail of the differential pair with a Cascoded Flipped Voltage Follower. The Cascode Flipped Voltage Follower (FVF) was reported in [49]. It is a high-swing FVF that uses local negative feedback, by means of cascode transistor MC and Msink, to generate a very low impedance node at VG. Transistor MFVF operates as a floating battery V_{GSQ}. The input common-mode detector (ICMDT) uses very large resistive elements Rlarge (Figure 10b). It is implemented with quasi-floating gate transistors [50] and small capacitances in parallel as shown in Figure 10b. These are used to detect the common mode input voltage V_{iCM} of the OTA terminals Vi+ and Vi−. This voltage is applied at the gate of MFVF and is followed by VG causing node VG to follow common-mode input signals. The local feedback in the cascoded FVF causes VG performs as a very low impedance node (tens of Ωs) for differential signals and as a high impedance node (hundreds of kΩs) for common-mode input signals. The cascoded FVF (shown in red in Figure 10c) in conjunction with the ICMDT implements the scheme reported in [48] and shown in Figure 10a. M1 and M2 perform in this circuit as a class AB differential pair where transistors M1, M1P can generate currents Ia, Ib much larger than $2I_{BIAS}$ while in the conventional differential pair transistors M1, MP can only generate maximum currents with value $2I_{BIAS}$. The class AB differential pair of Figure 10a,c has a small signal transconductance gain with value g_{m1} for differential signals and very low transconductance gain ($<1/2r_{osink}$) for common mode signals.

The local negative feedback causes the class AB differential pair to have higher common mode rejection than the conventional differential pair. Under quiescent conditions, the gate-source voltage of MFVF is the same as that of, M1 and M1p, and sets their quiescent currents. For differential input signals Vd the gate-source voltages in M1 and M1P take values $V_{GS1} = V_{GSQ} + V_d/2$ and $V_{GS1P} = V_{GSQ} - V_d/2$. This is not restricted to small signal operations. It also applies to large signals.

Figure 11 shows the transconductance characteristics I_{out} vs. V_{in} of the super class AB OTA of Figure 10 biased with I_{BIAS} = 0.25 μA, for the RLCMFB OTA of Figure 3b and for the conventional OTA of Figure 3a. Simulations were performed in 130 nm CMOS technology with PMOS and NMOS transistor dimensions W/L = 5/0.26 (μm), output transistors scaled by a factor of 2, R = 2000 kΩ, R_s = 2 kΩ C_L = 5 pF C = 1pF, $V_{DD} = -V_{SS}$ = 0.6 V applying complementary input signals $V_{i+} = V_{in}/2$, $V_{i-} = -V_{in}/2$ and with the OTA outputs connected to ground. It can be seen that the super class AB OTA delivers ±400 μA peak output currents, the RLCMFB OTA delivers ±100 μA peak output currents while the

conventional OTA delivers only +1.5 µA and −2.5 µA peak output currents. The open loop gains of the super class AB and the RLCMFB OTAs are identical to those shown in Figure 4 (in red) and are not shown for the sake of space.

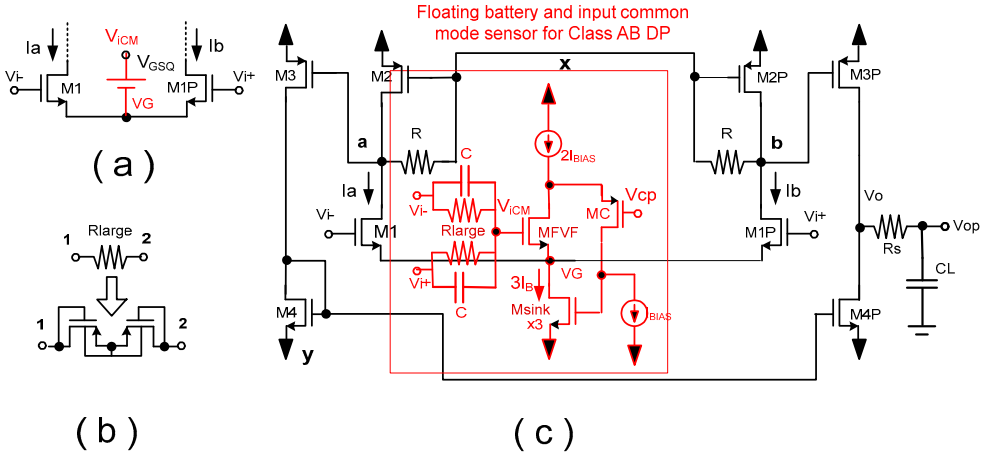


Figure 10. High gain super class AB OTA using the combined current boosting effect of RLCMFB and of class AB differential pair. (**a**) Conceptual implementation of class AB DP using the floating battery. (**b**) Implementation of very large resistive elements using quasi-floating gate transistors. (**c**) Transistor level implementation of super class AB OTA.

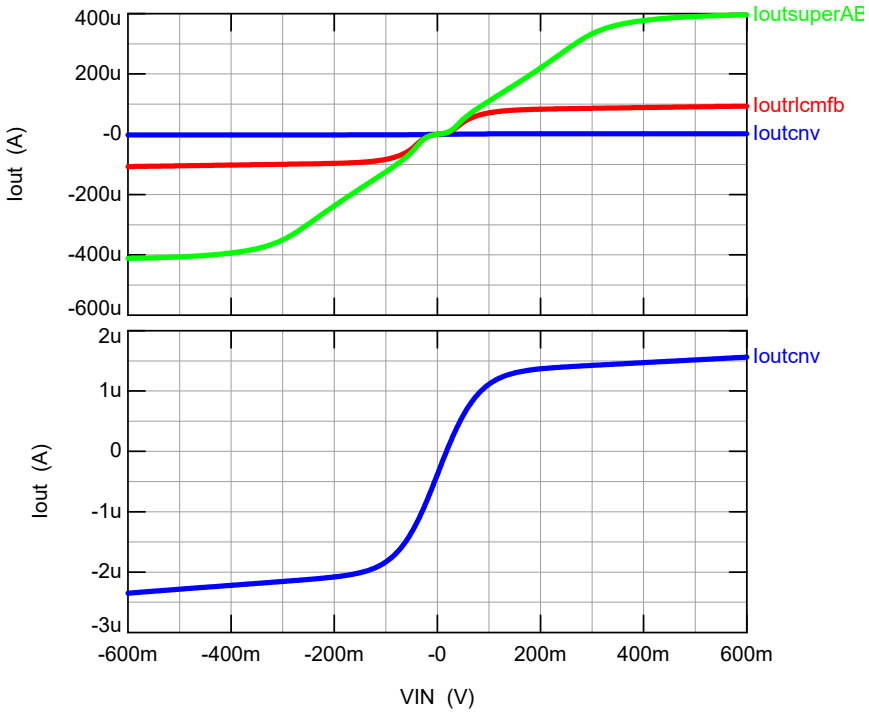


Figure 11. Transconductance characteristics of conventional OTA of Figure 3a (blue trace), RLCMFB OTA of Figure 3b (red trace) and super class AB OTA of Figure 10 (green trace).

Figure 12 shows the CMRR frequency response of the same circuits. The OTAs were biased in this case with I_{BIAS} = 5 µA, a 1% mismatch in the W/L of transistors and in R values was introduced to mimic fabrication mismatches and obtain realistic values of CMRR. The CMRR of the super class AB OTA, the RLCMFB OTA and the conventional OTA are 89 dB, 80 dB and 54 dB, respectively. The increased CMRR of the super class AB OTA is caused by the local feedback in the class AB DP. This increases the effective impedance for common mode signals at node VG by approximately a factor of 2.8 (or 9 dB).

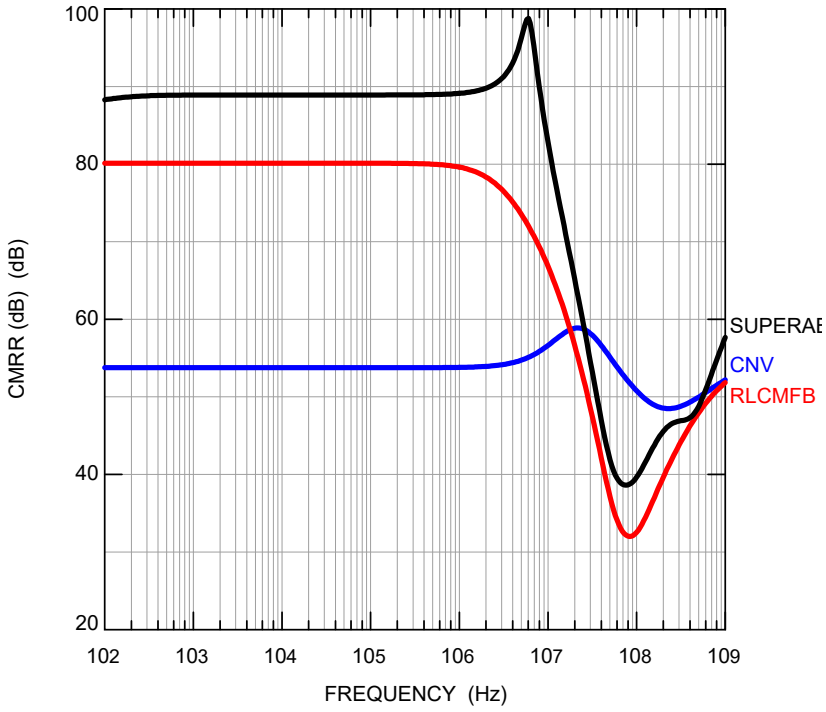


Figure 12. CMRR of super class AB OTA of Figure 10, of RLCMFB OTA of Figure 3b and of conventional OTA of Figure 3a simulated with I_{BIAS} = 5 µA.

5. Feedforward Amplifiers

The RLCMFB differential pair of Figure 1d can be also used to implement feedforward amplifiers with high gain and bandwidth. Figure 13 shows the scheme of a two-stage feedforward amplifier followed by an output buffering stage. The first two cascaded sections have a gain $A_{1,2} = g_m R'$ and bandwidth (in Hz) $BW_{1,2} \approx (1/2\pi)\,(1/(R'C_{a,b}))$. These two stages correspond to the DPs with RLCMFB of Figure 1d. The output buffer (with close to unity gain) is used to drive the capacitive load $C_{L.}$ It has a differential pair with resistive gain degeneration R3 and common mode feedback resistive loads R2. It has a gain Abuf = (R2||ro2)/((1/gm1 + R3/2) and a bandwidth (in Hz) BWbuf ≈ (1/2π)(1/(R2CL)). The current sources, Ishift and Ishiftbuf, are used to obtain quiescent values at the output nodes VoQ1,2 = VDD − VSGQ2 − RIshift/2, VoQbuf = VDD − VSGQ2buf-RIshiftbuf/2 close to zero Volts to maximize output signal swing. It is possible to achieve higher gains by adding more gains stages. This circuit does not require compensation since it does not use global feedback. The amplified input DC offset can saturate the outputs. In order to prevent this, the gain stages of this circuit should be AC coupled or if a wideband gain starting from very low frequencies (close to DC) is required, a servo-loop (similar to the one reported in [51]), that attenuates gain for DC signals, should be connected between the output of the second stage and the input of the first stage.

The circuit of Figure 13 was simulated in 130 nm CMOS technology with I_{BIAS} = 5 µA in the first and second stages and 20 µA in the output buffer stage. Dual supplies $V_{DD} = -V_{SS}$ = 0.6 V, and dimensions for PMOS and NMOS transistors W/L = 5/0.26 (µm) were used. The dimensions and bias currents of the output stage transistors were scaled by a factor of 4. Values R = 300 kΩ, R2 = 8.5 kΩ, R3 = 10 kΩ and C_L = 2 pF were used. Figure 14 shows the frequency response of the circuit. Figure 15a shows the transient response to a triangular wavefrom. Figure 15b shows the pulse reponse. The gain of the circuit is A = 46.4 dB, the bandwidth BW = 7.2 MHz and the power dissipation P_{dis} = 72 µW. This corresponds to a small signal figure of merit FOM_{SS} = A BW C_L/Pdis = 40 MHzpF/µW.

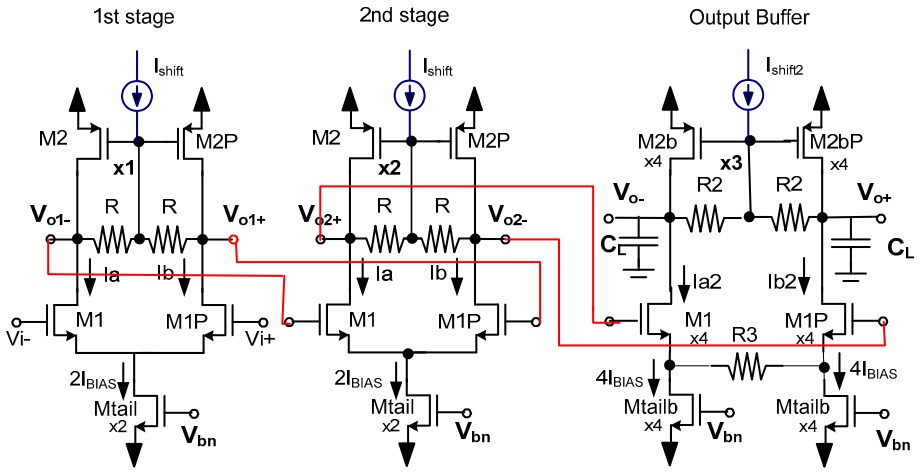


Figure 13. Feedforward high gain multistage amplifier consisting of two cascaded gain stages and a buffering output stage.

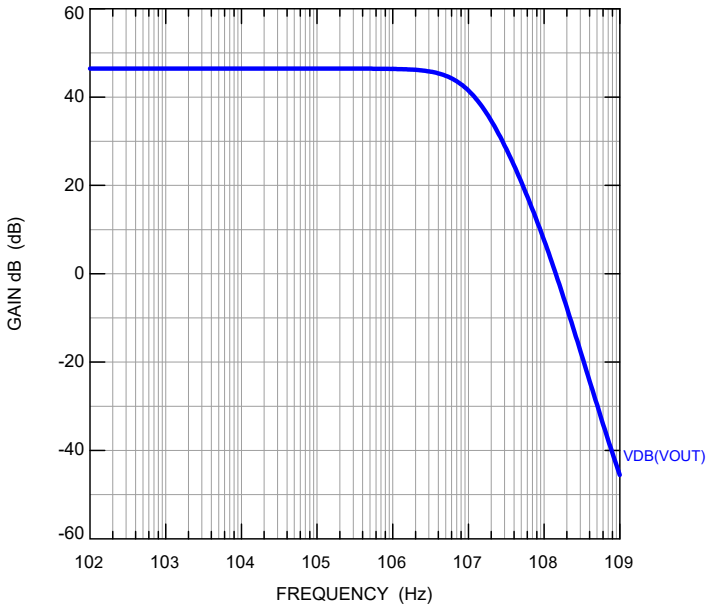
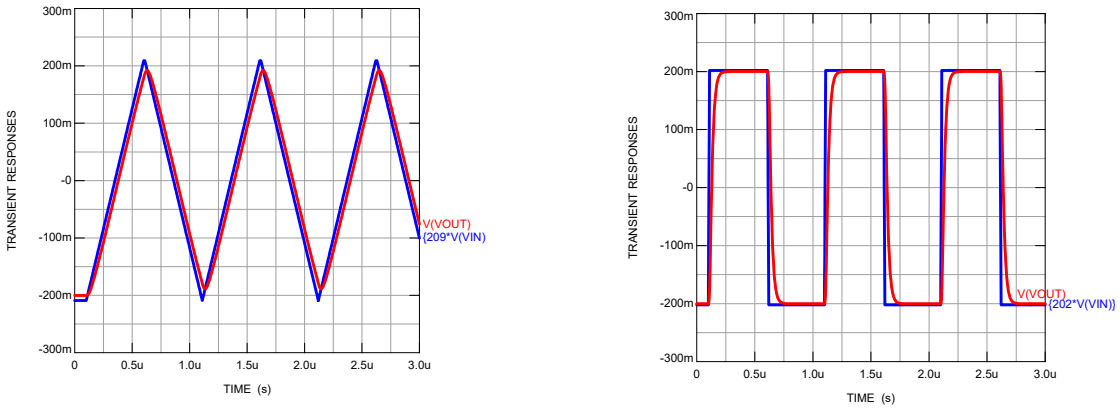


Figure 14. Frequency response of circuit of Figure 13.



(**a**) (**b**)

Figure 15. Transient response of circuit of Figure 13 (**a**) with triangular input signal, (**b**) with pulse input signal.

6. Other Applications

Since the RLCMFB technique to increase slew rate and gain was reported in [1], as well as other applications in [8,9] many other applications that achieve performance enhancement in analog circuits using this technique have been reported [10–47]. These include the utilization of capacitive (instead of resistive) local common mode feedback using floating gate transistors as shown in Figure 16b [12,15,16,22,23]. This is in order to reduce the silicon area if resistors R >> ro1 | | ro2 are required to achieve maximum K_{enh} values. Ultra high gain op-amps [39], Bulk driven and multistage operational amplifiers [29,35,45], rail-to-rail sample and hold circuits [18], buffers for high-density microelectrode arrays [24], LDOs [27], delta-sigma modulators [34], VGAs [36], gain and GB improved common mode feedback networks used in fully differential op-amps [30], etc. Other possible applications include the implementation of high frequency, high Q bandpass amplifiers using inductive common mode feedback (Figure 16c) where resistors are replaced by inductors and capacitors Ca, Cb by varactors C_L to achieve tunable resonant frequencies $\omega_{res} = 1/(LC_L)^{1/2}$ in a multistage feedforward configuration similar to the one shown in Figure 13.

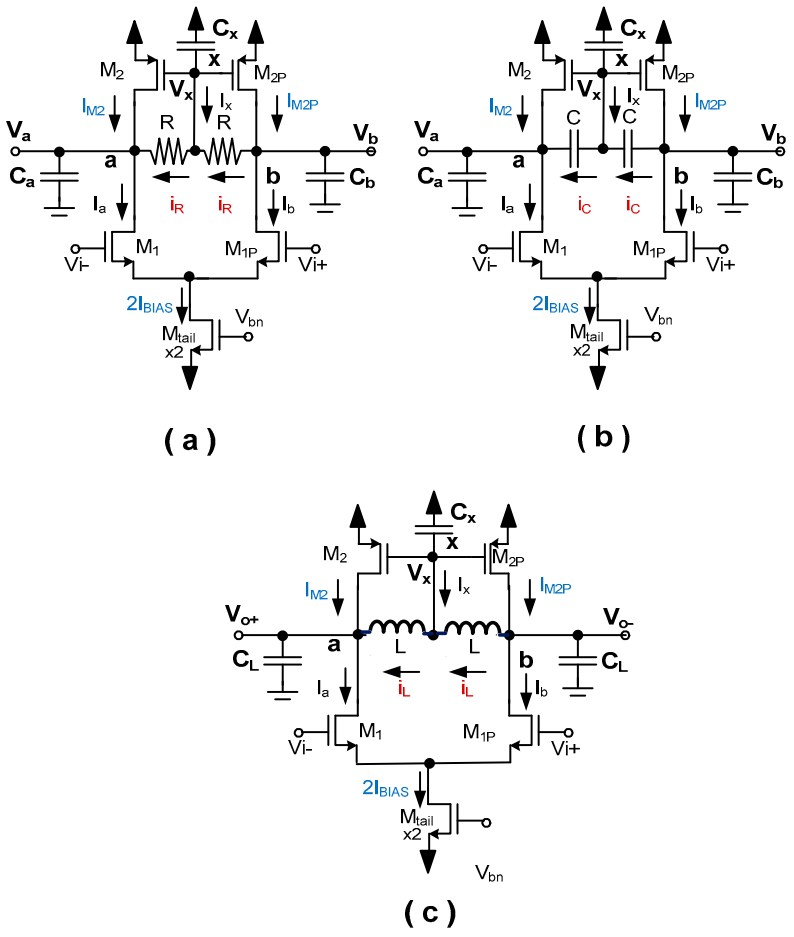


Figure 16. (**a**) Differential pair with resistive local common mode feedback. (**b**) Differential pair with capacitive local common mode feedback. (**c**) Differential pair with inductive local common mode feedback.

7. Conclusions

In this paper, a review of the resistive local common mode feedback technique and its application to improve amplifier's performance was presented. It was shown that this technique is especially appropriate in current deep submicrometer CMOS technologies to essentially improve open loop gain, GB, SR, CMRR and PSRR of amplifiers without

increasing power dissipation or supply requirements and by adding small additional circuit complexity.

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