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UIS Characterization of LOCOS-Based LDMOS Transistor Fabricated by 1 µm CMOS Process †

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Abstract: This paper investigates the ruggedness of an n-type LDMOS under single shot unclamped inductive switching (UIS) stress conditions. We present a detailed method to define the electrothermal safe operating area (SOA), and the physics of the failure mechanism is described. We conclude that the device robustness depends mainly on the gate bias, much less on the pulse duration on millisecond range, the inductive load value, or the initial operating temperature, although the Kirk effect is always present under all conditions. However, the failure mechanism fundamentally changes to pure avalanche breakdown under short pulses.

Keywords: LDMOS; TCAD; UIS; ruggedness

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1. Introduction

Laterally diffused MOSFET transistors (LDMOS) are the primary choice for high-voltage (HV), RF/microwave applications. Even when the process nodes are downscaled, and variants of LDMOS designs are reported, the usage of older, much more robust technologies are still adopted in the market [1–6].

Such technologies rely on the extension of the drift region, the reduced surface field principle (RESURF), the local oxidation of silicon (LOCOS), and the separation field oxide (FOX) to achieve a balance between the off-state breakdown voltage (BV) and the on-state resistance (R_{ON}). That balance is commonly known as the figure of merit (FoM), which is calculated often using Baliga's equation. Additionally, by using a standard CMOS process, the integration of such devices along the high-performance (HP) circuits is possible with little additional effort [7].

However, that integration comes with the cost of a low BV, as is the case in the device under test (DUT). The low BV value; of 21 V; raises the concern of catastrophic failure during switching, because LDMOS transistors have primarily an inductive load, which stresses the device at the switching moment under a high-power value, in addition to small parasitic inductive loads, which could have the same effect [8]. The purpose of this study is to assess whether the DUT could sustain such sudden power dissipation. The LDMOS design is a conflicting process between a wide SOA, high BV, and low R_{ON}.

Defining the SOA depends heavily on the final application, as the final implementation requires different standards, as such, the breakdown mechanism will change accordingly [9]. Under short pulses, the device unavoidably will be under electrostatic discharge (ESD), as a charge device model (CDM), human body model (HBM) conditions, machine model (MM), and/or transmission line measurement (TLP), or even high-power electromagnetic interference (EMI) [10,11]. The stress time range is of several pico, nano, or microseconds.

In this case, the breakdown is purely electrical. The SOA upper-boundary is when the device shows negative resistance [12,13], which is due to the electrical onset of the NPN transistor [14,15].

Under pulses of a few milliseconds and up to tens of seconds ranging in values, such as the polarity reversal of an H-Bridge in smart-power ICs [16], the breakdown is electrothermal, which is due to the impact-ionization and thermal generation, a consequence of the onset of the parasitic NPN transistor and its Kirk effect [17].

Furthermore, longer pulses, hundreds of seconds up to years of stress, are often categorized as hot carrier injection (HCI) degradation, which affects the electrical parameters non-catastrophically [18–20], although, it also could be a combination of HCI and a thermal degradation component called bias temperature instability (BTI) [21]. This work addresses some aspects of the former two cases, as the layout does affect the robustness.

This paper is organized as follows: Section 2 describes the device and the simulation setup. Section 3 we presents the various stress results and discusses the physics of the failure mechanism, and concludes in Section 4.

2. Device and UIS Set-Up

The DUT is obtained from a process simulation, using Sentaurus tool [22], following a 1 µm CMOS flow, adopted in CDTA's cleanroom [23,24]. It uses a 15 nm thick gate oxide and 787 nm FOX using the LOCOS separation feature. We shorted the source and the body to reduce the effect of parasitic BJTs, which is one of the causes of avalanche generation. The DUT, shown in Figure 1a, is where we added the thermodes required for the electrothermal simulation. We extended the simulated substrate thickness to 100 µm, unlike regular simulations to allow a realistic dissipation of heat.

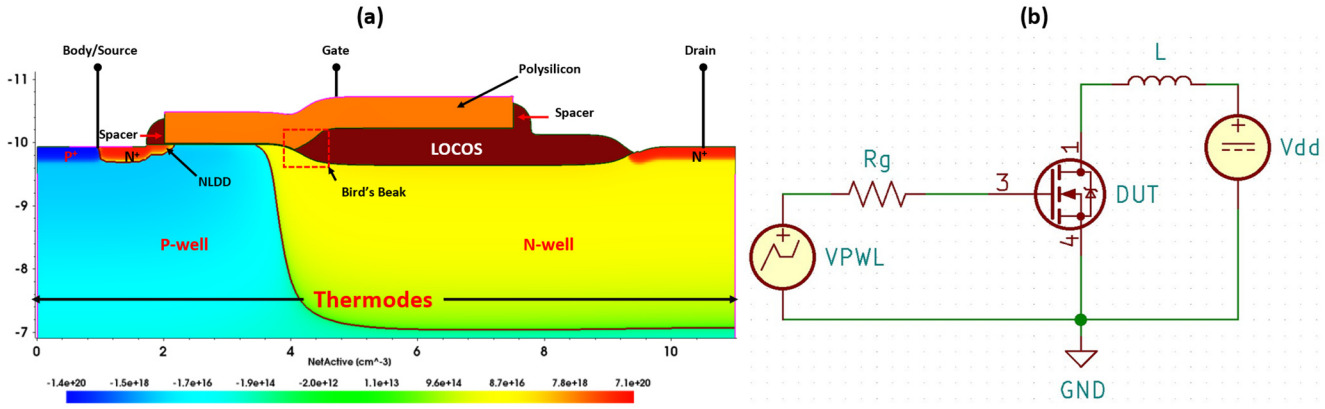

Figure 1. (**a**) DUT final doping distribution and (**b**) UIS test circuit.

In practice, integrated LDMOS devices are tested under clamped inductive switching (CIS), done by adding a Zener diode. This is to ensure that the thermal runway of nearby devices and/or nearby cells does not underestimate the safe operating area (SOA) by a premature thermal breakdown. Nonetheless, it is not the case in this TCAD simulation, and a UIS set-up, shown in Figure 1b, gives us an SOA that extends the device lifetime by reducing other degradation mechanisms [18]. Apart from the DUT, we used SPICE compact models for the other components, hence it is a mixed-mode simulation. The drain is attached to a variable inductive load; the gate is attached to a 10 Ω resistor, to approximate the single-cell metallic resistance, with voltage pulses of variables durations. The contact thermal resistance at the gate was set to 10^3 cm^2 KW^{-1} as an approximate boundary condition of the DUT width [25], although in practice, dealing with surface resistances is much more complicated [26].

3. Results & Discussion

After the quasi-stationary ramp that sets V_{DS} to 15 V, a transient simulation that applies the pulse, shown in Figure 2, is performed for up to 1 s to check the thermal runaway. The failure mechanism could either be: a localized excess in temperature at the bird's beak, which is due to high impact-ionization, due to hot-carriers caused by the high electric field, or an excess in current that triggers *NPN* parasitic transistor.

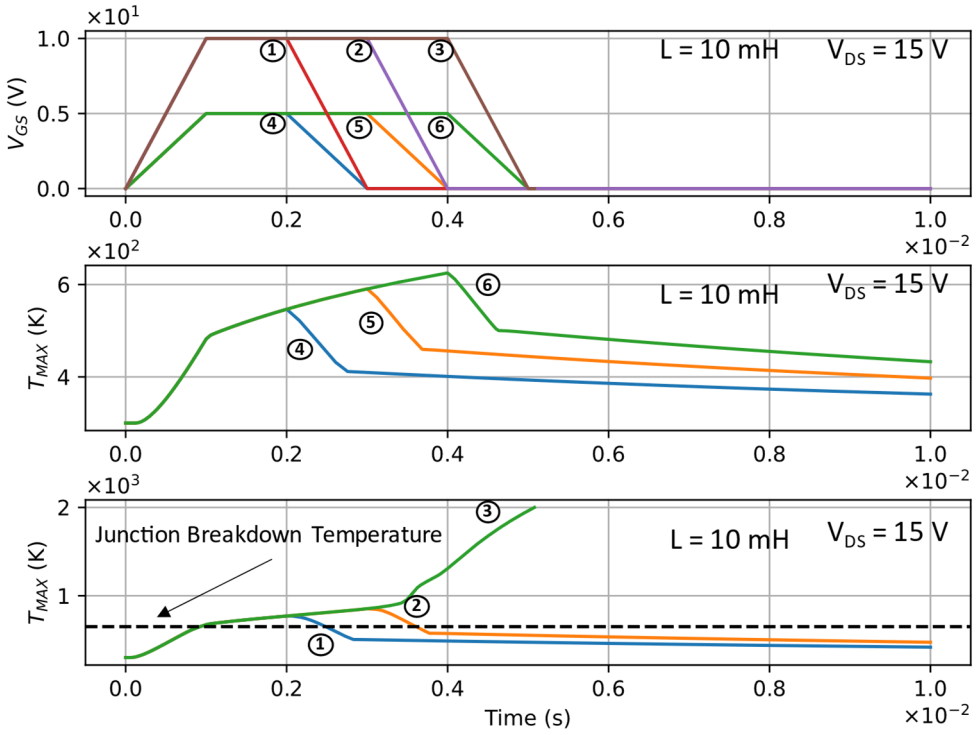

Figure 2. DUT temperature response to millisecond pulses of various durations and gate voltage amplitudes.

First, we noticed that the inductive load values, which were L = [10−2, 10−1, 1, 10] mH, under millisecond pulses, do not have a main impact on the characteristics, so we kept only a 10 mH value for the following results. Second, we tested the DUT under peak a V_{GS} pulse of 5 V and 10 V, the pulse duration is PW = [1, 2, 3] ms. There was no significant voltage overshoot that could reach the drain BV value under all variations or a critical excess in temperature. I_{DS} remains under nominal values when V_{GS} = 5 V. The electric field peak of 2.88 MV/cm is at the bird's beak, and the lattice temperature peak range is between 546 K and 623 K, which is considerably lower than the 650 K limit [27], especially when the temperature hot spot is in the bottom of the substrate and not in the active area. It is at V_{GS} = 10 V that the device fails under all pulses, and the current value is well over the nominal values.

To better define the SOA, we checked T_{MAX} under various V_{GS} values, from 5 V to 10 V with a 1 V step at V_{DS} = 15 V. We noticed that the device does not fail if V_{GS} < 7 V. Next, we checked T_{MAX} again, under various V_{DS} values, from 10 V to 20 V (sub-BV) while V_{GS} = 7 V. The results are summarized in Figure 3. The device is safe as long as V_{GS} < 7 V, irrespective of V_{DS}. Therefore, the device failure location is located near the gate. Precisely for this particular structure, at the bird's beak.

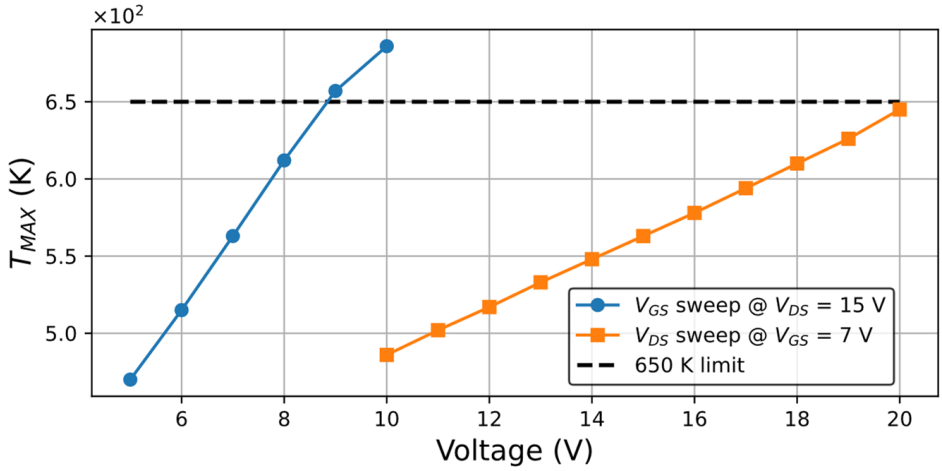

Figure 3. DUT thermal SOA and voltage dependency.

The physics of the failure mechanism is as follows. We noticed that the electron velocity, under all scenarios, is ~10^7 cm/s, which is a saturation velocity v_{sat}. We also noticed that the electron density n and the donor concentration (ionized impurity concentration) N_D have the same scalar distribution. Finally, the space charge is extended towards the drift region. The aforementioned conditions meet the expected Kirk effect (or base-push-effect) triggered by the parasitic *NPN* BJT. Under all biases, a strong inversion regime is reached, and the electrons that created the channel (Δn) also create a space charge region (SCR). The SCR by definition extends towards the least doped region, which, in this case, is the drift region. As Δn gets bigger, the SCR extends deeper into drift region until it reaches the drain. Since the Kirk effect is always present in the DUT, the high energetic carriers accelerated by the high electric field created by the drain potential always cause a significant impact ionization rate. If this electric field exceeds ~0.55 MVcm^{-1} in the silicon, the impact ionization rate peaks at 3.15×10^{28} cm^{-3} s^{-1}, and thus increases the probability of creating additional electron-hole pairs (EHP). The new EHPs are as energetic—or more energetic—as the loss in energy occurs due to the collisions with the lattice atoms, which is compensated by the thermal runaway. Since the SCR covers most of the drift region and the drain, a critical value of EHPs is reached that causes avalanche breakdown. Therefore, the failure mechanism is a thermal runaway followed by an avalanche breakdown [17].

In practice, however, such an HV transistor is likely to be near a significant source of heat. Therefore, we must consider the initial temperature (T_{init}). The results in Figure 4, show a sweep at V_{DS} = 15 V, V_{GS} = 7 V, where T_{init} is varied from 300 K to 420 K with a 20 K step. The behavior is linear; T_{MAX} increases by the same amount as T_{init}. With all parameters considered, the primary electrothermal SOA is $V_{DS} \leq 15$ V, $V_{GS} \leq 7$ V, and $T_{init} \leq 380$ K (105 °C). However, it is worth noting that the thermal runaway does not stop at the first cycle of the pulse. Figure 5, shows that the thermal breakdown is easily reached under repetitive UIS, hence the necessity of the protection circuit even under SOA.

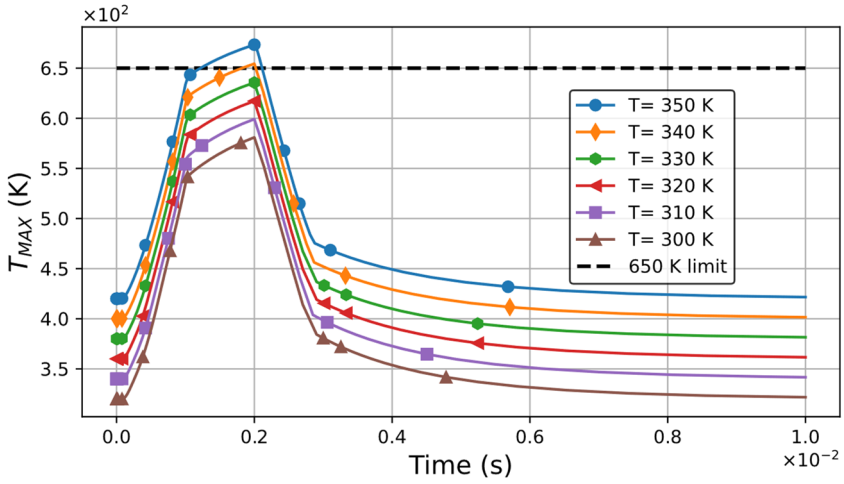

Figure 4. DUT thermal SOA against initial thermal conditions.

The qualitative failure mechanism described above does not hold under all scenarios. The shorter pulses change the breakdown mechanism from an electrothermal one to a purely electrical breakdown (avalanche only). The device under short pulses does not have the time to generate a significant current, thus heat, as plotted in Figure 6A. On the other hand, the drain voltage overshoot exceeds *BV*, as illustrated in Figure 6B. This causes a snap-back and current crowding as the relatively high doping profile of the drift region, which is meant for the CMOS logic n-well, reduces the parasitic collector ballast resistance. The latter will increase the gain of the parasitic BJT and thus, the early onset of a premature failure. The failure has also a component of a very high electric field at the edges. Finally, in practice, there will be a probability of premature oxide breakdown, and current filamentation between the device cells [15].

The presented DUT, obtained from a process meant for HP circuitry, got a low BV, but a wide SOA under millisecond pulse UIS stress. The range of drain and gate biases should be enough to achieve an unconditional stable gain in a power amplifier, which is a subject for future studies. Depending on the layout, the type of cooling (passive or active), and the final application, the SOA could be extended, especially under sub-millisecond pulse stress, as well as the lifetime of the device.

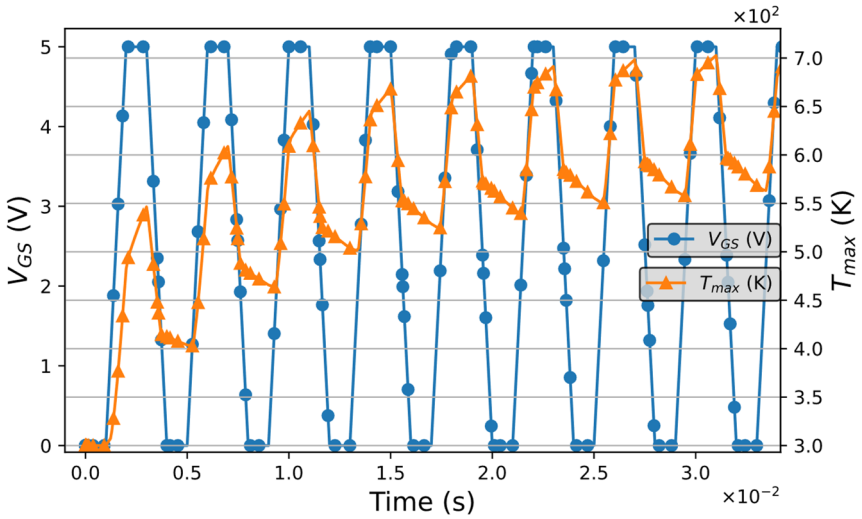

Figure 5. DUT thermal SOA against repetitive UIS.

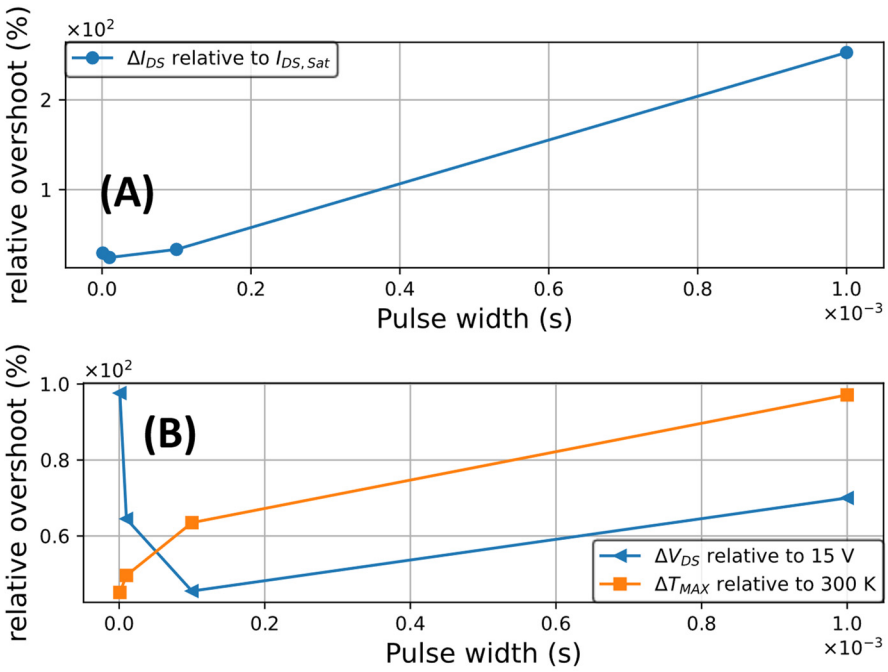

Figure 6. Failure mechanism physics towards short and mid-long UIS pulses. (**A**) Due to the short pulse, the device could not generate a lot of drain to source current, (**B**) shows the consequence in terms of temperature and drain to source potential.

4. Conclusions

A detailed setup of UIS stress to evaluate the SOA of a LOCOS-based LDMOS made with a 1 µm CMOS process is presented. The failure mechanism is a thermal runaway followed by an avalanche breakdown. Replying on such a process allows a wide SOA at the expense of a relatively low *BV* even when the Kirk effect is always present under nominal bias conditions. However, under sub-millisecond pulses durations, the breakdown becomes purely electrical, and the SOA narrows down. Which requires additional technological and design efforts to avoid failure.

Author Contributions: A.H. created the scripts of the TCAD simulations, extracted and visualized the results, and wrote the paper. B.D. provided the necessary process parameters, examined the numerical values of the results, and assisted in the paper's correction. All authors have read and agreed to the published version of the manuscript.

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