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Design of an LDMOS Transistor Based on the 1 µm CMOS Process for High/Low Power Applications †

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Abstract: In this paper we investigate the performance of an integrated n-type laterally-diffused metal oxide semiconductor (nLDMOS) transistor, using 2D TCAD simulations. This work is based on the 1 µm CMOS technology node at CDTAs clean room. The nLDMOS process uses the necessary steps extracted from logic-integrated circuits fabrication flow, which yields to local oxidation of silicon (LOCOS), single reduced surface field (RESURF)-based nLDMOS, without needing any additional masks or steps. The resulting device has a 22 V breakdown voltage (BV) and 272 mm^2 mΩ specific on-state resistance (R_{ON}). The analysis determined that the proposed device could be implemented in RF power amplifiers for wireless communications or automotive circuits as primary domains, provided experimental calibrations.

Keywords: LDMOS; TCAD; CMOS

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1. Introduction

In many power, RF, and microwave electronic circuits, the laterally-diffused metal oxide semiconductor (LDMOS) transistor is widely adopted, which is due to its low cost and excellent performance [1,2]. LDMOS transistor design is also a mature, well-optimized practice [3]. The influence of each process step, region, and operating regime is well understood, especially when it is fabricated in complementary MOS (CMOS) technology [4]. Additionally, the basic LDMOS structure allows easy integration with the logic, low power circuits, opening more application possibilities, even with old technology nodes [5]. A good LDMOS for power/analog applications should have a relatively high breakdown voltage (BV), low on-state resistance (R_{ON}), and a large safe operating area (SOA). It also needs to take into account the characteristics of various parasitic BJTs and their influence on self-heating, the capacitors' impact on the linearity and resistors' temperature dependence, and how it affects the frequency response [6,7].

Based on the available equipment at CDTAs clean room, which uses the 1 µm CMOS technology node [8,9], we propose an nLDMOS transistor by TCAD simulations. The latter is designed to be integrated with the rest of the logic circuits, as it follows the extracted CMOS flow adopted at the facility. The proposed device uses a single-RESURF and adopts the LOCOS separation method as field oxide. The DC and RF behavior is consistent with what is reported in the literature [10]. The characteristics described in the following paragraphs, more precisely the breakdown voltage of 22 V, show that the proposed device is a good candidate as a power device, RF power amplifiers (PA) for wireless applications, automotive circuits, or similar domains [11,12].

2. Results and Discussion

The proposed LDMOS structure was generated using the Sprocess tool in Sentaurus simulator [13]. The process flow was extracted from a standard CMOS flow adopted at CDTA [8,9]. CDTA's process uses 14 masks for both the FEOL and BEOL. However, for our study of the FEOL of the LDMOS, the process used seven masks and six implants. Figure 1 shows the general steps.

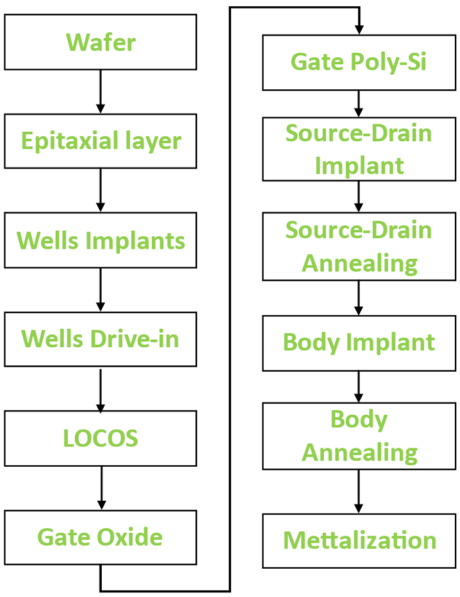

Figure 1. General process steps.

The substrate was boron-doped with a final resistivity of 10 Ω that corresponds to N_{sub} = 5 × 10^{14} cm^{-3}, <100> orientation, and 10 µm thickness. The transistor used an epitaxial layer, grown by diffusion at 1000 °C for 6 min, which gave a thickness of 12 µm; the same doping concentration as the substrate was chosen, thus the same resistivity. Next, the 2D mesh engine was triggered and we prepared the n-well, starting with a dry O_2 diffusion at 950 °C for 40 min, then photoresist deposition with a thickness of 1.2 µm. The implant used a phosphorus dose of 1.3 × 10^{13} cm^{-2}, at 150 KeV, tilting the substrate at 7°, using the Pearson distribution function.

After, we stripped the oxide. The same procedure was done to prepare the p-well implant, which used a boron dose of 3.7 × 10^{13} cm^{-2} at 160 KeV while adding a rotation of 22°. Before proceeding to other layers, we performed a well drive-in by diffusion in an N_2 environment at 1150 °C for 120 min.

The next step was to prepare the LOCOS separation, starting with stripping the previous oxide, diffusing dry O_2 at 950 °C for 20 min, then depositing a nitride isotropic layer of 150 nm thickness. We etched the nitride using the LOCOS mask anisotropically. Finally, a wet H_2O diffusion was performed at 960 °C for 240 min. The post-LOCOS steps included stripping the nitride and an isotropic oxide etch of 0.2 µm. For the threshold adjustment, we used a Boron implant with a dose of 2 × 10^{12} cm^{-2} at 25 KeV and a tilt of 7°.

The gate oxide used diffusion of dry O_2 at 900 °C for 40 min, followed by the poly-silicon layer, which used an isotropic deposition doped with phosphorus, with a concentration of 5 × 10^{19} cm^{-3} and a thickness of 0.5 µm. We etched 0.58 µm of poly-silicon using the gate mask anisotropically.

For the lightly doped drain step (LDD), the single implant found in the original process did not yield a good threshold voltage. V_{TH} was too high and it would be an issue for a full integration, thus it had to be changed. We used four consecutive implants of Boron with a dose of 1 × 10^{12} cm^{-2}, a tilt of 30°, and rotation by 90° for each implant. Then, we followed

immediately with an arsenic implant for the n-type extension, at a dosage of 1×10^{15} cm^{-2}, and 0° tilt and no rotation. The annealing peaks were at 960 °C under N_2 and O_2.

Next, the spacers were grown at rate of 150 nm/s at 750 °C, which was etched back as well as 20 nm of silicon. After, we prepared for the source and drain implant by diffusing dry O_2 at 925 °C for 20 min, then deposited a 1.2 µm photoresist layer. The implant used an arsenic dose of 5×10^{15} cm^{-2} at 60 KeV, also using the Pearson distribution function.

After, we prepared for the source and drain implant by diffusing dry O_2 at 925 °C for 20 min then deposited a 1.2 µm photoresist layer. The implant used an arsenic dose of 5×10^{15} cm^{-2} at 60 KeV, also using the Pearson distribution function.

During the process, we noticed the necessity of two additional annealing steps, one for the source and drain implant and another for the body implant. Without these annealing steps, the low energy implant was not enough for the species to make them penetrate the device at the desired depth. These particular steps used an adequate temperature elevation using N_2 environment, and a mixture of N_2 and O_2 gas flow, for a total duration of 1.67 min in the temperature range 700–1050 °C. We can make sure the annealing did not affect the previous layers destructively by simply observing the before and after structure.

Finally, for the body implant, after a 1.2 µm photoresist deposition, we used a BF_2 dose of 3×10^{15} cm^{-2} at 80 KeV with 7° tilt. Then we stripped the photoresist and performed annealing for 1.57 min. This particular step is the source and drain implant of the PMOS transistors.

Although it is feasible to simulate the deposition and etching of aluminum and titanium, it is not possible to solve the transport equations coupled with temperature for metals in our simulator version. Solving for temperature is critical to accurately evaluate the self-heating effect and the breakdown voltage. Therefore, the metal layers were omitted in the final structure.

Figure 2 shows the resulting device. The gate oxide and LOCOS thicknesses are 15 and 787.4 nm respectively.

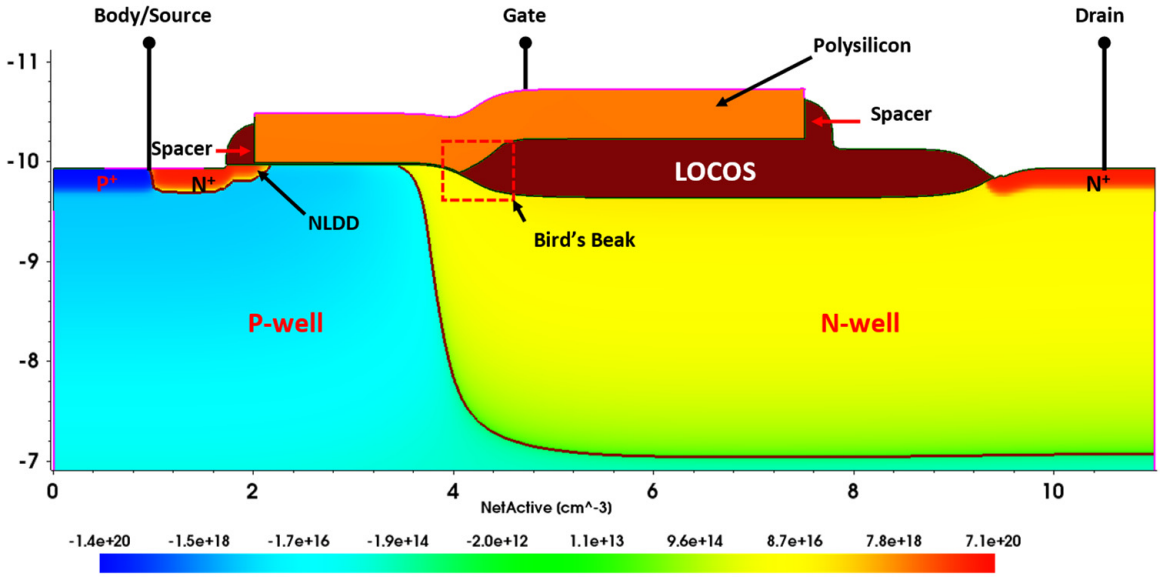

Figure 2. Final structure net doping profile.

The device simulation, conducted using the SDevice tool [14], will reflect the front-end of line (FEOL) behavior only. We used the area-factor function to simulate a device width of 100 µm without using an actual 3D mesh. We chose the hydrodynamic transport model with Fermi statistics and density quantization model for electrons, and mobility degradation using the "Inversion-Accumulation layer mobility model" coupled with the Hänsch model for high field saturation. Doping and temperature-dependent Shockley-Read-Hall (SRH),

Auger, and avalanche (UniBo) were used to model recombination and impact ionization. Finally, the "OldSlotboom" model was used for bandgap narrowing.

The transfer characteristic is plotted in Figure 3a, where the sweep is done for various V_{DS}, from 3 to 30 V with a 3 V step. The highest leakage current (I_{off}) is 1.3 × 10^{-11} A under V_{DS} = 30 V. The curves were then differentiated to show the transconductance (g_m), plotted in Figure 3b. g_m keeps increasing with increasing V_{GS} when V_{DS} is high, which is good for RF behavior, as the cut-off and maximum frequencies are directly proportional to g_m.

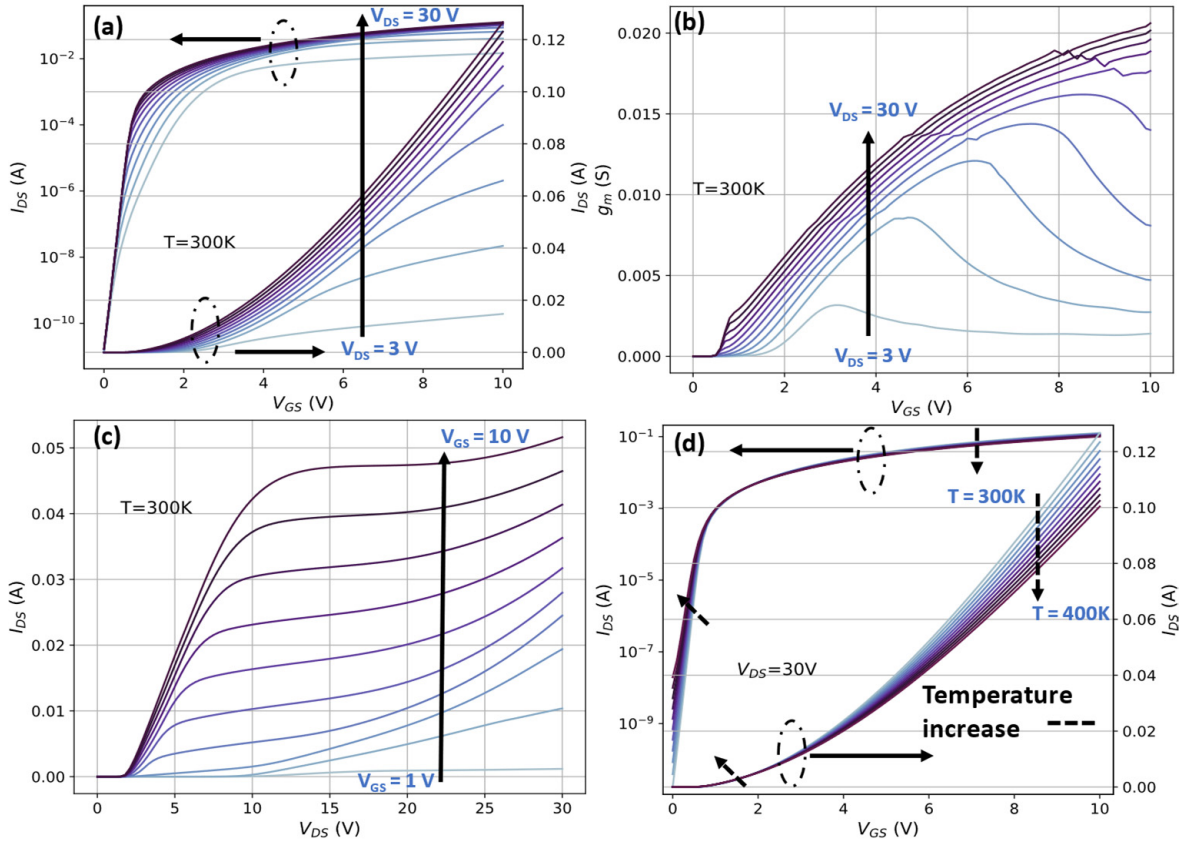

Figure 3. Various IV characteristics: (**a**,**d**) Transfer, (**b**) transconductance, (**c**) output.

Figure 3c shows the output characteristic plotted for various V_{GS} values. According to this electrothermal simulation, temperature rises, during this DC sweep, did not create the self-heating effect. Self-heating manifests as a dip in I_{DS} after saturation and causes a compression effect in the output characteristic due to the Kirk effect [15], which is practically absent in our device. Instead, this device suffers from a prolonged quasi-saturation regime at low V_{GS} as well as an early on-state breakdown.

We also plotted the transfer characteristic for various temperatures, as shown in Figure 3d, to extract the zero-temperature coefficient point (*ZTC*). The *ZTC* point is where the threshold voltage and mobility temperature dependencies are canceled. This point is useful for current referencing, a common practice in RF design [16]. The *ZTC* point occurs in our case at ~1.6 V. We also noticed a rise in I_{off}, where it reached 1.9 × 10^{-8} A at 400 K, which is a good value considering that we did not include any form of thermal dissipation of the backend of the process and the packaging.

As for the breakdown voltage (*BV*), it was extracted using the continuation method, while maintaining the gate voltage, V_{GS} at 0. *BV* occurs at V_{DS} = 22 V and approximately 10^{-11} A, the result is plotted in Figure 4. If we leave a 30% safe operating area, which is a standard value in LDMOS designs, the limit will be 15.4 V for an off-state drain bias.

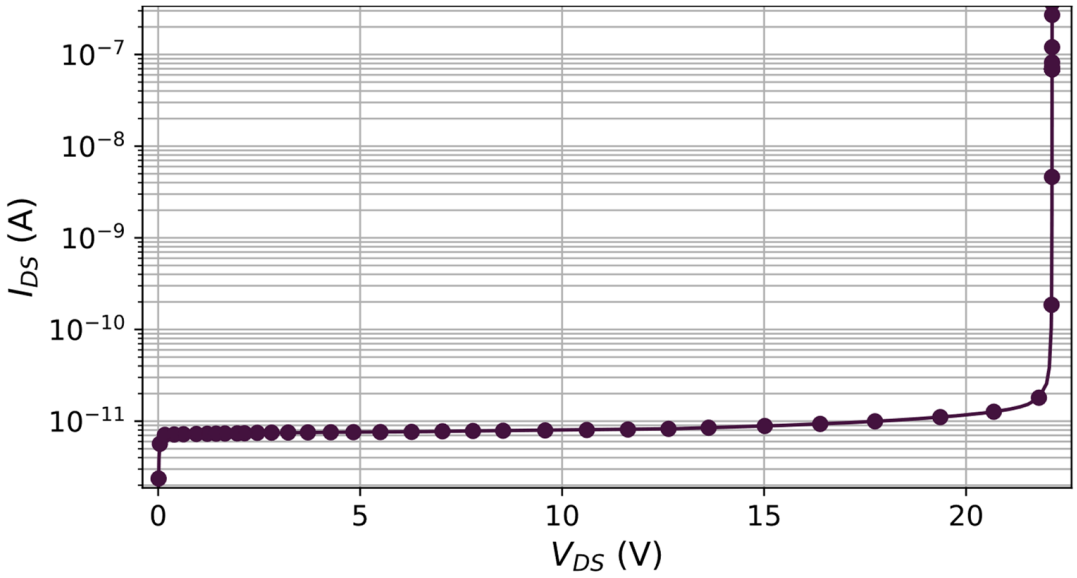

Figure 4. Off-state breakdown characteristic of the LDMOS.

Figure 5 shows the 2D scalar distribution of the absolute value of the electric field and with its extracted maximum path. The bird's beak and near areas have the highest values, and we reported that it triggers noticeable degradation under hot carrier injection [17,18].

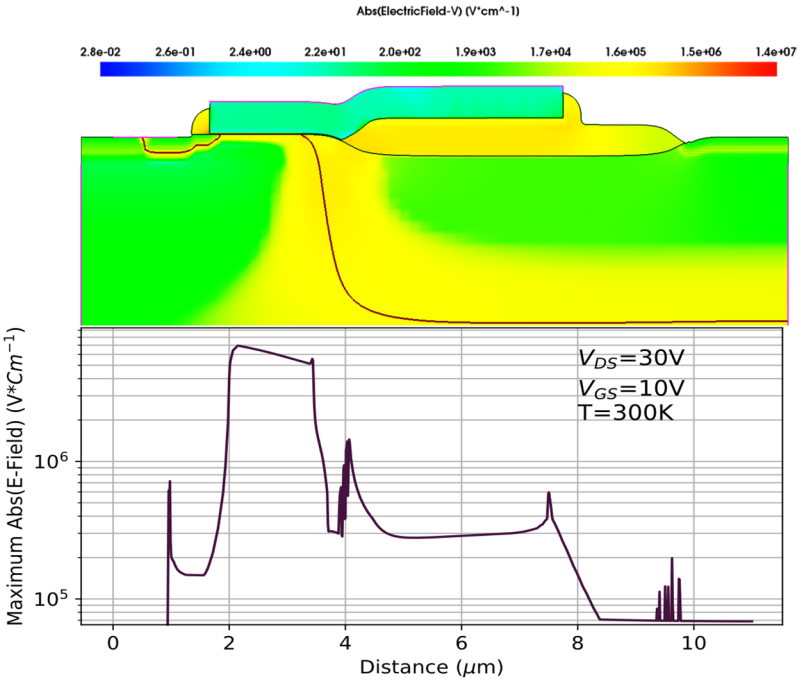

Figure 5. Electric-field scalar distribution and its maximum value along the LDMOS.

As mentioned earlier, the LDMOS operates in RF modes, thus it is important to determine its frequency response. The AC sweep simulation saves all possible combinations of capacitances and admittances between the electrodes. The saved data were used in the Svisual tool, which relies on a two-port network configuration to extract the RF parameters. The resistances 150 and 1 kΩ were used for stability at the source and substrate, respectively, as well as using a 100 kΩ resistance for the gate to drain feedback to reduce low-frequency gains. This setup was intended as a first approximation for the LDMOS response, not a final configuration, as further impedance matching will be in SPICE circuit level simulations.

First, we extracted the maximum oscillation frequency (f_{max}) and the cut-off frequency (f_T), using the admittance and hybrid parameters, respectively, with the unit-gain-point method. The results are plotted in Figure 6a,b. Next, we examined the transistor gain as a function of frequency for multiple gate voltages, using Mason's unilateral gain (MUG) approach. MUG simulation results are plotted in Figure 6c. Stable gains occur if $V_G \leq 6$ V and under 10^9 Hz frequencies, thus strong inversion regimes must be avoided; it also causes hot carrier injection degradations.

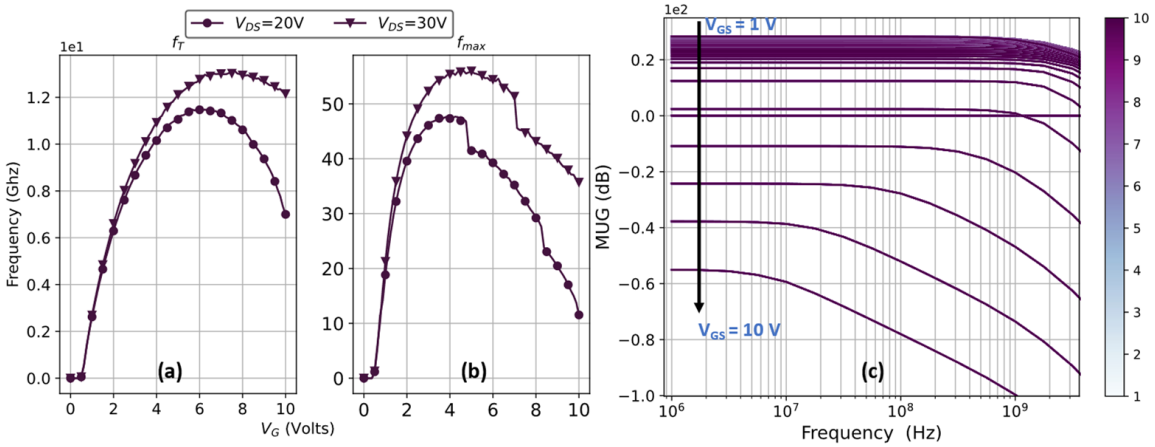

Figure 6. Maximum and cut-off frequency extracted from a two-port network simulation (**a**,**b**), respectively. (**c**) Mason's unilateral gain (MUG) as a function of gate voltage.

A recapitulation of the DC and RF parameters is presented in Table 1. This simulation showed that integrating RF and/or power modules is possible using the 1 µm CMOS process flow at CDTA, and the results show overall acceptable electrothermal behavior under DC and RF regimes, provided further studies. However, to take full advantage of the RESURF principle, which can enhance BV up to 120 V, a slight change in the process flow (like implant energies) and using a double-gate design are more fitting to our targeted applications.

Table 1. Main electric parameters from DC and RF characteristics.

Parameter	Value
Off-state current (I_{off}) @V_{DS} = 30 V	1.7×10^{-11} (A)
ON-state current (I_{ON}) @ V_{DS} = 30 V	0.126 (A)
Threshold voltage (V_{TH}) @ V_{DS} = 30 V	0.44 (V)
Peak transconductance	0.136 (S)
Zero-temperature coefficient (ZTC)	1.6 (V)
Subthreshold swing (SS)	105 mV/dec
On-state resistance (R_{ON})	272 (mm^2 mΩ)
Breakdown voltage (BV)	22 (V)
Figure of merit (FoM) ($FoM = BV^2/R_{ON}$)	1.77 (V/mm^2 mΩ)
Maximum oscillation frequency (f_{max})-PeakdB-	56.07 (GHz)
Cut-off frequency (f_T)-Peak0-	13.14 (GHz)

3. Conclusions

The DC and RF performances of an integrated LDMOS were investigated in this paper. The 2D process simulation was based on the 1 µm CMOS technology node, available at CDTA. The extracted process flow yielded a 22 V BV and 272 mm^2 mΩ R_{ON}. The temperature effect and the stability in various bias conditions and frequencies are presented. According to the extracted data, the proposed nLDMOS could be used for power amplifiers in wireless communications, automotive, and similar domains.

Author Contributions: A.H. created the scripts of the TCAD simulations, extracted and visualized the results, and wrote the paper. B.D. provided the necessary process parameters, examined the numerical values of the results, and assisted in the paper's correction. All authors have read and agreed to the published version of the manuscript.

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References

1. Ma, G.; Burger, W.; Dragon, C.; Gillenwater, T. High efficiency LDMOS power FET for low voltage wireless communications. In Proceedings of the International Electron Devices Meeting, Technical Digest, San Francisco, CA, USA, 8–11 December 1996; pp. 91–94.
2. Houadef, A.; Djezzar, B. Process and performance optimization of Triple-RESURF LDMOS with Trenched-Gate. *Int. J. RF Microw. Comput.-Aided Eng.* **2021**, *31*, e22755. [CrossRef]
3. Golio, M. *RF and Microwave Semiconductor Device Handbook*; CRC Press: Boca Raton, FL, USA, 2017.
4. Kwon, O.K.; Ng, W.T. Others An optimized RESURF LDMOS power device module compatible with advanced logic processes. In Proceedings of the 1992 International Technical Digest on Electron Devices Meeting, San Francisco, CA, USA, 13–16 December 1992; pp. 237–240.
5. Tan, Y.; Kumar, M.; Sin, J.K.; Cai, J.; Lau, J. A LDMOS technology compatible with CMOS and passive components for integrated RF power amplifiers. *IEEE Electron Device Lett.* **2000**, *21*, 82–84. [CrossRef]
6. Fu, Y.; Li, Z.; Ng, W.T.; Sin, J.K. *Integrated Power Devices and TCAD Simulation*; CRC Press: Boca Raton, FL, USA, 2014.
7. Houadef, A.; Djezzar, B. Hot Carrier Degradation in Triple-RESURF LDMOS with Trenched-Gate. In Proceedings of the 2021 IEEE 32nd International Conference on Microelectronics (MIEL), Nis, Serbia, 12–14 September 2021; pp. 141–144.
8. Djezzar, B.; Bellaroussi, M.T. Process and Device Simulation of 1.2 µm- Channel N- well C-MOS Technology. In Proceedings of the 5th International Conference on Microelectronics (ICM'93), Dhahran, Saudi Arabia, 14–16 December 1993; pp. 28–32.
9. Boubaaya, M.; Larbi, F.H.H.; Oussalah, S. Simulation of Ion Implantation for CMOS 1 µm Using SILVACO Tools. In Proceedings of the 2012 24th International Conference on Microelectronics (ICM), Algiers, Algeria, 16–20 December 2012.
10. Whiston, S.; Bain, D.; Deignan, A.; Pollard, J.; Chleirigh, C.N.; O'Neill, C.M.M. Complementary LDMOS transistors for a CMOS/BiCMOS process. In Proceedings of the 12th International Symposium on Power Semiconductor Devices and ICs. Proceedings (Cat. No. 00CH37094), Toulouse, France, 22–25 May 2000; pp. 51–54.
11. Ma, G.; Burger, W.; Shields, M. High efficiency 0.4/spl mu/m gate LDMOS power FET for low voltage wireless communications. In Proceedings of the 1999 IEEE MTT-S International Microwave Symposium Digest (Cat. No. 99CH36282), Anaheim, CA, USA, 13–19 June 1999; Volume 3, pp. 1195–1198.
12. Gray, P.R.; Meyer, R.G. Future directions in silicon ICs for RF personal communications. In Proceedings of the Proceedings of the IEEE 1995 Custom Integrated Circuits Conference, Santa Clara, CA, USA, 1–4 May 1995; pp. 83–90.
13. *SentaurusTM Process User Guide 2017*; Synopsys: Mountain View, CA, USA, 2017.
14. *SentaurusTM Device User Guide 2017*; Synopsys: Mountain View, CA, USA, 2017.
15. Hower, P.; Lin, J.; Pendharkar, S.; Hu, B.; Arch, J.; Smith, J.; Efland, T. A rugged LDMOS for LBC5 technology. In Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs, Santa Barbara, CA, USA, 23–26 May 2005; pp. 327–330.
16. Najafizadeh, L.; Filanovsky, I.M. A simple voltage reference using transistor with *ZTC* point and PTAT current source. In Proceedings of the 2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No. 04CH37512), Vancouver, BC, Canada, 23–26 May 2004; Volume 1, pp. 1–909.
17. Houadef, A.; Djezzar, B. HCI Degradation of LOCOS-based LDMOS Transistor fabricated by 1 µm CMOS Process. In Proceedings of the 2020 International Conference on Electrical Engineering (ICEE), Istanbul, Turkey, 25–27 September 2020; pp. 1–6.
18. Houadef, A.; Djezzar, B. Evaluation of Hot Carrier Impact on Lateral-DMOS with LOCOS feature. *Alger. J. Signals Syst.* **2021**, *6*, 16–23.