engineering proceedings

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Proceeding Paper

Process and Device Simulation of SAW Temperature Sensors Compatible with 1 µm CMOS Technology †

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† Presented at the 1st International Conference on Computational Engineering and Intelligent Systems, Online, 10–12 December 2021.

Abstract: Process and device simulation of a surface acoustics wave (SAW) temperature sensor based AlN material as piezoelectric film, grown on Si wafer and patterned with Al electrodes, is described. CMOS 1 µm process is the process used to simulate a SAW sensor with number of IDT electrodes pairs N_p = 16 using Silvaco software; fabrication steps inside the cleanroom are also described. The Athena Silvaco module is used for technological process simulation and the Atlas module is used to characterize the sensor in terms of electrical potential and electric field distribution under IDTs. IDS = f (VDS) simulation curves are compared to those issued from experimental characterizations performed on PMOS and NMOS transistors realized by 1 µm CMOS technology. The mask needed for SAW realization is designed. In order to choose the best sensor to manufacture, two SAW sensors with N_p = 16 are characterized using Comsol multiphysics. Their IDTs length "*a*" and spacing "*b*" are 2 µm for the first sensor and 3 µm for the second one, which corresponds to 600 MHz and 400 MHz resonance frequencies respectively. The mechanical displacement field at the center frequency of the 3 µm structure and the reflection coefficients (S_{11}) of both structures are determined to deduce the piezoelectric response. Afterwards, the SAW temperature sensors are studied in the temperature range extending from −25 °C to 200 °C; their sensitivities are evaluated at 19.10 ppm/°C and 23.53 ppm/°C for 600 MHz and 400 MHz devices respectively.

Keywords: SAW temperature sensor; CMOS 1 µm process; Silvaco; Comsol; S_{11} reflection coefficient; sensitivity

Citation: Belkhelfa, N.; Serhane, R. Process and Device Simulation of SAW Temperature Sensors Compatible with 1 µm CMOS Technology. *Eng. Proc.* **2022**, *14*, 9. https://doi.org/10.3390/engproc2022014009

Academic Editors: Abdelmadjid Recioui, Hamid Bentarzi and Fatma Zohra Dekhandji

Published: 28 January 2022

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1. Introduction

For a long time, many types of sensors have been elaborated; these sensors have been developed by the means of various methods and techniques [1–4]. Compared to the other sensors, surface acoustic wave detectors (SAWs) have a lot of characteristics that make them more favorable. Among their numerous features we can mention reusability, higher sensitivity, reliability, multifunctionality and noninvasiveness.

SAW device principle is based on the conversion of an interrogative electromagnetic wave into an acoustic one by means of interdigital transducers (IDTs) fabricated over a piezoelectric crystal (Figure 1). During acoustic wave propagation over the piezo substrate, its velocity changes while the surrounding environment conditions change, the modified acoustic wave is transduced back into an electromagnetic signal that is transmitted for processing (determination of frequency shift or time delay according to the sensor type). The propagation properties (like wavelength and resonance frequency) of acoustic waves in piezoelectric media depend on the substrate material, the crystal cut and the structure of electrodes [5,6].

A typical SAW device in sensor applications consists in a transmitting IDT and a receiving one separated by few wavelengths, which constitutes the delay line configuration. IDTs with reflectors (called Bragg reflectors) form the resonator model and are mainly used in telecommunication circuits; they also can be used as sensors [7].

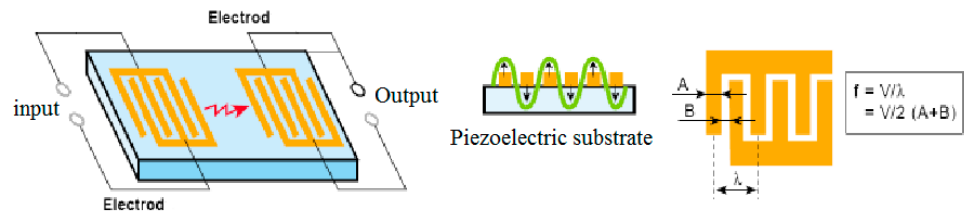


Figure 1. SAW devices working principle and geometrical parameters.

In this work, a SAW temperature sensor was designed using Silvaco TCAD Tools, Silvaco TCAD refers to technology computer-aided design. TCAD modules required for SAW simulation are Athena and Atlas [8]. The sensor was simulated using a specific fabrication process that is the CMOS 1 µm technology; this process was adopted because it is the process acquired by our fab. The necessary process steps needed for sensor realization were identified and simulated using Athena module, details about the realization steps inside the cleanroom were described. Characterizations using Atlas module were achieved to determine distribution of dopants, electrical potential and electric field under IDTs. The mask needed for IDTs realization, with different SAWs configurations and dimensions, was designed.

After that, a complementary study, following on from a previous one and performed in the Comsol multiphysics environment, was achieved on two sensors (2 µm and 3 µm IDTs width). The mechanical displacement field at the center frequency of the 3 µm IDTs structure was highlighted and (S_{11}) the variation of the reflection coefficient with temperature ranging from −25 °C to 200 °C was investigated for both structures; their sensitivities were evaluated and the adequate design for sensor realization was adopted.

2. Relevant Geometrical Parameters of SAW Sensors

Parameters such as IDTs width a, spacing between them b, their pairs number (N_p) and the acoustic aperture W are very important. The reason is that the SAW central frequency f_0 depends on them, and this central frequency has a direct effect on the sensor sensitivity, which is the first feature to focus on while designing a SAW device [5]. The sensitivity is related to the center frequency according to Equation (1) in the case of a resonator type sensor and according to Equation (2) in the case of a delay line type sensor:

$$S = \frac{1}{f_0}\frac{\partial f_0}{\partial T} = TCF \tag{1}$$

where δT is temperature variation and δf_0 is the resonance frequency shift, and:

$$s = \delta f/\delta T = 2\pi a f_0 \tau \tag{2}$$

where δf is the phase shift and τ is the delay.

3. Description of 1 µm CMOS Process

This technology realizes simultaneously on the same substrate MOS transistors with N channel and MOS transistors with P channel, for which the length of the gate is 1 µm. In our simulations, the SAW sensor is designed next to the N and P CMOS 1 µm transistors resulting from the simulation of the whole 1 µm process flow; it is simulated at the same time using the same flow. The aim is to check the possibility of fabricating the SAW sensor in the same chip with its electronic read out, which forms the integrated circuit later. We have chosen this approach because, in recent years, acoustic-sensor-based devices have become more and more important for sensing; which means SAW sensors can be applied as well as wired sensor elements in active circuits and as remote passive devices [4].

The 1 µm CMOS process's main characteristics are:

- P type substrate, orientation (100), resistivity 10 Ohm·cm;
- N-well/P-well;
- Double poly doped n^+;
- Double metal;
- Barrier metal Ti/TiN;
- 14 photolithography steps;
- 12 masques.

4. The 1 µm CMOS Process Steps for SAW Sensor Realization

The fabrication of circuits on silicon wafers is done with various layers, each with its own pattern, deposited on the surface by a specific order and over precise areas that are defined by the technological process. The several patterns used while depositing layers on the substrate (or during other realization steps such as doping or etching) are shaped by a process called lithography [9]. Some technological steps necessary to realize a surface acoustic wave sensor are described in Figures 2–5 resulting from Silvaco simulations (obviously during realization, all these processes take place inside the clean room). We have chosen 1 µm as the IDT length because the aim of this study is to list and understand the SAW realization steps and to have a representative idea of the behavior of the sensor after each one. The final IDT length will be adopted after Comsol characterizations achieved in Section 6.

Figure 2. AlN piezoelectric layer deposition.

The process flow steps needed for SAW sensor realization are:

Substrate initialization (definition), it is a silicon substrate-doped boron for which resistivity is 10 Ohm·cm (concentration 10^{15} e^-/cm^3) and orientation is (100). In the fab, the wafer is first cleaned using acetone and ethanol baths, agitated by ultrasound to eliminate most of the surface pollutions (grease, dust, etc. . . .) [10]. The ethanol being extremely volatile, its use facilitates the drying of the substrate under dry nitrogen flow, which is done after a rinse with deionized water. It should be noted that the silicon substrates (100) undergo, before this standard cleaning, a hydrofluoric acid bath (HF at 5%) in order to eliminate the native SiO_2 layer present on their surface.

AlN piezoelectric layer deposition (Figure 2), its thickness is 1.5 µm; AlN thickness was deduced from a previous study which objective was the optimization of SAW technological parameters [11]. AlN was chosen as the piezoelectric layer because of its several properties and its compatibility with CMOS process [10]. In fact, in the cleanroom, AlN is deposited using a PVD process (physical vapor deposition) with a specific recipe [12] inside a PVD cluster tool called the MRC Star Eclipse. Sputtering is the technique used for AlN deposition. It is a relatively simple and industrialized technique, allowing the deposition of thin films on various substrates at relatively low temperatures (<400 °C) and therefore CMOS compatible. Thus, for the realization of the sensor's piezoelectric layer an aluminum target is placed in an atmosphere constituted of an inert gas (Argon Ar) and a reactive gas (Nitrogen N_2). The nitrogen molecules are split and the nitrogen atoms (N) react with the aluminum target to form AlN. Argon is then sprayed onto the AlN created on the surface of the target to form the thin film on the substrate that is attached to the anode [12].

First metal layer deposition (Figure 3), the first metal layer is titanium that is 0.115 nm thick (100 nm TiN + 15 nm Ti). Ti, TiN layer is a barrier used to prevent metal diffusion into Si and to improve its adhesion This Ti layer has the characteristic of being very adhesive to Si and SiO2. In the cleanroom, it is a PVD deposition using MRC Star Eclipse tool.

Second metal layer deposition, it is Al that is 500 nm-thick (Figure 3). Aluminum is the metal used in the 1 µm CMOS process (deposited by PVD technique in the cleanroom on the whole substrate surface).

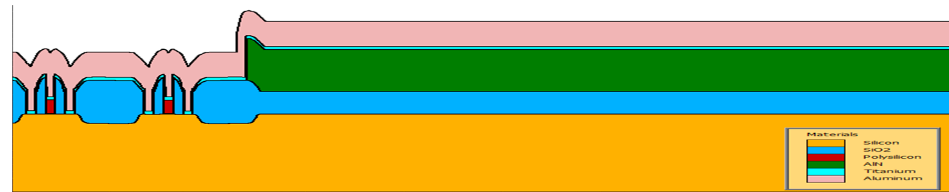
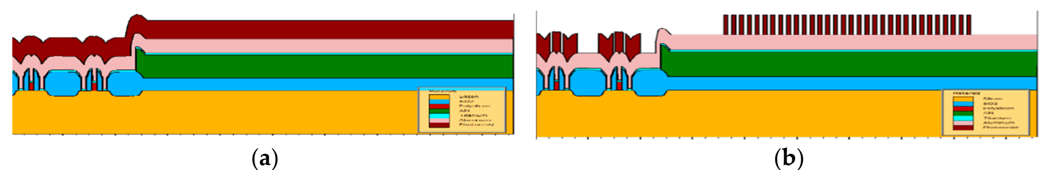


Figure 3. Metal layers deposition.

The following step is *metal etch for SAW sensor IDTs formation*. Such a process is done in two steps: first, the lithography step where we deposit a protection layer called photoresist and, second, etching step where only the open areas of the metal are etched. During simulations, the photolithographic step consists in photoresist deposition; its thickness in our process is 1.2 µm (Figure 4a), and the photoresist etch opens the areas of the metal to be etched (Figure 4b).



(**a**) (**b**)

Figure 4. Photoresist deposition and etch.

Inside the cleanroom, these two steps are completed as follows: a layer of photoresist (PR) material is first spin-coated on the surface of the wafer using SVG 8800 tool. The resist layer is then selectively exposed to radiation such as ultraviolet light, with the exposed areas defined by the exposure tool mask which is UV i-line Stepper GCA, i.e., we use ultraviolet light to form patterns on the photoresist through printing. After exposure, the PR layer is subjected to development, which destroys unwanted areas of the PR layer, and allows exposing the corresponding underlying layer (the unwanted areas in the PR are dissolved by the developer SVG 8800 tool).

After that, *aluminum and titanium are dry etched* to get read of them between the covered IDTs (Figure 5). In the cleanroom, metal dry etch is achieved in the LAM 9600 tool, which is a reactive ion etching reactor (RIE) that allows, added to metal etch, in situ resist etching and metal rinsing and drying to avoid the metal corrosion phenomenon. This tool uses chlorine (Cl_2) and argon (Ar) plasma to achieve the metal etch, oxygen (O_2) to etch the photoresist inside the tool and azote (N_2) to dry the wafer. The accuracy of the metal etch is very important, because IDTs pitch etch accuracy influences the response signal and helps reducing the noise [13,14].

Figure 5. Titanium and aluminum etch.

The remaining *photoresist is etched later* (Figure 6). In the fab, photoresist for metal patterning is etched inside the LAM 9600 metal etcher but the photoresist used for other technological steps is etched in the Tepla 300 tool, which is a microwave, high-frequency

reactor that uses oxygen plasma. The photoresist can also be etched through the wet etch process. In this case, liquid solutions (like HF) are used to remove the photoresist and other chemicals to clean the wafer, the chemicals used depend on the required etch selectivity. Many tools are employed, such as the Spray Cleaner Semitool. The wet etch process is also used in some technological steps where the anisotropy (etch directionality) is not a critical criterion.

Inside the cleanroom and for *metal passivation*, an oxide layer, namely silicon nitride (SiON) is deposited. Its thickness is 1.5 µm and it is later etched to open the bond pad.

The simulated sensor is a one-port resonator with number of IDT pairs N_p = 16; it is represented in Figure 6 next to the N and P transistors resulting from the 1 µm CMOS process flow simulation. The sensor was simulated using the 1 µm process steps that overlap with those necessary for its realization, i.e., within the 1 µm process flow; which gives a sensor on the same substrate (in the same die) with the N and P transistors.

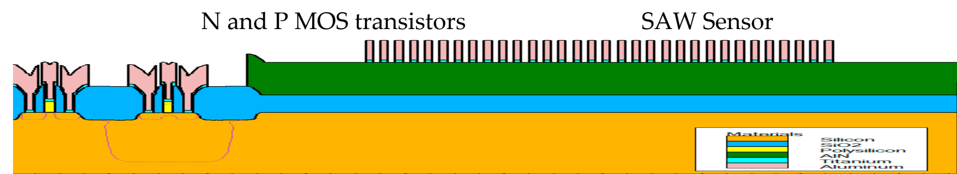
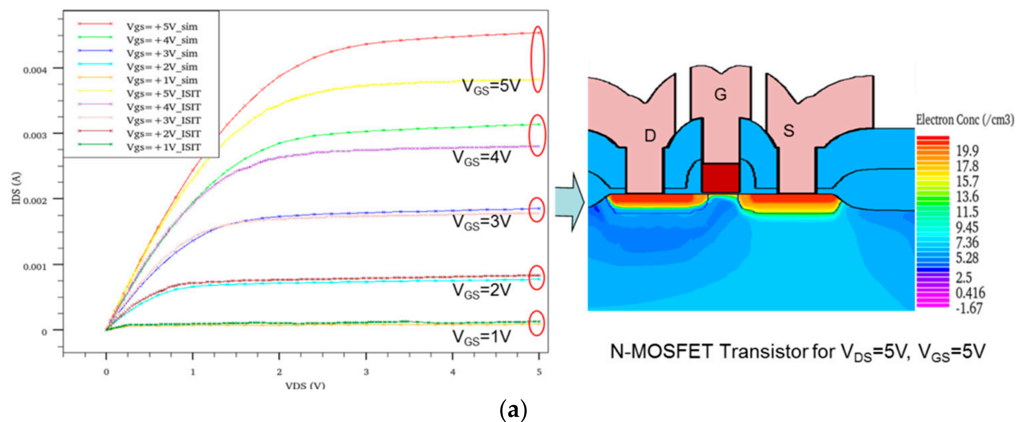


Figure 6. Athena results of CMOS process simulation (N and P transistors besides the SAW temperature sensor).

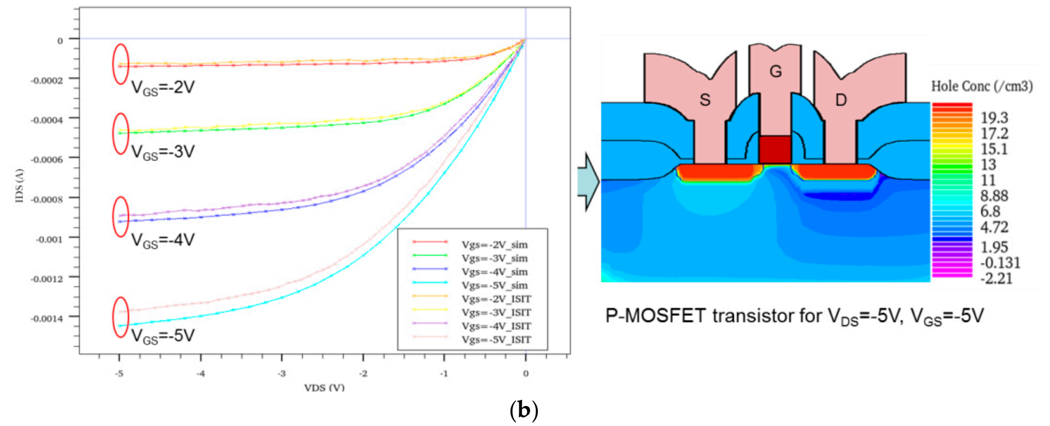
5. CMOS Process and Devices Validation

To validate our process simulation results, characterizations of the resulting PMOS and NMOS transistors were achieved in the Atlas tool to evaluate their IDS = f (VDS) curves. The latter were compared to curves issued from experimental characterizations performed on devices realized by 1 µm CMOS technology in ISIT fab (Experimental ISIT structures). The results are represented in Figure 7a,b, and they show a good agreement between experimental curves and those issued from simulations, for both N and PMOS structures.



(**a**)

Figure 7. *Cont.*

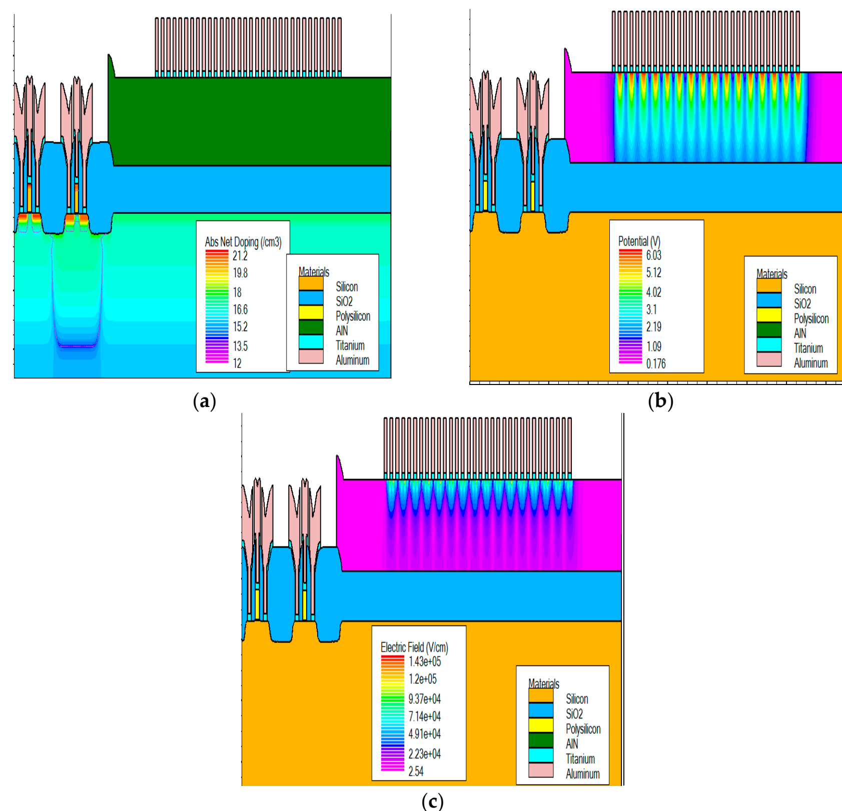


(**b**)

Figure 7. IDS = f (VDS) characteristics comparison between experimental and TCAD simulated data of NMOS (**a**) and PMOS (**b**) transistors, realized by 1 µm CMOS technology (ISIT).

Electrical characterizations in terms of dopant concentrations, electric potential and electric field distribution under IDT electrodes (Figure 8a–c) are achieved on the obtained SAW sensor using Atlas module. From Figure 8a, we deduce that the highest concentration is under the source and drain electrodes added to the poly-gate of the N and P transistors. It is around 10^{21} e^-/cm^3. In Figure 8b, we can see the electrical potential distribution under IDT electrodes after the application of 5V voltage. This electrical potential induces an electric field (Figure 8c) that launches, by reverse piezoelectric effect (Equation (3) [15]), a surface acoustic wave propagating over the AlN piezoelectric layer.

$$D_j = e_{jkl}S_{kl} + \varepsilon^S_{jk}E_k \text{ and } T_{ij} = c^E_{ijkl}S_{kl} - e_{kij}E_k \quad (3)$$



(**a**) (**b**) (**c**)

Figure 8. (**a**) Distribution of dopants concentration in the realized structure, (**b**) electrical potential distribution under IDT electrodes and (**c**) electric field distribution under IDTs.

6. The Designed Sensor Mask

A mask or "photomask" is a square glass sheet on which is patterned a mixture of metal film (on one side only). The mask is aligned with the wafer, so that the pattern can be reproduced faithfully onto its surface. An open-access design software was employed to design the mask used in the fabrication process. IDT masks designed have different electrodes lengths "*a*" and spacing "*b*" values (1 µm 2 µm, 3 µm, 4 µm, etc.) and different SAW configurations (one-port resonators, two-port resonators, delay lines). Figure 9 shows the layout of the designed mask.

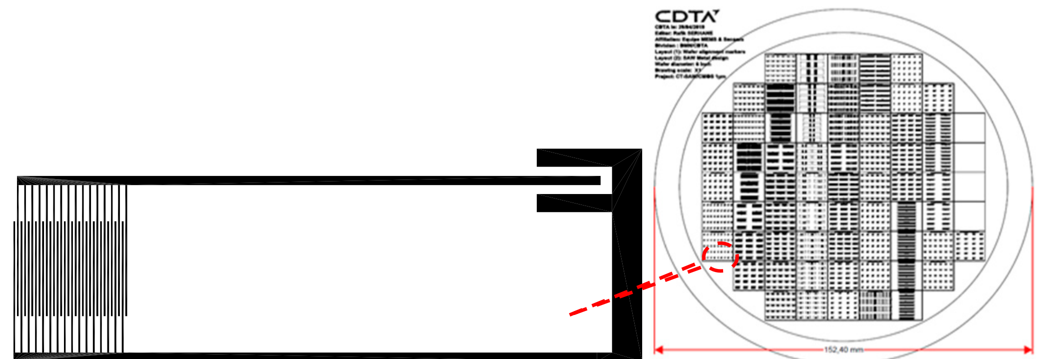


Figure 9. The designed SAW IDTs mask.

7. Multiphysics Simulation of the Designed SAW Sensor

A 2D finite element method (FEM) simulation using Comsol software was used to evaluate the physical and electrical behaviors of two SAW sensors. The sensors are one-port resonator type, they differ in the length of IDTs "*a*" and each of them has N_p = 16. The ongoing study follows on from a previous one [11] which the objective was the optimization of SAW geometrical parameters. The perspectives of the cited work were the investigation of 2 µm and 3 µm structures (corresponding to 8 µm and 12 µm wavelengths respectively) and the results presented in the current study concern their sensitivities, since the other characteristics (like velocity and reflectivity) have already been studied and were interesting [11].

When simulating SAW devices in Comsol, boundary conditions are imposed to the structure: the acoustic displacements and stresses are assumed continuous at the AlN-silicon interface and both top and bottom sides of the structure are assumed to be stress free surfaces. In order to avoid the slowness of the calculations, silicon depth is fixed at 3λ and a perfectly matched layer (*PML*) approximation is used to simulate the endless edges of the structure. Its thickness is 1.5λ [11].

The mechanical displacement field, of the 3 µm IDT length structure, is represented in Figure 10a; one can notice that this mechanical field is located in the interface between the Al and AlN layer, which is a characteristic of the Rayleigh mode surface acoustic wave.

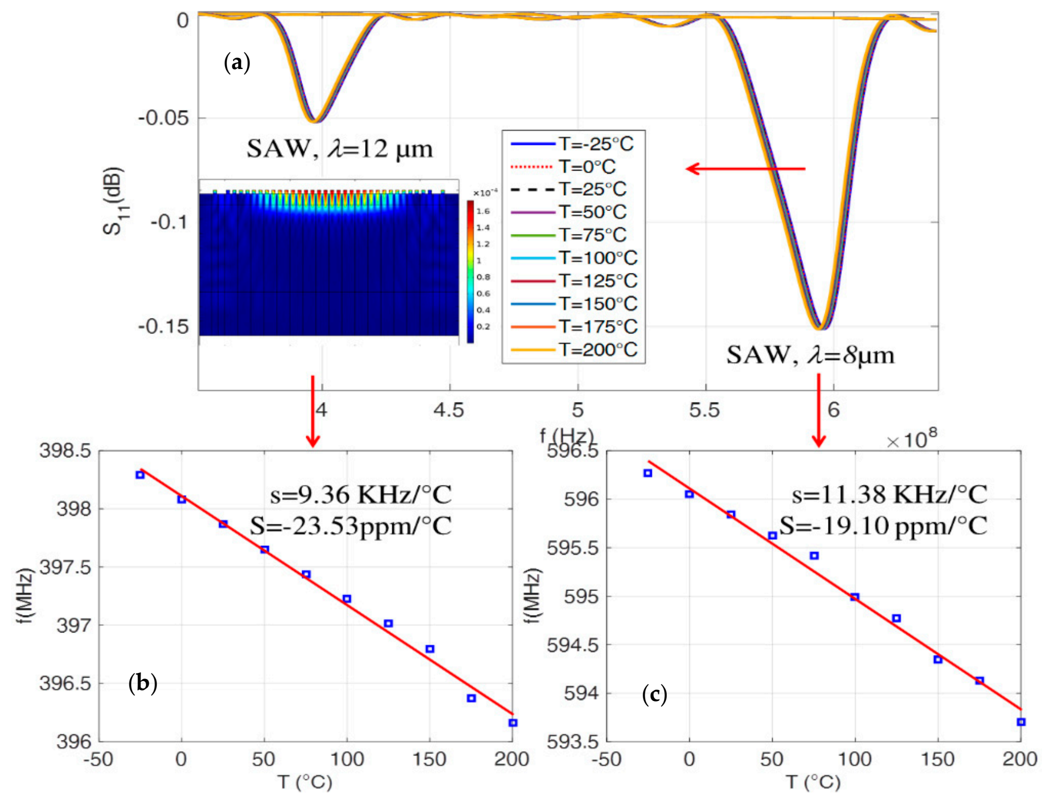


Figure 10. (**a**) Reflection coefficient (S_{11}) and (**b**) frequency shift variation, versus temperature for structures with (**b**) 12 µm and (**c**) 8 µm wavelengths.

Simulation of the SAW Sensors Sensitivity to Temperature

The variation of the reflection coefficient (S_{11}) parameter is computed for different values of the temperature ranging from −25 °C to 200 °C with a step of 25 °C; it is plotted in Figure 10a for structures with 8 µm and 12 µm wavelengths respectively.

We can notice that the resonance frequency of the sensor (f_0) shifts toward low values and that (S_{11}) magnitude increases slightly for both structures, when temperature rises. For the study of (S_{11}) variation with temperature, we used a theoretical temperature model coupled to FEM model, this model was developed in a previous work [16].

The calculated sensitivities, resulting from the determination of the slope of the lines obtained in Figure 10b,c and using Equation (1), are 19.10 ppm/°C and 23.53 ppm/°C for 600 MHz and 400 MHz devices respectively (corresponding to 8 and 12 µm wavelength, respectively). This sensitivity was evaluated at S = 8.53 ppm/°C for a structure of 1 µm IDTs length (f_0 = 1.16 GHz), which means that the structure with 3 µm-long IDTs gives the best sensitivity and acceptable other characteristics, as deduced from [11].

8. Conclusions

In the past, researchers depended on experiments to design and develop SAW devices but, nowadays, the design of SAW devices is enhanced by the use of modeling techniques such as TCAD and FEM, which helps the study of all their characteristics. In this paper, SAW temperature sensors were designed and simulated using Silvaco TCAD tools and Comsol Multiphysics software. The simulated SAW temperature sensors consist in a silicon substrate on which an AlN piezoelectric layer has been deposited; AlN was chosen for its compatibility with the 1 µm CMOS process available in our cleanroom. The electrodes are made of aluminum. The process steps for SAW realization are described by indicating their course inside the cleanroom; electrical properties like potential and electric field distribution were extracted using Atlas Silvaco module.

We performed FEM analysis of acoustic waves propagating on two SAW devices (8 µm and 12 µm wavelengths working at 600 and 400 MHz frequency respectively). Mechanical characterizations in terms of mechanical displacement field and electrical characterizations in terms of electrical power reflection coefficient (S_{11}) were performed while temperature was varied. S_{11} variation with temperature showed a shift toward low frequencies when temperature increased whereas its magnitude rose. The sensor-calculated sensitivities were S = 19.10 ppm/°C and S = 23.53 ppm/°C for 600 MHz and 400 MHz devices respectively. Knowing that this sensitivity was evaluated at S = 8.53 ppm/°C for the structure of 1 µm IDTs (f_0 = 1.16 GHz, previous work), we deduce that the structure with 3 µm IDTs length gives the best sensitivity added to acceptable other characteristics, which makes it a good candidate for the manufacture of our SAW temperature sensor.

Author Contributions: Conceptualization, N.B. and R.S.; methodology, N.B. and R.S.; software, N.B. and R.S.; validation, N.B. and R.S.; formal analysis, N.B. and R.S.; investigation, N.B.; resources, N.B. and R.S.; data curation, N.B. and R.S.; writing—original draft preparation, N.B.; writing—review and editing, N.B.; visualization, N.B.; supervision, N.B.; project administration, R.S.; funding acquisition, R.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by Ministère de l'enseignement supèrieur et de la recherche scientifque and funded by Direction Générale de la Recherche Scientifique et du Développement Technologique (DGRSDT), Algeria, grant number: 05/CDTA/DGRSDT/2017, CT-SAW/CMOS 1 µm project. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Experimental data provided by Fraunhofer ISIT Institute in Itzehoe, Germany and available at CDTA.

Conflicts of Interest: The authors declare no conflict of interest.

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