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An Advanced Synchronized Time Digital Grid Twin Testbed for Relay Misoperation Analysis of Electrical Fault Type Detection Algorithms

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Abstract: Distributed energy resources and the number of relays are expected to rise in modern electrical grids; consequently, relay misoperations are also expected to grow. Relays can detect electrical fault types using an internal algorithm and can display the result using light indicators on the front of the relay. However, some relays' internal algorithms for predicting types of electrical faults could be improved. This study assesses a relay's external and internal algorithms with an Advanced Synchronized Time Digital Grid Twin (ASTDGT) testbed with paired relays. A misoperation relay analysis focused on measuring the accuracy of using the boundary admittance (the external algorithm) versus the set-default (the internal algorithm) relay method to determine the electrical fault types was performed. In this study, the internal and external relay algorithms were assessed with a synchronized time digital grid twin testbed using a real-time simulator. This testbed evaluated two sets of logic at the same time with the digital grid twin and paired relays in the loop. Different types of electrical faults were simulated, and the relays' recorded events and electrical fault light indicator states were collected from the human–machine interfaces. This ASTDGT testbed with paired relays successfully evaluated the relay algorithm misoperations. The boundary admittance method had an accuracy of 100% for line-to-line, line-to-ground, and line-to-line ground faults.

Keywords: power system protection; relaying; relays; digital twin; testbed

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1. Introduction

Modern electrical networks are equipped with a higher number of relays [1–4], driven by the rapid expansion of distributed energy resources (DERs). This is because the integration of DERs requires the addition of more relays, which can increase the misoperations of relays. The North American Electric Reliability Corporation's PRC-004.6 [5] standard analyzes relay data to identify patterns in system protection operations that could adversely affect grid reliability. Misoperations in relays are primarily attributed to errors in settings, logic, or design, equipment malfunctions, and issues in communication networks [6,7]. Relays play a critical role as digital devices capable of identifying circuit breaker statuses [8,9], classifying types of electrical faults [10,11], identifying fault locations [12–14], and conveying this information rapidly through light indicators and/or digital displays.

Various types of relay protection logic are in place to execute essential functions [15], like presenting applications to clear faults [16], localizing electrical faults within the grid in power lines [17], and identifying electrical faulted phases [18]. The accuracy of relays in detecting phase faults using the sequence method is not completely accurate for detecting the fault type [10]. The sequence method is used to identify the electrical fault type in relays, which is achieved utilizing visual indicators such as lights and digital displays. This approach calculates the variation of angles between negative and zero sequence currents at the relay's location when a fault occurs [10].

The initial step for engineers in assessing fault events involves the rapid examination of the illuminated indicators on relays, which serves as a preliminary gauge for detecting the types of electrical faults [18]. However, the sequence technique's reliance on the zero and negative sequence angle of currents to identify the electrical fault types is not completely accurate because it produces identical angles for diverse fault scenarios [10]. Consequently, protection engineers are required to analyze the electrical fault state relay's behavior using the recorded events to accurately identify the nature of the disturbances, and this task is notably time-intensive [19,20].

To detect the specific faulted phase, a simple method is to measure the surge in current levels across each phase, as electrical faults typically induce an increase in the current magnitude [21]. In scenarios involving microgrids, whether connected to hydroelectric power sources (characterized by high inertia) or not, overcurrent relays can identify the faulted phases [22]. However, this method could be imprecise in electrical grids powered by inverter-based DERs with a lack of inertia [22]. The most usual faults in electrical grids are phase-to-ground faults. These faults can be identified by monitoring voltages, which drop in the faulted phase [23]. Considering that during a fault state the current increases while the voltage decreases, the ratio of voltage to current along power lines could serve as a reliable indicator for finding electrical fault types. Alternatively, a data-driven strategy leveraging phasor measurement unit data has been proposed, which does not need previous knowledge of the electrical grid configuration [24].

The impedance technique, which assesses both current and voltage magnitudes, offers another alternative for the identification of electrical fault types [11]. The phase-to-ground fault apparent (PGFA) impedance is based on the distance elements for mho relays [25,26], using a resistance–reactance (R-X) diagram. This is a plot that indicates the impedance variation of the power line over time (apparent impedance) [27]. Based on this, the impedance is captured within an R-X plane circle [14]. In this study, the PGFA admittance algorithm with phase and ground boundaries was used, and it was implemented using an external algorithm with a real-time simulator (RTS) and a relay in the loop. This algorithm presented by Dr. Piesciorovsky [28] computes the admittance magnitudes to identify electrical fault types. The PGFA admittance algorithm [28] was named boundary admittance in this article, and it was assessed against a set-default (internal algorithm) relay method for the first time.

The inaccuracy of the PGFA admittance algorithm is related to computation and sensor errors. For the computation error, the PGFA admittance algorithm [28] is based on using an inverse distance protection element, and then it can be presented using a complex current/voltage ratio [28]. Consequently, the current/voltage ratio error can be presented as the percentage current error minus the percentage voltage error [28]. If the percentage current and voltage errors have the same sign, the percentage voltage and current errors are mutually canceled, demonstrating good accuracy in the calculated admittance. However, the worst-case scenario could be when the percentage current error and the percentage voltage error have opposite signs [28] because these percentage errors are added, causing possible inaccuracy in the calculated admittance. For sensor errors, the admittance is calculated by measuring the phase currents and voltages. While the phase currents are measured with current transformers, they could be saturated during electrical fault states. This situation could affect the measurement of the phase currents and consequently the calculated admittance (admittance = current/voltage). However, phase voltages measured with potential transformers are usually not affected by the effect of saturation.

Digital twins have received significant attention in various industry domains, replicating physical systems of the real world as digital systems in the digital world [29]. In power system applications, digital twins have been used to monitor power system operations. In robot applications, digital twins have provided the framework for establishing interfaces for various manipulator systems [30]. In metrology applications, digital twins have been used to investigate the impact of misalignment on individual optical elements [31], with the development of digital twins for optical measurement systems, creating an algorithm

for a laser line scanner [32]. Another digital twin system has been used for meteorological applications, considering the essential requirements of simulating meteorological uncertainties [33]. Digital twins are created through simulations and off-line programs [34]; then, digital twin prototypes can be used for monitoring and testing applications to allow the verification of a process [35]. In this study, an Advanced Synchronized Time Digital Grid Twin (ASTDGT) testbed with paired relays is presented to assess the detection of different electrical fault types in a power grid, comparing the boundary admittance (external algorithm) method with a set-default (internal algorithm) relay method.

In electrical utility substations, electrical engineers normally use commercial relay test systems [36–38] to commission relays. These commercial relay test systems usually test one relay in the loop, and they are operated using a three-phase current/voltage power source that feeds the relay's analog signals. The relay test systems generate the states before, during, and after the fault states with breaker pole state sequences and trip/close signals to assess the relay settings and programmed logic (algorithms) during electrical fault tests. A proposed ASTDGT testbed with an RTS and paired relays was presented in this study. The ASTDGT testbed with paired relays allowed us to assess two different electrical fault detection algorithms with a synchronized time source and evaluate the event behavior for both relays with the same time stamp. The misoperation analysis between the boundary admittance method and the set-default (internal algorithm) relay method was carried out one using an RTS configured with two identical relays in the loop and simulating two similar digital power grids with the same electrical characteristics. The relay's front lighting signals (for detecting electrical fault types) and the recorded data from the relays were evaluated for the boundary admittance (external algorithm) method and the set-default (internal algorithm) relay approach. This study revealed the importance of integrating external algorithms with electrical grid boundaries, which could significantly enhance the accuracy of electrical fault type detection, and the use of the ASTDGT testbed with paired relays to assess the internal and external relay's logic to minimize possible relay misoperations.

The organization of this article describes the set-default (internal algorithm) relay method and the boundary admittance (external algorithm) method for detecting the types of electrical faults with relays. The ASTDGT testbed with paired relays and a synchronized time source system is described in detail. The relay results based on running different types of electrical faults are presented, and the relays' recorded events and the electrical fault light indicator states are analyzed. Then, the accuracy of the set-default (internal algorithm) relay method and the boundary admittance (external algorithm) method is assessed by plotting the results of the A, B, and C phases and the ground light indicators for the electrical fault tests. Then, using the ASTDGT testbed with the set-default (internal algorithm) relay method and the boundary admittance (external algorithm) method is discussed, and the conclusions of this study are presented.

2. The Set-Default Relay Method vs. the Boundary Admittance Method

2.1. The Set-Default Relay Method

A misoperation analysis of the set-default relay method and the boundary admittance method for the detection of electrical fault types in relays was performed with two identical SEL 451 relays [18]. While the set-default relay method was based on an internal algorithm applied to the protection device by itself, the boundary admittance method was implemented using an external algorithm applied in an RTS. The set-default relay method uses A, B, and C phases and ground targets that are based on illuminating the relay targets. This method defines which phases and/or grounds are involved in an electrical fault. The relay logic target words for the phases (A, B, and C) and ground (GND) status are included in the default relay settings for the T9_LED to T12_LED settings, as shown in Figure 1a. The fault types were defined as line-to-ground (LG), line-to-line (LL), three-line (3L), line-to-line ground (LLG), and three-line-to-ground (3LG) electrical faults and were detected based on

the electrical fault target lighting in Figure 1b. The acSELerator QuickSet SEL-5030 software (version 7.2.2.4) was used to set the SEL 451 relays and collect the plots in Figure 1.

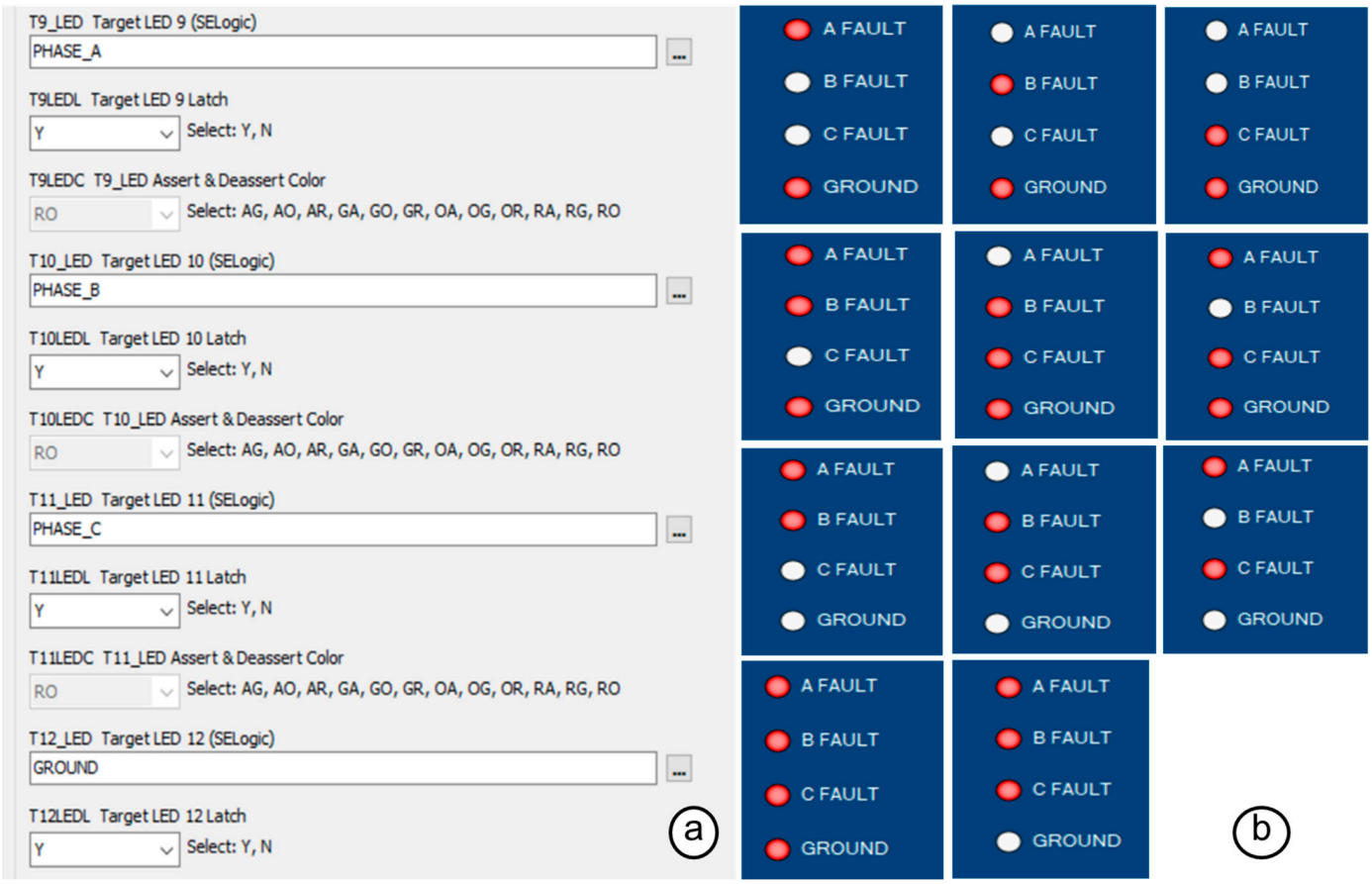

Figure 1. Target LED settings (**a**) and types of electrical faults (**b**) for the set-default relay method.

In this method, an LG electrical fault between the A phase and the ground illuminates both the A FAULT and GROUND targets. An LL electrical fault between the A and B phases illuminates the A FAULT and B FAULT targets. This set-default relay method does not require the pre-calculation of settings, and it is used at any site where a relay is installed in an electrical grid. The logic circuit of the LED target settings for the A, B, and C phases and ground is based on internal logic that cannot be modified. However, the target LEDs from the T9_LED to T12_LED settings can be set with other relay targeting logic, different from the factory target LED settings, to study the results of using new methods to detect electrical fault types. In Figure 1b, the red circles represent the phase and ground faulted states for the different types of electrical faults.

2.2. The Boundary Admittance Method

The boundary admittance method was based on implementing an external logic circuit using the algorithm in Figure 2, based on a previous algorithm presented by Dr. Piesciorovsky [28]; it was validated with a software simulation without relays in the loop. It needs to calculate the total admittance (Y_T), the total zero sequence admittance (Y_{T0}), and the zero sequence compensation factor (K_0) for the electrical grid circuit. The phase currents and voltages are measured at the relay location to calculate the PGFA admittance for phases A, B, and C. The phase and ground boundaries define the phase and ground faults based on identifying the desired conditions of the phases (A, B, C) and ground light indicators (Figure 2) for faulted and non-faulted states.

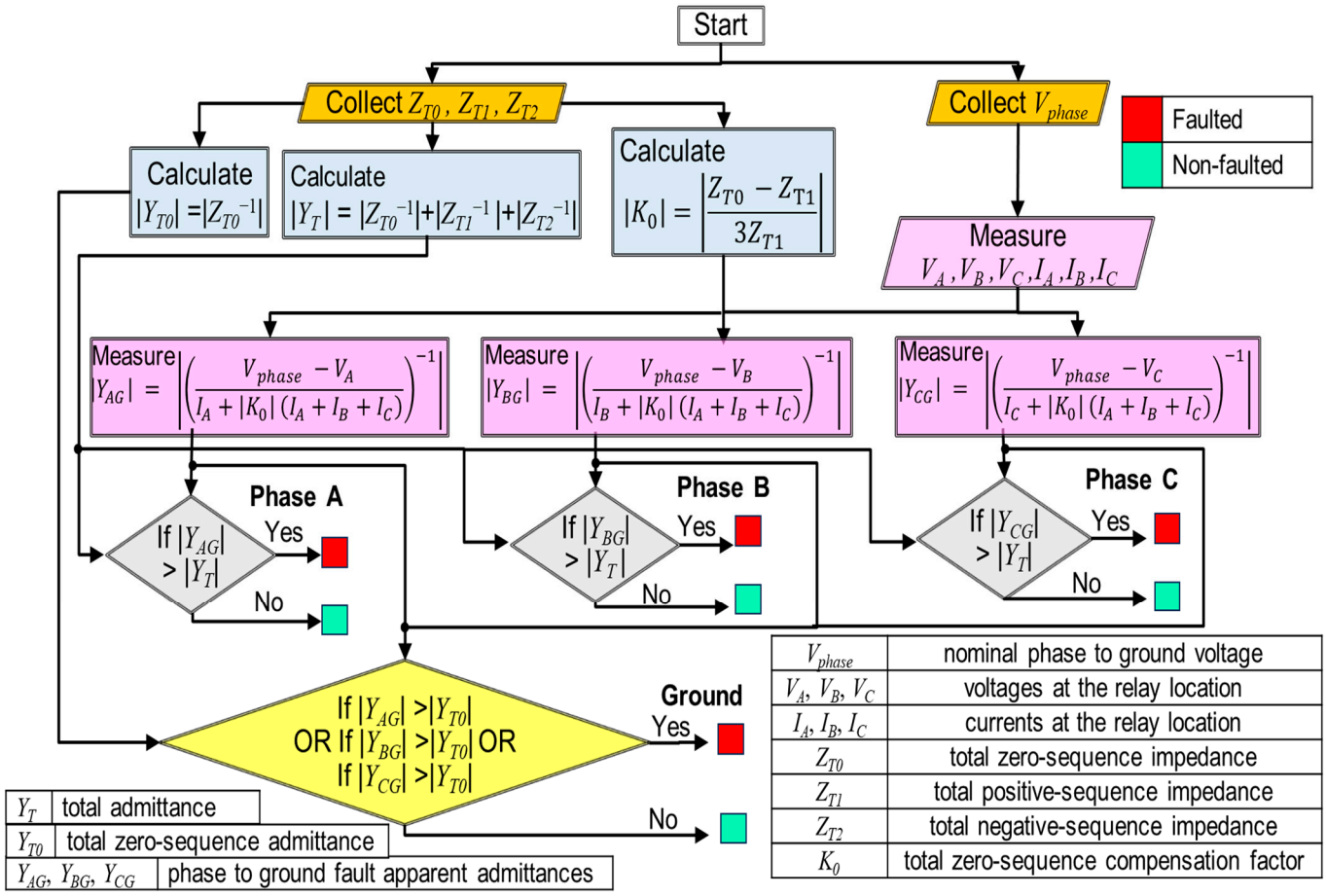

Figure 2. Phase-to-ground fault apparent admittance algorithm [28].

The boundary admittance method is based on measuring the inverse impedance magnitude to identify electrical fault types. In Figure 2, the voltages (V_A, V_B, V_C), and currents (I_A, I_B, I_C) at the location of the breaker were recorded to calculate the PGFA admittance magnitude during faulted and non-faulted states. From Figure 2 [28], the PGFA admittance magnitude for a generic phase p is given by Equation (1),

$$|Y_{pg}| = \left|\left(\frac{V_{phase} - V_p}{I_p + |K_0|\,(I_A + I_B + I_C)}\right)^{-1}\right|. \quad (1)$$

where Y_{pg} is the PGFA admittance magnitude for a p generic phase in siemens, V_{phase} is the nominal phase-to-ground voltage in volts, V_p is the measured line-to-ground voltage for a p generic phase in volts, I_p is the measured current for a p generic phase in amps, I_A, I_B, I_C are the measured phase currents in amps, and K_0 is the total zero sequence current compensation factor calculated by Equation (2),

$$K_0 = \frac{Z_{T0} - Z_{T1}}{3Z_{T1}}, \quad (2)$$

where Z_{T0} and Z_{T1} are the total zero and positive sequence impedance in ohms.

In Equation (2), the zero sequence current compensation factor magnitude ($|K_0|$) and the angle ($K_{0<}$) of the power line sections were implemented to define the boundary admittance algorithm. Then, $|K_0|$ and $K_{0<}$ were calculated using Equations (3) and (4), respectively.

$$|K_0| = \left|\frac{Z_{T0} - Z_{T1}}{3Z_{T1}}\right|, \quad (3)$$

$$K_{0<} = \tan^{-1}\left(\frac{K_{0\ imag}}{K_{0\ real}}\right), \tag{4}$$

where $K_{0\ imag}$ and $K_{0\ real}$ are the imaginary and real parts of the zero sequence current compensation factor magnitude, respectively.

In Figure 2, the phase and ground conditions represent the admittance boundaries for detecting the fault types. Then, the faulted phase and ground zones were defined by $|Y_T|$ and $|Y_{T0}|$, respectively. The phase faulted zones for the admittance were given by Equation (5) in siemens,

$$|Y_{pg}| > |Y_T| = \left|\left(\frac{R_T}{R_T^2 + X_T^2}\right) + i\left(\frac{-X_T}{R_T^2 + X_T^2}\right)\right| (phase\ faulted\ zone), \tag{5}$$

and the ground faulted zone for the measured admittance magnitudes was given by Equation (6) in siemens,

$$|Y_{pg}| > |Y_{T0}| = \left|\left(\frac{R_T}{R_T^2 + X_T^2}\right) + i\left(\frac{-X_T}{R_T^2 + X_T^2}\right)\right| (ground\ faulted\ zone). \tag{6}$$

where Y_{pg} is the PGFA admittance magnitude for a p generic phase in siemens, Y_T is the phase faulted zone limit in siemens, Y_{T0} is the ground faulted zone limit in siemens, R_T is the total resistance of the power line sections in ohms, and X_T is the total reactance of the power line sections in ohms.

With the boundary admittance method (external algorithm), from the A, B, and C phase and ground conditions (Figure 2) in Equations (5) and (6), the phases (A, B, C) and ground states are defined using a well-established algorithm that shows how green (non-faulted states) or red (faulted states) light indicator sequences define the electrical fault types.

3. Materials and Methods

3.1. The Advanced Synchronized Time Digital Grid Twin Testbed with Paired Relays

In the ASTDGT testbed, the set-default relay method (internal algorithm) and boundary admittance method (external algorithm) were evaluated. The set-default relay method was defined by internal relay logic, and it only depended on setting the A, B, and C phase and ground target LEDs (Figure 1) without the need to modify the setting values. However, the boundary admittance method used an external algorithm that was run with an RTS and the relay in the loop. In this external algorithm, the phase-to-ground fault apparent admittance application (Figure 2) required the sequence impedance of the power line sections to be collected to calculate the total admittance (Y_T), total zero sequence admittance (Y_{T0}), and zero sequence compensation factor (K_0) for the electrical grid circuit. These setting values (Y_T, Y_{T0}, K_0) were set directly in the external algorithm implemented by the RTS (target computer) using the Windows command station (host computer) as an interface (Figure 3) via Transmission Control Protocol/Internet Protocol (TCP/IP). However, the RTS can be connected either directly to the host computer (direct connection), like in Figure 3, or via a local area network (a local area network configuration). In the ASTDGT testbed, the algorithm of the boundary admittance method was implemented with the RTS. Then, the algorithm signal outputs of the RTS were connected directly to the relay control inputs, which allows relays from different manufacturers with control inputs to be used for future applications. The ASTDGT testbed with paired relays was implemented to analyze the misoperations of the boundary admittance method (external algorithm) and the set-default relay method (internal algorithm) to determine the electrical fault types based on the light indicators of the relays (Figure 3). The testbed diagram includes a host computer (Figure 3a) with a time source system (Figure 3b) and an RTS (Figure 3c), which were connected to the relays (Figure 3c,d) with a human–machine interface (HMI) computer (Figure 3a).

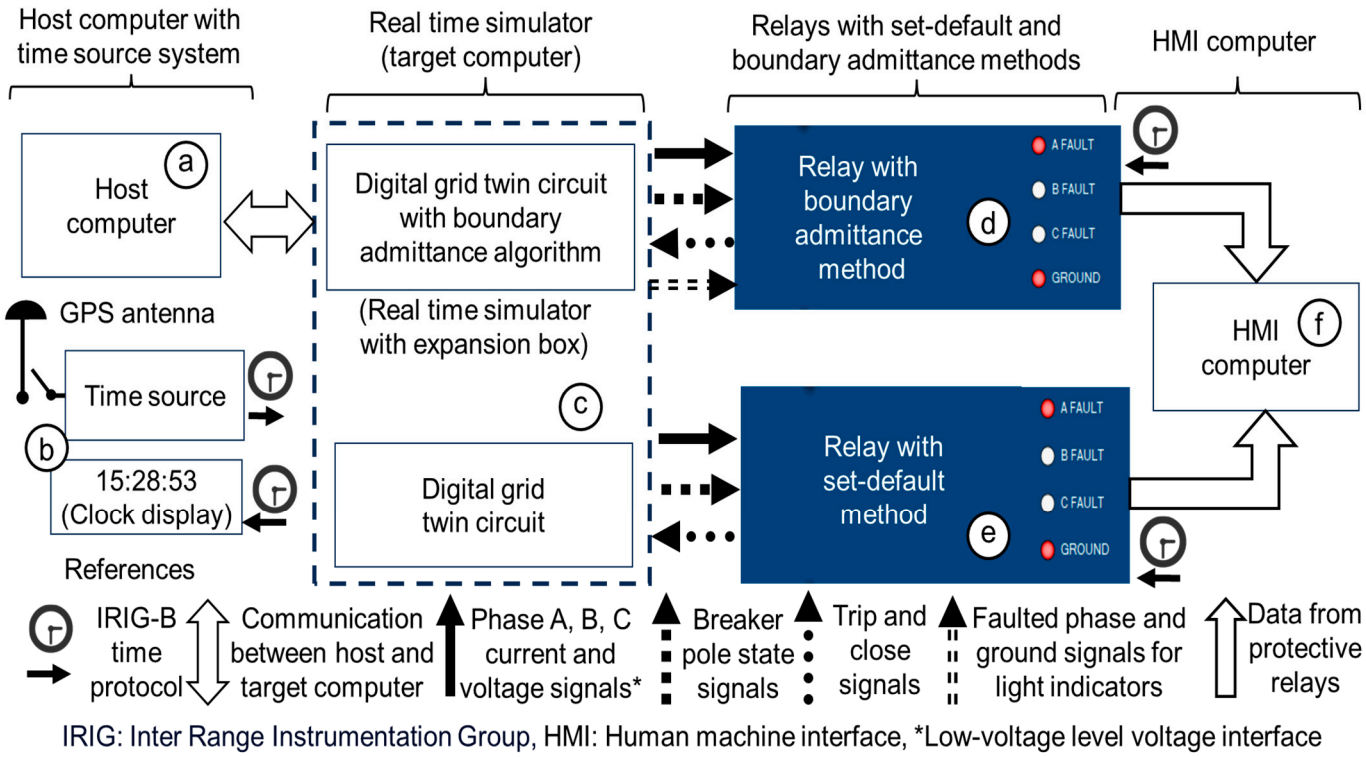

Figure 3. Host computer with time source system (**a**,**b**), real-time simulator (**c**), relays (**d**,**e**), and human–machine interface (HMI) computer (**f**).

Inside the RTS (target computer), the digital grid twin circuits were set with the boundary admittance algorithm (Figure 3c). One digital grid twin circuit with the boundary admittance algorithm (Figure 3c) was connected to a relay (Figure 3d), and another identical relay with the set-default algorithm (Figure 3e) was connected to the second digital grid twin circuit (Figure 3c). The HMI computer (Figure 3f) collected the data from the relays. The host computer (Figure 3a) downloaded and ran the RT-LAB project to execute and supervise the tests. The RTS (Figure 3c) generated the phase current and voltage signals (solid arrows), which were injected into the relays and generated the breaker pole state signals (square arrows) that were collected from the relays. The relays generated the trip/close signals (dotted arrows) that controlled the breakers inside of the digital grid twin circuits. The phases (A, B, C) and ground light indicator signals (double-dashed arrows) were generated from the boundary admittance algorithm in the RTS and collected by the relay (Figure 3d). The time source (Figure 3b) could be synchronized using a GPS antenna (or an internal clock of the time source), which set the same time stamp for all relays with the Inter Range Instrumentation Group-B protocol. This protocol is an important tool for assessing the time stamps from the recorded events for both relays by observing whether a delay time is present in the implemented boundary admittance method. Figure 4a shows the relay front side with the clock display (CD) and the relays. Figure 4b shows the relay rear side with the faulted phase and ground signals for the light indicators connected to the control input IN202-03-04-05 of the relay with the boundary admittance method (RWBAM). Figure 4c shows the RTS with an expansion box that simulates the digital grid twin circuits for the relays and the boundary admittance algorithm.

In Figure 4, the RTS interacts with the relay using the boundary admittance method (RWBAM) and the relay with the set-default method (RWSDM). The RTS analog output signals for the phase current/voltage signals were wired to the low-voltage level interface of the SEL 451 relays' front sides (Figure 4a). In the relays, the current and voltage gains for the RTS were calculated at the low-voltage level interface using the current and voltage scaling factors from the relay's instruction manual [18]. The analog signals for the relays

were scaled using simulated phase currents and voltages with gain blocks. These current and voltage gains were calculated by Equations (7) and (8), respectively.

$$CG_R = 1/(CTR_R \times CSF) \tag{7}$$

where CG_R is the current gain in the RTS for the relay, CTR_R is the current transformer ratio of the relay (80), and CSF is the SEL 451 relay's current scaling factor (75 A/V) in amperes per volt.

$$VG_R = 1/(PTR_R \times VSF) \tag{8}$$

where VG_R is the voltage gain in the RTS for the relay, PTR_R is the potential transformer ratio of the relay (60), and VSF is the SEL 451 relay's voltage scaling factor (150 V/V) in volts per volt.

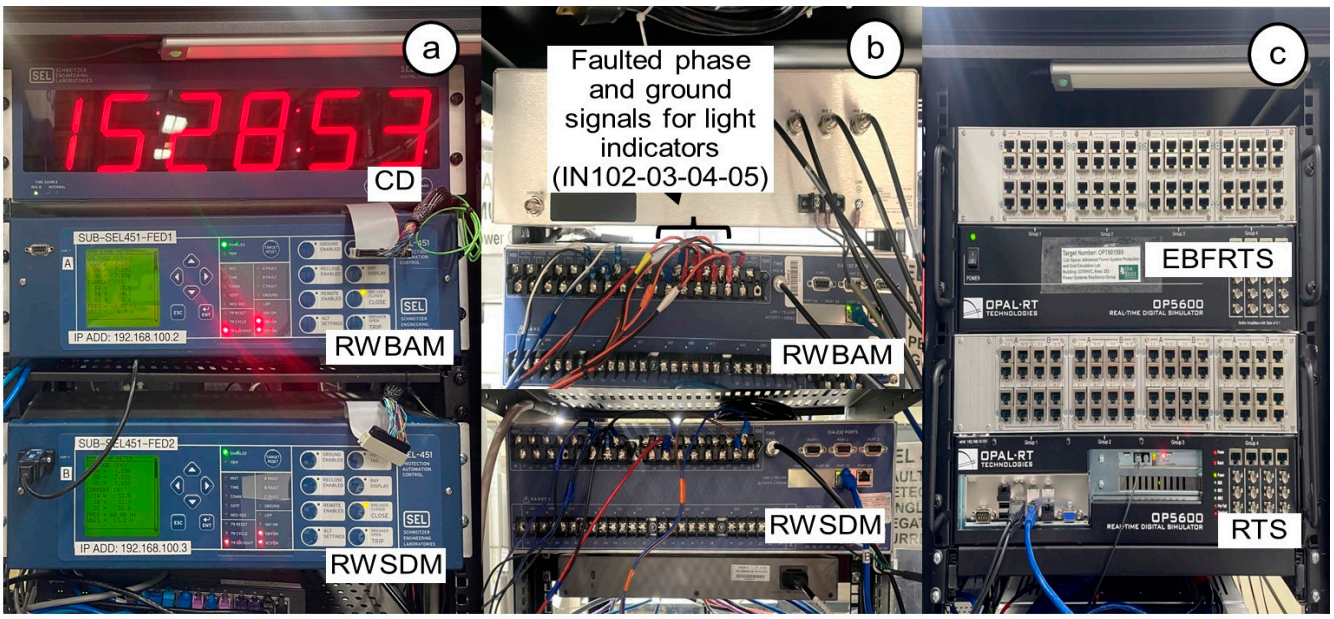

Figure 4. Testbed relay's front (**a**) and rear (**b**) sides with the real-time simulator (**c**).

In the RTS, the analog inputs for the trip/close signals of the breakers were connected to the control outputs of the relay's rear sides (Figure 4b). The RTS digital outputs for the breaker pole state and the faulted phases and ground signals for the light indicators were wired to the control inputs of the relay's rear sides (Figure 4b).

3.2. A Single-Line Diagram of the Digital Grid Twin

In this experimental model, the digital grid twin was created in an RT-LAB project using part of the Electric Power Board (EPB) Riverside substation [22]. Single-line diagrams of the electrical grid for the digital grid twin are shown in Figure 5. This electrical configuration was a radial system with a 7.2 kV phase-to-ground voltage. The digital grid twin grid circuits were set into the RTS (Figure 5a,b), and the relays were the hardware-in-the-loop. In Figure 5a, the boundary admittance algorithm was run inside the RTS, and the outputs of the algorithm were wired to the relay's control inputs. However, the set-default relay algorithm was run inside the relay (Figure 5b). The boundary admittance algorithm (Figure 5a) and the set-default relay (Figure 5b) algorithm were applied between power line sections 27 and 38. The purpose was to assess both algorithms for different electrical faults near the relay's breaker and at the end of power line section 38.

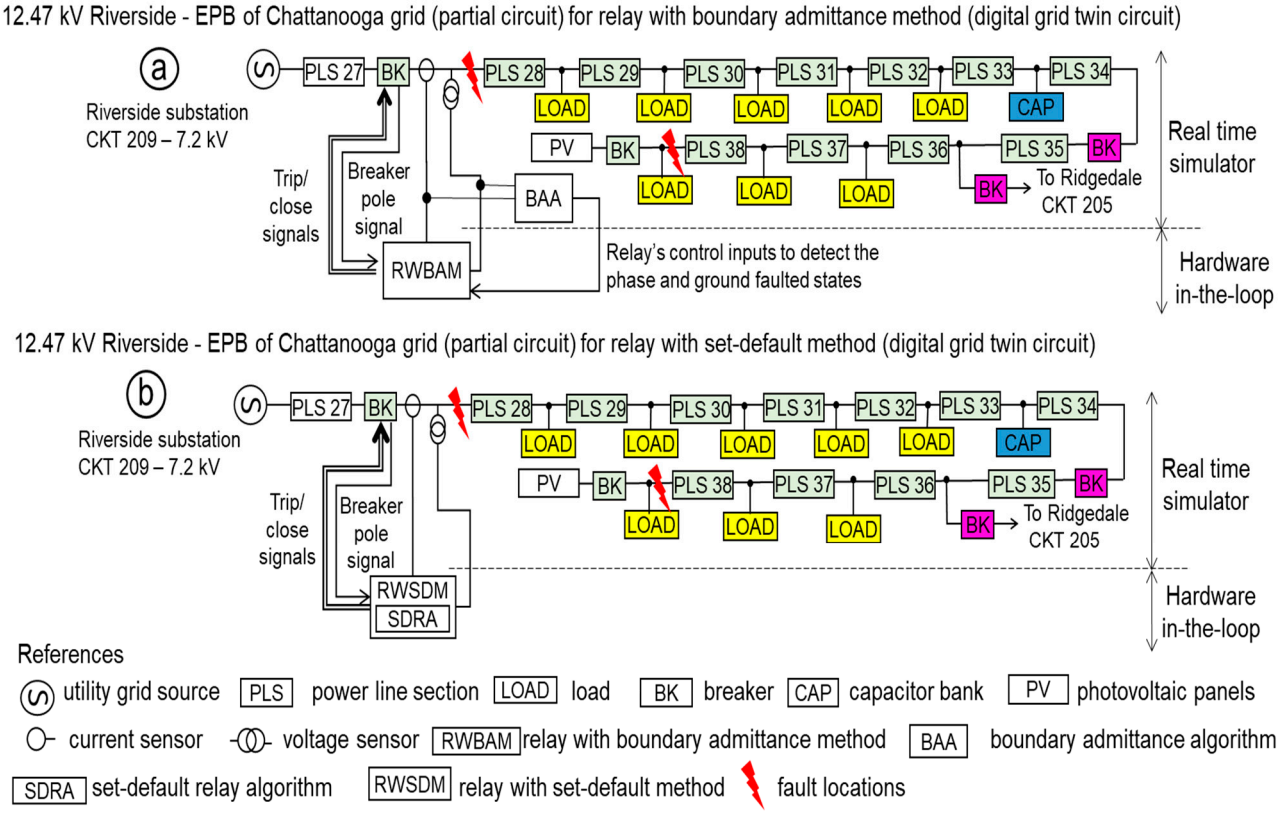

Figure 5. Single-line diagram of digital grid twin for relay with boundary admittance (**a**) and set-default (**b**) methods.

3.3. A Three-Line Diagram of the Digital Grid Twin

The RT-LAB project was built to run the use case tests. Figure 6 shows three-line diagrams of the digital grid twin that were created with MATLAB/Simulink models, based on Figure 5. The electrical grid circuits for the relays with the boundary admittance method and the set-default relay method are shown in Figure 6a and 6b, respectively. The three-line diagrams of the EPB Riverside microgrid partial circuit (Figure 6a,b) show the fault block circuit (Figure 6c), fault blocks (Figure 6d,e), breaker signals (Figure 6f,g), three phase breakers (Figure 6h,i), and analog signals (Figure 6j,k).

The digital grid twin three-line diagrams (Figure 6a,b) include the source, capacitor banks, power lines, loads, and breakers. In this study, the tests were run for 10 s, and the faults were created by fault blocks (Figure 6d,e) controlled by the fault block circuit (Figure 6c) that triggered fault states at 5 s. The fault tests were based on generating different electrical faults located near the breaker site and at the end of power line section 38. IntelliRupters were used in the power grid circuit of the EPB in Chattanooga [22]. However, two identical SEL 451 relays were used in the digital grid twin circuits (Figure 6a,b). The sensor blocks (Figure 6j,k) collected the currents and voltages at the three phase breaker locations (Figure 6h,i). Tests for the same types of electrical faults and locations were run in synchronized time using these two identical electrical grid circuits and the recorded events from the relays collected with the same time stamp.

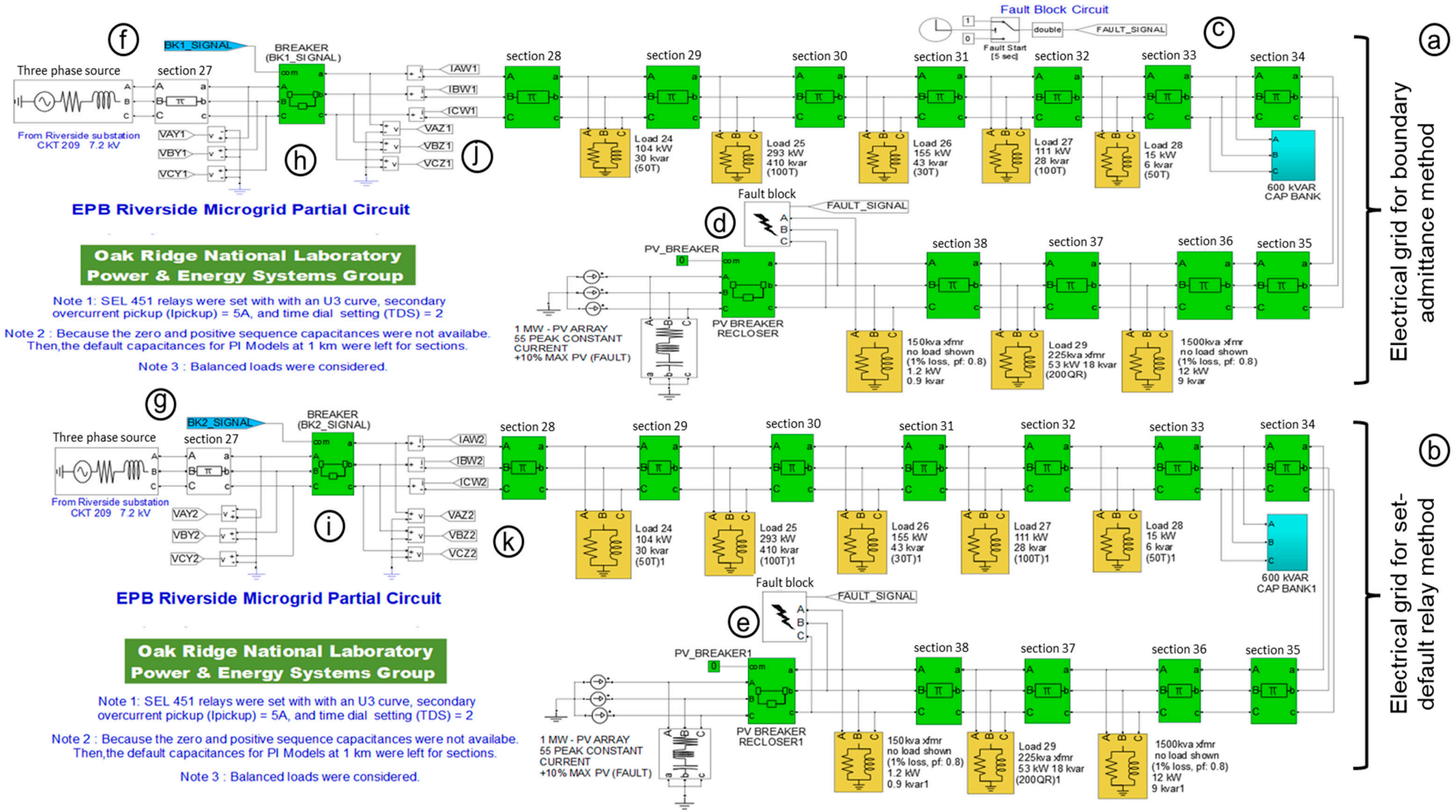

Figure 6. Three-line diagram of digital grid twin of EPB Riverside microgrid partial circuit (**a**,**b**), fault block circuit (**c**), fault block (**d**,**e**), breaker signals (**f**,**g**), three phase breakers (**h**,**i**), and analog signals (**j**,**k**).

3.4. Twin Relay Settings

In the ASTDGT testbed, the paired SEL 451 relays [18] were set with an inverse time overcurrent protection scheme because SEL 451 relays [18] are mainly overcurrent relays and they were located near feeder loads (Figure 5). However, different protection schemes could be applied in the relays of the ASTDGT testbed depending on the power grid topology for the RT-LAB project, the types of relays (overcurrent, distance, differential, etc.), and the relay locations (feeders, transformers, generators, etc.) in the power grid. In this study, the paired relays were set with the same inverse time current (ITC) curve settings. The U3 Very ITC curve was given by Equation (9), and the relays had a time dial setting (*TDS*) of 2 s, a current transformer ratio (*CTR*) of 80, and a relay current pickup (I_P) of 5 A.

$$T_R = TDS \times \left(K_1 + \frac{K_2}{\left(I_{primary}/CTR/I_P \right)^{K_3} - 1} \right) \times 60, \quad (9)$$

where T_R is the relay time in cycles, $I_{primary}$ is the primary current in amperes, and K_1 (0.0963), K_2 (3.88), and K_3 (2) are the constants of the ITC curve (U3).

The inverse time current curves of the relays allowed us to trip the breakers (Figure 6h,i) at the fault currents. In the ASTDGT testbed (Figure 3), selectivity coordination between the primary and backup relays was not performed because one relay was set for each digital grid twin (Figure 5), and the boundary admittance (external algorithm) method and set-default (internal algorithm) relay method determined the electrical fault types without the necessity of studying the selectivity coordination.

The electrical fault tests were performed for 10 s. In the relays, the target LEDs for identifying the electrical fault types were set based on Table 1. The LEDs for the phases (A, B, C) and the ground were given by the T9_LED, T10_LED, T11_LED, and T12_LED settings, respectively. However, the LED settings for the relay using the boundary admittance (external algorithm) method were given by the control inputs IN102, IN103, IN104, and IN105 (Figure 4b) for the T9_LED–T12_LED settings, respectively.

Table 1. Target LED settings of relays to identify types of electrical faults.

Relay Front Panel Location and Setting Identification		**Relay Target LED Settings**	
Relay front panel location	Relay setting identification	Set-default (internal algorithm) relay method	Boundary admittance (external algorithm) method
A FAULT	T9_LED	PHASE_A	IN102
B FAULT	T10_LED	PHASE_B	IN103
C FAULT	T11_LED	PHASE_C	IN104
GROUND	T12_LED	GROUND	IN105

3.5. The Algorithm, Logic Circuit, and Boundaries

The algorithm and logic circuit for the boundary admittance method (Figure 7) were built in the RT-LAB project. In the relay, the signals of the IN102, IN103, IN104, and IN105 control inputs were generated by the boundary admittance algorithm for phases A, B, and C (Figure 7a–c) with the logic circuit (Figure 7d). In Figure 7, the boundary admittance algorithm for phases A, B, and C with the logic circuit was designed based on measuring the admittance with phase and ground boundaries to determine the electrical fault types, as shown in Figure 2.

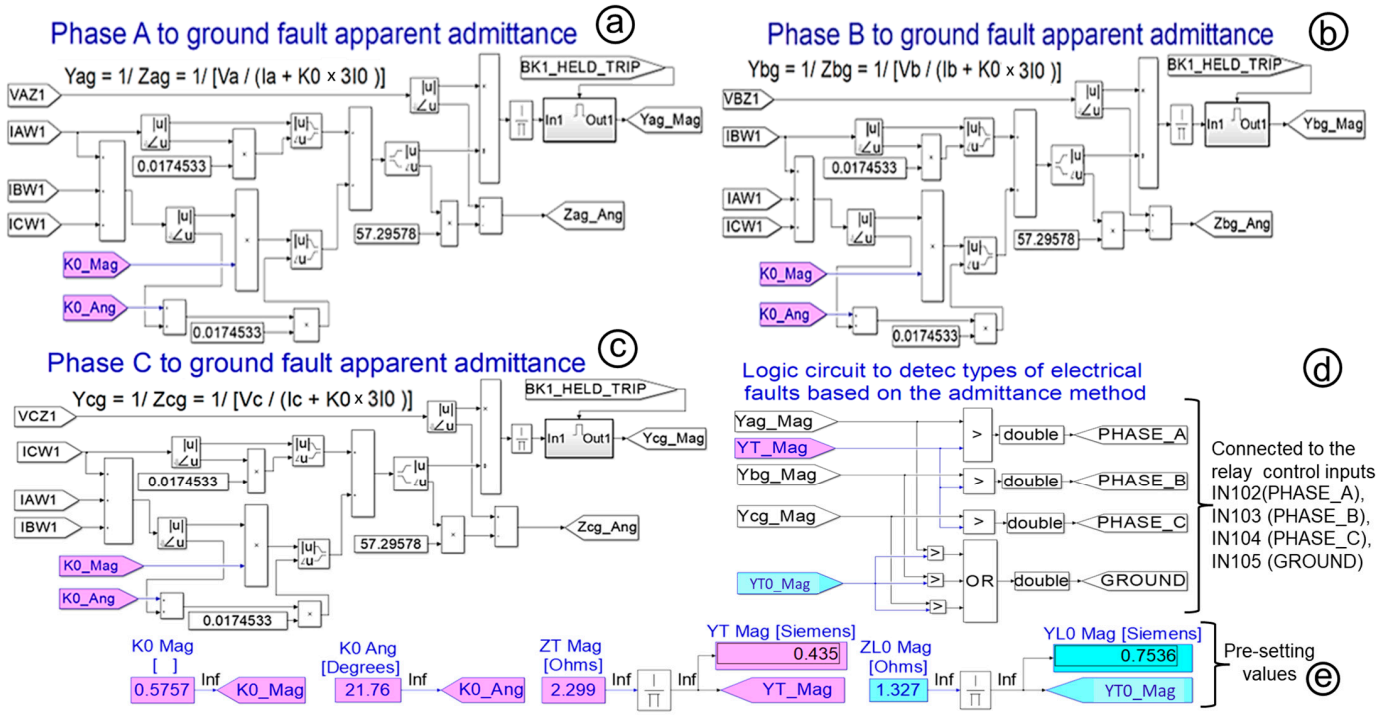

Figure 7. Phase-to-ground fault apparent admittance algorithm for phases A (**a**), B (**b**), and C (**c**) with the logic circuit (**d**) and pre-setting values (**e**) to find out the electrical fault types.

In the circuits in Figure 7a–c, the phase-to-neutral voltages (VAZ1, VBZ1, VCZ1) and phase currents (IAW1, IBW1, ICW1) were recorded from the voltage/current sensors (Figure 6j). The zero sequence current compensation factors (K0_Mag, K0_Ang) in Figure 7e were calculated with Equations (3) and (4), respectively, from power line sections 28 to 38 (Figure 6a). Figure 7 shows the logic circuit that recorded the phase-to-ground apparent admittance magnitude (Yag_Mag, Ybg_Mag, Yc_Mag) in Figure 7a–c. In Figure 7e, the total admittance magnitude (YT_Mag) and total zero sequence admittance (YT0_Mag) were calculated with Equations (5) and (6), respectively. Finally, the PHASE_A, PHASE_B, PHASE_C, and GROUND label signals (Figure 7d) were connected to control inputs IN102–IN105, respectively, for the relay using the boundary admittance method. Table 2 shows the steps used to calculate the limits of the boundary admittance method for the phase and ground faulted zones for the electrical grid circuit in Figure 6a, set as "YT_Mag" and "YT0_Mag" in Figure 7e. In Table 2, the total resistance (R_T) and reactance (X_T) and the total zero sequence resistance (R_{T0}) and zero reactance (X_{T0}) from power line sections 28 to 38 (Figure 6a) were calculated. Then, the magnitudes of the total admittance ($|Y_T|$) and the total zero sequence admittance ($|Y_{T0}|$) were calculated with Equation (5) and (6), respectively. These admittances define the phase and ground faulted zone limits for the boundary admittance method to detect the fault type with the relay's light indicators. The limit of the boundary admittance method for the phase faulted zone was $|Y_{pg}| > |Y_T| = 0.435$ siemens, and for the ground faulted zone, it was $|Y_{pg}| > |Y_{T0}| = 0.7536$ siemens (Table 2).

Table 2. Calculation steps.

1—Computation of Total Resistance and Reactance from Power Line Sections 28–38				2—Computation of Total Admittance	3—Computation of Boundaries
R_{T1}	X_{T1}	$R_T = 2\,R_{T1} + R_{T0}$	$X_T = 2\,X_{T1} + X_{T0}$	$\|Y_T\|$	$\|Y_{pg}\| > \|Y_T\|$
0.3044 Ω	0.3900 Ω	1.1518 Ω	1.9904 Ω	0.435 S	$\|Y_{pg}\| > 0.435$ S
R_{T0}	X_{T0}			$\|Y_{T0}\|$	$\|Y_{pg}\| > \|Y_{T0}\|$
0.5430 Ω	1.2104 Ω			0.7536 S	$\|Y_{pg}\| > 0.7536$ S

4. Results

4.1. Events and Tests

In this study, the analog signals (voltages and currents) and digital signals (trip phases and ground variables) were generated in the pre-fault, fault, and post-fault states. These recorded events were collected by the relays using the set-default relay method and the boundary admittance method to identify the electrical fault types using the phase (A, B, C) and ground light indicators on the relays. The boundary admittance method uses PGFA admittance with phase and ground boundaries [28], and the set-default relay method uses an internal algorithm. Figure 8a,b show the relay events recorded during this study. These figures compare the phase currents (i), phase-to-neutral voltages (ii), digital signals (iii), event data (iv), and phase/ground LED (v) results from the relays using the boundary admittance (Figure 8a) and set-default (Figure 8b) relay methods. The relays used a time source system (Figure 3b), and the same time stamps (hh:mm:ss:mmm = 9:04:03:849 and 9:04:03:852) were used for the same two algorithm events (Figure 8a,b). The boundary admittance method did not show a delay time compared to the set-default relay method. Then, the application of the relay's control inputs was validated with the external algorithm implemented in the RTS (Figure 3c). The tests were run for electrical faults located at the breaker site and the power line section 38 site. The events were recorded and compared for each test with the boundary admittance and set-default relay methods. Although the actual electrical fault type was an ABC electrical fault, the relay with the boundary admittance method detected an ABCG electrical fault (Figure 8a), and the relay with the set-default method detected an ACG electrical fault (Figure 8c). The measured values were considered the types of electrical faults collected from the relays, and the true values were considered the types of electrical faults set on the MATLAB/Simulink fault blocks (Figure 6d,e) before initiating the tests. Table 3 shows the measured values compared with the true values for the electrical fault tests using the boundary admittance method and the set-default relay method with the ASTDGT testbed (Figures 3 and 4). The synchroWAVe Event software (version 1.9.0.89) was used to plot and analyze the data stored in the relays, as shown in Figure 8.

Table 3. Results for electrical fault tests using the boundary admittance and set-default relay methods.

Test No.	Test Name (Method_Fault Location_Fault Type)	Measured Values						True Values
		Relay Event No.	Electrical Fault on Relay's LED				Results	Electrical Fault in MATLAB Fault Block
			FAULT A	FAULT B	FAULT C	GND		
1	BOUNDARY ADMITTANCE METHOD_BREAKER_AG	10,814	X			X	AG	AG
	SET-DEFAULT RELAY METHOD_BREAKER_AG	11,232	X	X		X	ABG	
2	BOUNDARY ADMITTANCE METHOD_BREAKER_BG	10,815		X		X	BG	BG
	SET-DEFAULT RELAY METHOD_BREAKER_BG	11,233		X		X	BG	
3	BOUNDARY ADMITTANCE METHOD_BREAKER_CG	10,816			X	X	CG	CG
	SET-DEFAULT RELAY METHOD_BREAKER_CG	11,234		X	X	X	BCG	
4	BOUNDARY ADMITTANCE METHOD_BREAKER_ABG	10,817	X	X		X	ABG	ABG
	SET-DEFAULT RELAY METHOD_BREAKER_ABG	11,235	X	X		X	ABG	

Table 3. *Cont.*

Test No.	Test Name (Method_Fault Location_Fault Type)	Measured Values						True Values
		Relay Event No.	Electrical Fault on Relay's LED				Results	Electrical Fault in MATLAB Fault Block
			FAULT A	FAULT B	FAULT C	GND		
5	BOUNDARY ADMITTANCE METHOD_BREAKER_BCG	10,818		X	X	X	BCG	BCG
	SET-DEFAULT RELAY METHOD_BREAKER_BCG	11,236		X	X	X	BCG	
6	BOUNDARY ADMITTANCE METHOD_BREAKER_ACG	10,819	X		X	X	ACG	ACG
	SET-DEFAULT RELAY METHOD_BREAKER_ACG	11,237	X		X	X	ACG	
7	BOUNDARY ADMITTANCE METHOD_BREAKER_AB	10,820	X	X			AB	AB
	SET-DEFAULT RELAY METHOD_BREAKER_AB	11,238	X	X			AB	
8	BOUNDARY ADMITTANCE METHOD_BREAKER_BC	10,821		X	X		BC	BC
	SET-DEFAULT RELAY METHOD_BREAKER_BC	11,239		X	X		BC	
9	BOUNDARY ADMITTANCE METHOD_BREAKER_AC	10,822	X		X		AC	AC
	SET-DEFAULT RELAY METHOD_BREAKER_AC	11,240	X		X		AC	
10	BOUNDARY ADMITTANCE METHOD_BREAKER_ABCG	10,840	X	X	X	X	ABCG	ABCG
	SET-DEFAULT RELAY METHOD_BREAKER_ABCG	11,258	X		X	X	ACG	
11	BOUNDARY ADMITTANCE METHOD_BREAKER_ABC	10,841	X	X	X	X	ABCG	ABC
	SET-DEFAULT RELAY METHOD_BREAKER_ABC	11,259	X	X	X		ABC	
12	BOUNDARY ADMITTANCE METHOD_SECTION38_AG	10,847	X			X	AG	AG
	SET-DEFAULT RELAY METHOD_SECTION38_AG	11,275	X			X	AG	
13	BOUNDARY ADMITTANCE METHOD_SECTION38_BG	10,848		X		X	BG	BG
	SET-DEFAULT RELAY METHOD_SECTION38_BG	11,276		X	X	X	BCG	
14	BOUNDARY ADMITTANCE METHOD_SECTION38_CG	10,849			X	X	CG	CG
	SET-DEFAULT RELAY METHOD_SECTION38_CG	11,277			X	X	CG	
15	BOUNDARY ADMITTANCE METHOD_SECTION38_ABG	10,851	X	X		X	ABG	ABG
	SET-DEFAULT RELAY METHOD_SECTION38_ABG	11,279	X	X		X	ABG	
16	BOUNDARY ADMITTANCE METHOD_SECTION38_BCG	10,852		X	X	X	BCG	BCG
	SET-DEFAULT RELAY METHOD_SECTION38_BCG	11,280		X	X	X	BCG	

Table 3. *Cont.*

Test No.	Test Name (Method_Fault Location_Fault Type)	Measured Values						True Values
		Relay Event No.	Electrical Fault on Relay's LED				Results	Electrical Fault in MATLAB Fault Block
			FAULT A	FAULT B	FAULT C	GND		
17	BOUNDARY ADMITTANCE METHOD_SECTION38_ACG	10,853	X		X	X	ACG	ACG
	SET-DEFAULT RELAY METHOD_SECTION38_ACG	11,281	X		X	X	ACG	
18	BOUNDARY ADMITTANCE METHOD_SECTION38_AB	10,854	X	X			AB	AB
	SET-DEFAULT RELAY METHOD_SECTION38_AB	11,282	X	X			AB	
19	BOUNDARY ADMITTANCE METHOD_SECTION38_BC	10,855		X	X		BC	BC
	SET-DEFAULT RELAY METHOD_SECTION38_BC	11,283		X	X		BC	
20	BOUNDARY ADMITTANCE METHOD_SECTION38_AC	10,856	X		X		AC	AC
	SET-DEFAULT RELAY METHOD_SECTION38_AC	11,284	X		X		AC	
21	BOUNDARY ADMITTANCE METHOD_SECTION38_ABCG	10,857	X	X	X	X	ABCG	ABCG
	SET-DEFAULT RELAY METHOD_SECTION38_ABCG	11,285	X		X	X	ACG	
22	BOUNDARY ADMITTANCE METHOD_SECTION38_ABC	10,858	X	X	X	X	ABCG	ABC
	SET-DEFAULT RELAY METHOD_SECTION38_ABC	11,286		X	X		BC	

Table 3 shows the measured values for the electrical fault tests using the boundary admittance method and the set-default relay method alongside the true values. The measured values are the results from the target values of the phase (A, B, C) and ground (GND) LEDs that were collected from the relay events. The true values are the types of electrical faults that were set in the fault blocks (Figure 6d,e) in the RT-LAB project for each test before running the simulations. The same type of electrical fault was set in both fault blocks for each test, and the tests for the boundary admittance method and the set-default relay method were run together using the digital grid twin three-line diagram of the EPB Riverside microgrid partial circuit (Figure 6a,b). In Table 3, the test name column specifies the type of electrical fault and its location on the power grid. The electrical fault tests were conducted near the relay's breaker site and at the end of the power line section 38 site (Figure 5). From Table 3, the columns with the results and the true values were compared to assess whether the types of electrical faults detected by the boundary admittance method and the set-default relay method matched the types of electrical faults indicated in the column of the true values.

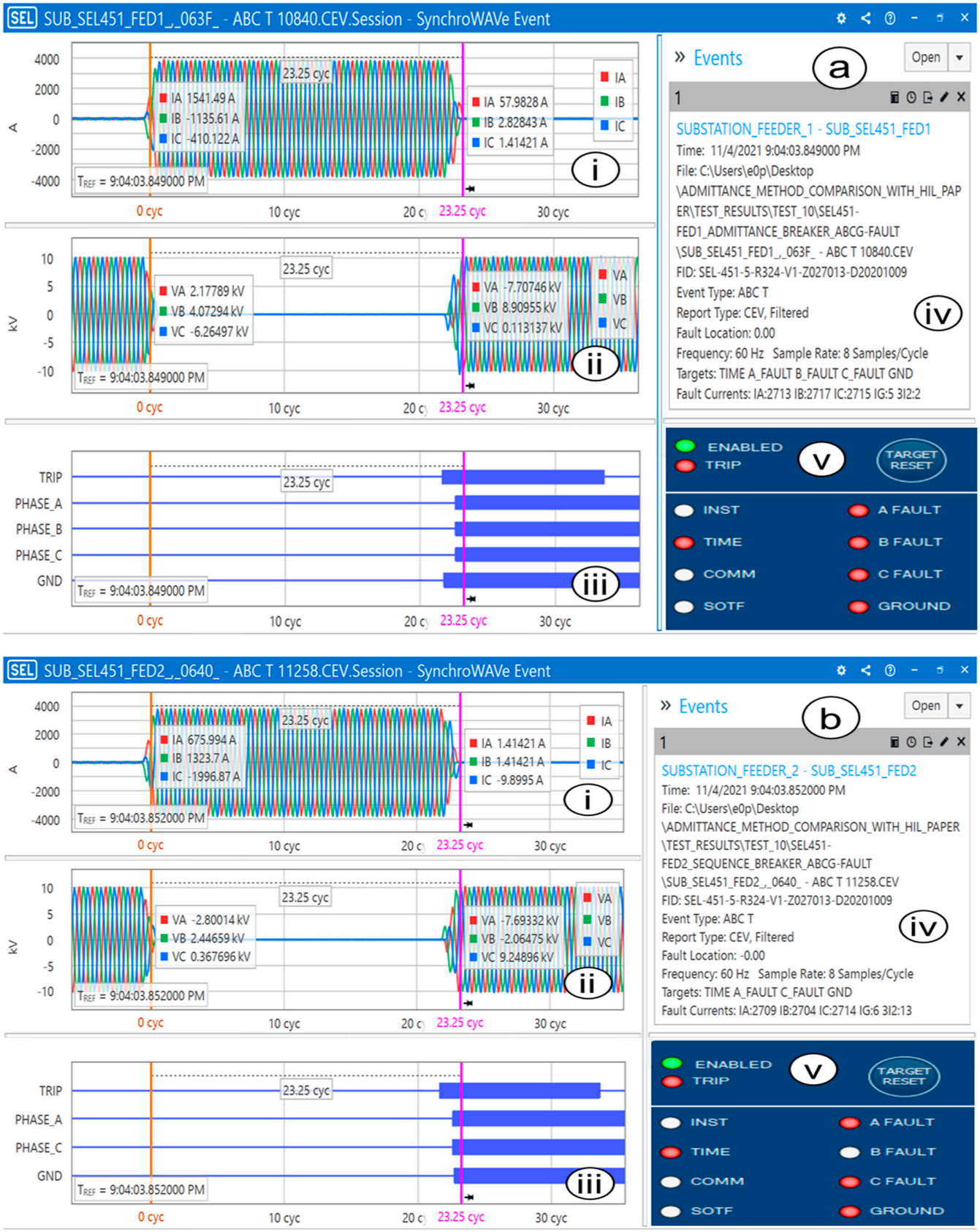

Figure 8. Phase currents (**i**), phase-to-neutral voltages (**ii**), digital signals (**iii**), event data (**iv**), and phase/ground LED (**v**) results from the relays with the boundary admittance (**a**) and set-default (**b**) relay methods.

4.2. Analysis of the Measured Phase and Ground LED States

The results for the phase (A, B, C) and ground LEDs from Table 3 are plotted in Figure 9. The true and measured values for the phase and ground LEDs were compared to see how they matched for both the set-default relay method and boundary admittance method. Black cross dots represent the true values, and blue and red dots represent the measured values for the boundary admittance and set-default relay methods, respectively. The phase (A, B, C) and ground true values versus the measured values are shown in Figure 9a, 9b, 9c and 9d, respectively.

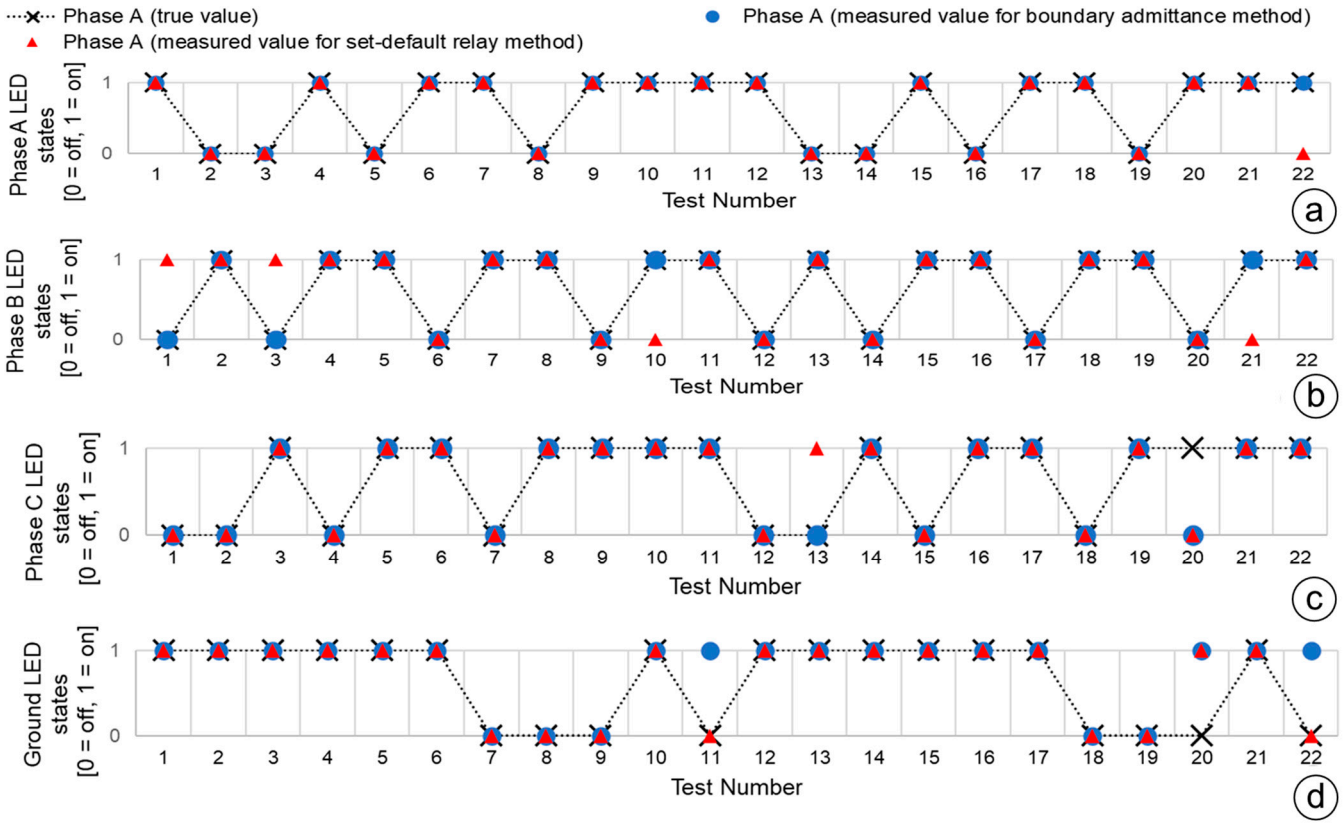

Figure 9. Phases A (**a**), B (**b**), and C (**c**) and ground (**d**) true values versus measured values.

The accuracy of each test result shows how close a measured value is to the true value based on percentage accuracy calculation; therefore, the percentage accuracy can be defined as the ratio of the difference between the true and measured value to the true value [39]. The percentage accuracy of the phase (A, B, C) and ground LED states for the boundary admittance method and the set-default relay method can be calculated with Equations (10) and (11), respectively.

$$Accuracy\%\ BAM_{\ LEDn} = 100 - \left[\frac{TV_{LEDn} - MV\ BAM_{\ LEDn}}{TV_{LEDn}} \times 100\right], \quad (10)$$

where $Accuracy\%\ BAM_{\ LEDn}$ is the percentage accuracy of the boundary admittance method for the phase and ground LEDs, TV_{LEDn} is the number of true values for the phase and ground LEDs, $MV\ BAM_{\ LEDn}$ is the number of measured values matching with the true values of the boundary admittance method for the phase and ground LEDs, and n^{th} is the phase (A, B, C) and ground LEDs.

$$Accuracy\%\ SDRM_{LEDn} = 100 - \left[\frac{TV_{LEDn} - MV\ SDRM_{LEDn}}{TV_{LEDn}} \times 100\right], \quad (11)$$

where $Accuracy\%\ SDRM_{LEDn}$ is the percentage accuracy of the set-default relay method for the phase and ground LEDs, TV_{LEDn} is the number of true values for the phase and ground

LEDs, $MV\ SDRM_{LEDn}$ is the number of measured values matching with the true values of the set-default relay method for the phase and ground LEDs, and n^{th} is the phase (A, B, C) and ground LEDs.

Based on Figure 9a,d, the number of measured values matching the true values for the boundary admittance method and the set-default relay method in the phase (A, B, C) and ground states are shown in Table 4. The percentage accuracy of the boundary admittance method and the set-default relay method for the phase and ground LEDs states was calculated with Equations (10) and (11), respectively, using the results from Table 4. Figure 10 shows the percentage accuracy of the phase (A, B, C) and ground states for the boundary admittance method and the set-default relay method.

Table 4. True and measured phase and ground states for the electrical fault tests.

LEDs (Phase/Ground)	A	B	C	GND
Figures	**Figure 9a**	**Figure 9b**	**Figure 9c**	**Figure 9d**
TV $_{LEDn}$: Number of true values for the boundary admittance and set-default relay methods at the phase and ground LEDs	22	22	22	22
MV BAM $_{LEDn}$: Number of measured values matching true values for the boundary admittance method at the phase and ground LEDs	22	22	21	19
MV SDRM $_{LEDn}$: Number of measured values matching true values for the set-default relay method at the phase and ground LEDs	21	18	20	21

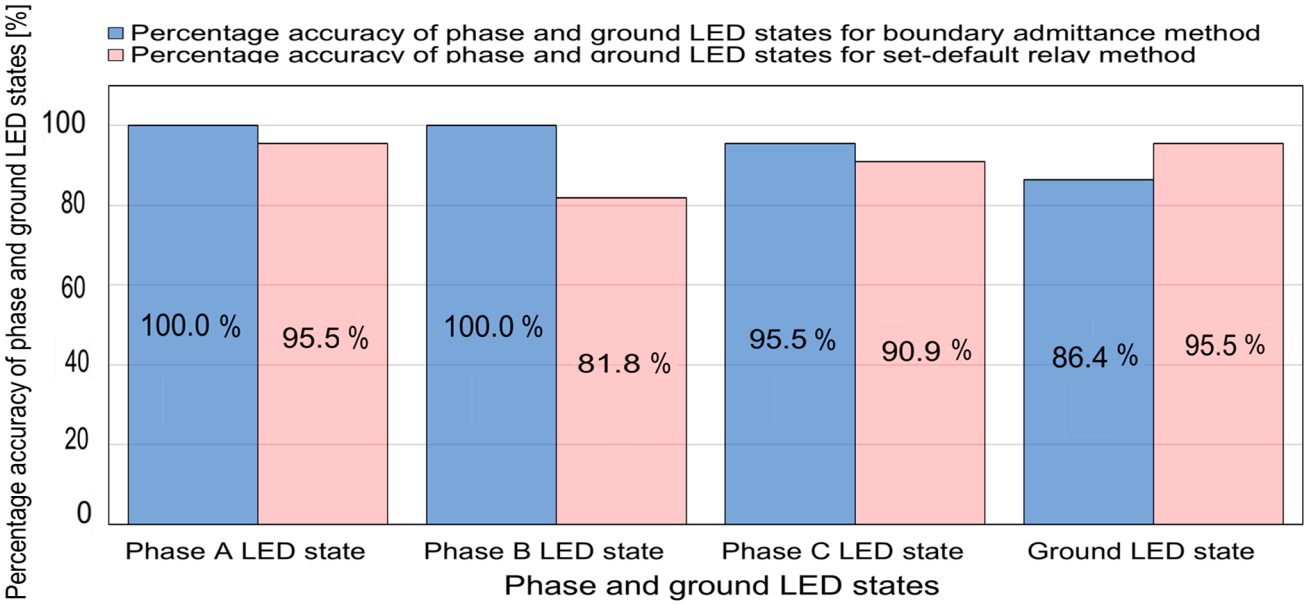

Figure 10. Percentage accuracy of the phase (A, B, C) and ground states for the boundary admittance method and the set-default relay method.

4.3. Analysis of the Measured Electrical Fault Types

The measured and true electrical fault type states presented in Table 3 allowed us to build Table 5. The number of electrical fault types for which the measured values matched the true values with the boundary admittance method and the set-default relay method is shown in Table 5.

LG: line-to-ground; LLG: line-to-line ground; LL: line-to-line; 3L/3LG: three-line/three-line-to-ground.

From Table 5, the percentage accuracy of the boundary admittance method and the set-default relay method for the electrical fault types could be computed with Equations (12) and (13), respectively.

$$Accuracy\%\ EFT_{BAMm} = 100 - \left[\frac{TV_{EFTm} - MV\ BAM_{EFTm}}{TV_{EFTm}} \times 100\right]. \quad (12)$$

where $Accuracy\%\ EFT_{BAMm}$ is the percentage accuracy of the electrical fault types with the boundary admittance method, TV_{EFTm} is the number of true electrical fault type values, $MV\ BAM_{EFTm}$ is the number of measured electrical fault type values matching the true electrical fault type values for the boundary admittance method, and m^{th} is the electrical fault type.

$$Accuracy\%\ EFT_{SDRMm} = 100 - \left[\frac{TV_{EFTm} - MV\ SDRM_{EFTm}}{TV_{EFTm}} \times 100\right]. \quad (13)$$

where $Accuracy\%\ EFTs_{DRMm}$ is the percentage accuracy of the electrical fault types for the set-default relay method, TV_{EFTm} is the number of true electrical fault type values, $MV\ SDRM_{EFTm}$ is the number of measured electrical fault type values matching the true electrical fault type values for the set-default relay method, and m^{th} is the electrical fault type.

Table 5. True and measured values for the types of electrical fault tests (from Table 3).

	Electrical Fault Types			
	LG	**LLG**	**LL**	**3L/3LG**
TV_{EFTm}: Number of true electrical fault type values	6	6	6	4
$MV\ BAM_{EFTm}$: Number of measured electrical fault type values matching true electrical fault type values for the boundary admittance method	6	6	6	2
$MV\ SDRM_{EFTm}$: Number of measured electrical fault type values matching the true electrical fault type values for the set-default relay method	3	6	6	1

Figure 11 shows the percentage accuracy of the types of electrical faults using the boundary admittance method and the set-default relay method, which was calculated using Table 5 and Equations (12) and (13).

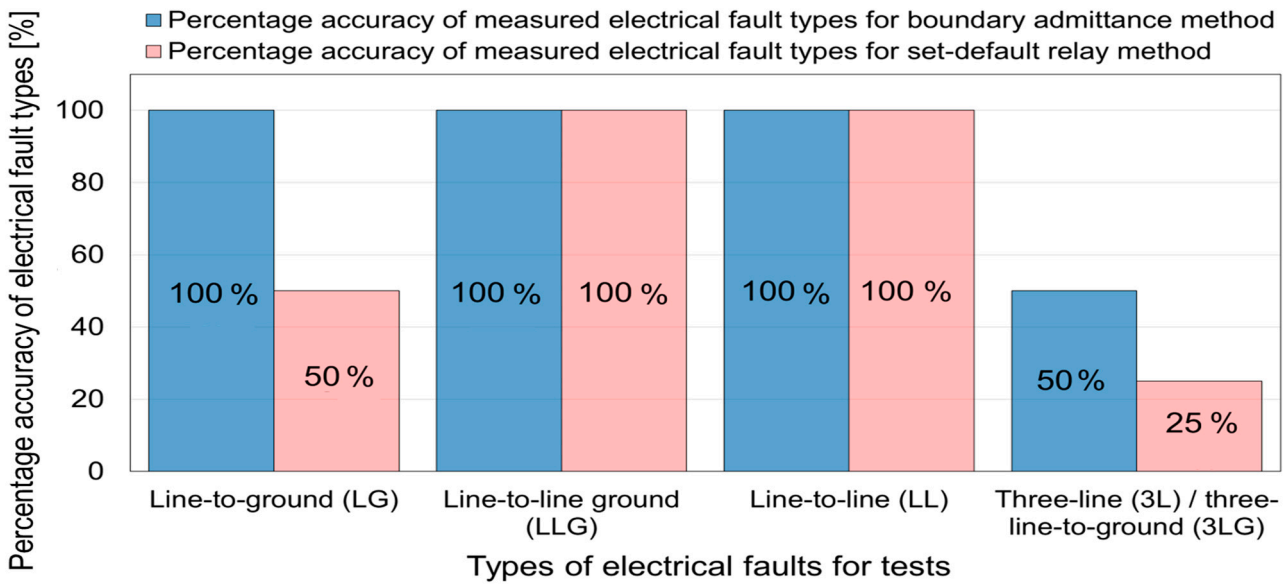

Figure 11. Percentage accuracy of electrical fault types for the boundary admittance method and the set-default relay method.

5. Discussion

The relay misoperation analysis was based on comparing the boundary admittance method with the set-default relay method using the ASTDGT testbed. In Figure 10, the phase and ground LED states of the relays were measured satisfactorily for electrical fault types near to and far from the breaker site. The boundary admittance method performed well in the detection of the phase (A, B, C) and ground target LEDs (blue bars in Figure 10). In Figure 11, the percentage accuracy of the electrical fault types for the boundary admittance method and the set-default relay method is plotted, and the boundary admittance method (blue bars in Figure 11) had a percentage accuracy of 100% for the detection of SLG, LLG, and LL electrical faults. For ABCG and ABC electrical fault tests (10, 11, 21, 22) in Table 3, the boundary admittance method always identified an ABCG electrical fault; here, the percentage accuracy was 50%. However, the set-default relay method identified one ABC electrical fault, so the percentage accuracy was 25%, as is shown in Figure 11 for 3L/3LG electrical faults.

The boundary admittance method used an external algorithm that was run with an RTS with a relay in the loop. This external algorithm is defined by the phase and ground boundaries (Equations (5) and (6)), which are estimated by collecting the sequence impedances of the power line sections and then calculating the total admittance (Y_T), and the total zero sequence admittance (Y_{T0}) for the electrical grid circuit. The set-default relay method does not need to calculate the pre-setting values, and it can be implemented at any location in the electrical grid (feeders, power transformers, power lines, generators, etc.). The set-default relay method is only based on the A, B, and C phase and ground target LED settings with internal relay logic.

Based on a literature review, using the sequence method [10] to identify faulted phases with the target LEDs in relays had the same performance for AG/BCG, CG/ABG, and BG/CAG faults [10]. However, the boundary admittance method did not differentiate between ABC and ABCG faults. But LG and LLG faults are usually more frequent than 3LG faults in power grids. Based on Figure 11, the boundary admittance method is expected to perform better than the sequence method [10] and the set-default relay method assessed in this study. Also, the sequence method [10] has the advantage of not requiring additional settings, as opposed to the boundary admittance method, which requires the sequence impedance of the power line sections.

It is common practice for electrical engineers to record and plot events after an electrical fault to observe the incident in detail because relays sometimes cannot immediately identify electrical fault types with their light indicators. However, an accurate and fast visual report of electrical fault types from target LEDs could lead to a quick decision after a fault situation in implementing a pre-setting electrical fault type detection method with an external algorithm, like the presented boundary admittance method.

The ASTDGT testbed showed the relay control inputs to be a good interface for integrating an external relay algorithm (like the boundary admittance) run with an RTS because practically no delay time was observed in the signals. These external algorithms for advanced protection functions could be applied with an RTS using time steps of 50 us to implement a fast calculation process in control grid operations. Also, the relays' analog signals from the low-voltage level interface could easily be connected with tee connectors from the relays to an RTS to implement external relay algorithms using the relays' current and voltage scaling factors and the relays be wired to the RTS [40]. If the relay's current and voltage scaling factors are not available in the relay manual, they could be estimated using an interface method to find low-voltage interfaces [41].

Power system protection engineers frequently use commercial relay test systems [36–38] to commission possible relay misoperations caused by incorrect and/or out-of-date relay settings. These commercial relay test systems usually test one relay in the loop, and they are enabled by a three-phase current/voltage power source that feeds the relay's analog signals. The relay test systems generate the pre-fault, fault, and post-fault states with breaker pole state sequences and trip/close signals to assess the relay settings and programmed logic

(algorithms) during electrical fault tests. In this study, an ASTDGT testbed with an RTS and paired relays was presented (Figure 3). It was based on a synchronized time digital grid twin testbed to compare the boundary admittance method (external algorithm) with the set-default relay method (internal algorithm). The novelties of the ASTDGT testbed are as follows:

- *Main novelty:* The ASTDGT testbed method was created to evaluate external relay algorithms because no specific standards are available for testing external relay algorithms; therefore, the ASTDGT testbed's main contribution was focused on comparing the test results for the boundary admittance method (external algorithm) to those for the set-default relay method (internal algorithm) to assess an external relay algorithm for detecting electrical fault types.
- *A platform with complex grids and high sampling frequencies:* The ASTDGT testbed (Figure 3) has a digital grid twin circuit (Figure 6) created with an RTS and a time step of 50 us (sampling frequency of 20 kHz). The digital grid twin circuit is formed of breakers, power line sections, capacitor banks, and source models from MATLAB/Simulink (Figure 6), offering a realistic simulation approach for electrical fault scenarios and relays with high sampling frequencies greater than 3 kHz. Thus, the ASTDGT testbed presents a better simulation approach than commercial relay test systems [36–38], which are formed with one three-phase voltage/current source that cannot implement complex electrical grids and has a frequency limitation of 3 kHz [42].
- *A digital grid twin to commission relays with synchronized time stamps:* The ASTDGT testbed (Figure 3) can commission internal and external relay algorithms at the same time with multiple relays. In this case, two identical relays were used to evaluate the set-default relay method (internal algorithm) and the boundary admittance method (external algorithm) using a digital grid twin circuit (Figure 6) and a synchronized time source system (Figure 3) to evaluate the event behavior for both relays with the same time stamps.
- *The application of time domain external relay algorithms:* The ASTDGT implements the boundary admittance algorithm (Figure 3c), formed of an external relay algorithm (Figure 7) in an RTS. The implementation of this external relay algorithm using an RTS could be a great tool for integration with relays in the field in the future, considering RTSs are based on a time domain process with a time step of 50 us, which could speed the relay's decisions up in some critical situations, such as the operation of breakers for inverter-based DERs.

6. Conclusions

The ASTDGT testbed assessed relay misoperations based on using an internal and external relay algorithm. The ASTDGT testbed with paired relays evaluated two different electrical fault detection algorithms with a synchronized time source, and the event behavior for both relays was analyzed and plotted. The boundary admittance method (external algorithm) presented good performance using the relay's control inputs, with observation of the electrical fault types based on the relay's front side light indicators and involving no delay time in the application of the external algorithm with the RTS.

The boundary admittance method (external algorithm) and the set-default (internal algorithm) relay method were assessed for detecting electrical fault types near to and far away from the relay's breaker location. The electrical fault tests were performed with the ASTDGT testbed, and the boundary admittance method was 100% accurate in the detection of LG, LL, and LLG electrical faults. Also, the application of the time domain process (time step of 50 us) in the boundary admittance (external algorithm) method with the RTS and the relay in the loop had a good time response in detecting the electrical fault types.

In the future, the ASTDGT testbed will be upgraded with high-sampling-frequency relays and meters integrated with external algorithms using advanced protection schemes for inverter-based DERs.

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