



Article Basic Circuit Model of Voltage Source Converters: Methodology and Modeling

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Abstract: Voltage source converters (VSCs) have emerged as the key components in modern power systems, facilitating efficient energy conversion and flexible power flow control. Understanding the fundamental circuit model of VSCs is essential for their accurate modeling and analysis in power system studies. A basic voltage source converter circuit model connected to an LC filter is essential because it lowers the harmonic distortions and enhances the overall power quality of the micro-grid. This guarantees a clean and steady power supply, which is necessary for the integration of multiple renewable energy sources and sensitive loads. A comprehensive methodology for developing a basic circuit model of VSCs, focusing on the key components and principals involved, is presented in this paper. The methodology includes the modeling of space vector pulse-width modulation (SVPWM) as well as the direct quadrature zero synchronous reference frame. Different design controls, including the design of current control loop in the S-domain, the design of the direct current (DC) bus voltage control loop in the S-domain, and the design of the alternating current (AC) voltage control loop in the S-domain, are explored to capture the dynamic behavior and control strategies of VSCs accurately. The proposed methodology provides a systematic framework for modeling VSCs, enabling engineers and researchers to analyze their performance and assess their impact on power system stability and operation. Future studies can be conducted by using case studies and simulation scenarios to show the efficiency and applicability of the developed models in analyzing VSC-based power electronics applications, including high-voltage direct current (HVDC) transmission systems and flexible alternating current transmission systems (FACTS). The significance of this work lies in its potential to advance the understanding and application of VSCs, contributing to more resilient and efficient power systems. By providing a solid foundation for future research and development, this study supports the ongoing integration of renewable energy sources and the advancement of modern electrical infrastructure.

Keywords: voltage source converter; LC filter; current control; DC voltage control; AC voltage control

1. Introduction

Voltage source converters (VSCs) have become integral components in modern power systems, playing a crucial role in facilitating efficient energy conversion and enabling flexible power flow control [1]. As the demands for renewable energy integration, grid stabilization, and improved grid reliability continue to grow, the accurate modeling and analysis of VSCs have become paramount [2,3]. The primary power interface connecting distributed generations (DGs) to micro-grids is the AC-DC converter. The voltage source converter functions in two distinct modes, operating as an active rectifier for direct current (DC) bus control and, as depicted in Figure 1, acting as an inverter during grid-feeding and grid-forming operations using distinct control loops [4]. Understanding the basic circuit model of VSCs, along with methodologies for their control and modeling, is essential for engineers and researchers to effectively design, analyze, and optimize VSC-based power electronics applications [5]. The aim of this paper is to present a comprehensive



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Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). methodology overview, control strategies, and modeling techniques associated with the basic circuit model of VSCs. This paper delves into the fundamental principles underlying the operation of VSCs, focusing on the key components and their interactions within the circuit. An emphasis is placed on elucidating different methodologies, such as space vector pulse-width modulation (SVPWM), the direct quadrature zero synchronous reference frame, and their integration into VSC circuits.

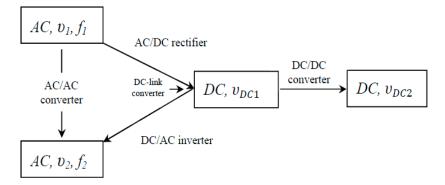


Figure 1. Solid-state power converter groups based on their operating transformation [6].

A fundamental voltage source converter circuit model connected to the LC filter is crucial because it helps in reducing harmonic distortions and improving the overall power quality in the micro-grid. This ensures a stable and clean power supply, which is essential for sensitive loads and the integration of various renewable energy sources. It also plays a key role in converting DC power from renewable sources like solar panels or batteries to AC power, which is required for most loads and for synchronization with the main grid. The LC filter aids in smoothing out the output, making the conversion process more efficient. Understanding the VSC circuit model and its interaction with the LC filter is essential for designing systems that can seamlessly integrate with the main grid or operate in island mode. This ensures that the micro-grid can handle fluctuations in supply and demand without compromising stability. In essence, the significance of introducing the fundamental VSC circuit model connected to the LC filter lies in its ability to address key challenges in energy conversion, stability, integration, and the management of hybrid renewable micro-grid systems.

Furthermore, this paper explores various control strategies employed in VSCs to regulate the voltage, current, and power flow in both grid-connected and standalone applications. Various control techniques using pulse width modulation (PWM) and proportional integral (PI) control are discussed. Moreover, the modeling aspects of the design and control of VSCs are also introduced to develop accurate and dynamic models that capture the transient and steady-state behavior of these devices. To ensure the relevance and applicability of the presented models in real-world scenarios, practical considerations, such as parameter estimation, validation, and implementation challenges, need to be addressed. Case studies and simulations are recommended to be conducted to shown the efficiency and accuracy of the presented methodologies and control strategies in analyzing VSC-based power electronics applications, such as flexible alternating current transmission systems (FACTS), grid-connected renewable energy systems, and high-voltage direct current (HVDC) transmission systems.

The following sections describe the remaining paper parts: In Section 2, two-level grid-connected VSC modeling with an LC filter is presented. The design of the current control loop in the S-domain is introduced in Section 3. Section 4 presents the design of a DC bus voltage control loop in the S-domain. In Section 5, the design of an AC voltage control loop in the S-domain is provided. Section 6 gives a brief discussion, and Section 7 concludes the paper.

2. Two-Level Grid-Connected VSC Modeling with LC Filter

A typical circuit model of a two-level inverter with an LC filter connected to a threephase load is presented in Figure 2. The signal applied to terminals *a*, *à*, *b*, *b*, *c*, and *è* regulates the power of the six switches that form the output, denoted as S1 to S6. It is assumed that switches S1 through S6 are complementary [7]. Typically, a voltage source converter with an LCL filter is regulated by a conventional linear controller augmented by a damping loop to ensure the stability of the system [8]. Furthermore, both the threephase AC system and the DC-side voltage source can directly receive power from the VSC. Consequently, there are two different modes of operation for the VSC, either the inverter (DC/AC) or rectifier (AC/DC) modes.

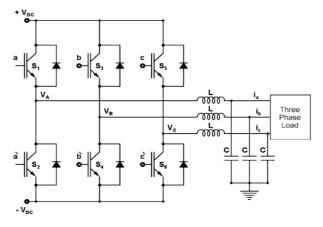


Figure 2. Voltage source converter with three phase-2 levels [7].

To connect the distributed generation systems to the grid, three-phase pulse-width modulation voltage source converters (PWM-VSCs) are commonly employed because of their superior controllability and higher efficiency compared to the other converters [9]. To enable DC-side voltage control and power factor at the point of common coupling (PCC), a two-level PWM-VSC topology is used. However, the implementation of the PWM results in baseband and sideband harmonics appearing in the AC voltage harmonic spectrum, necessitating the use of filters to reduce the harmonics of the grid current [10].

2.1. Space Vector Pulse-Width Modulation (SVPWM) Methodology

Using the triangle comparison strategy simplifies the execution of this procedure. Compared to triangle comparison PWM, it achieves a 15% increase in AC voltage and reduces voltage and current total harmonic distortion (THD). A standard space vector diagram of a two-level voltage source inverter (VSI) with switching states in the six sectors is presented in Figure 3 [11]. Table 1 illustrates that a typical three-phase, two-level voltage source inverter has eight switching states, with six active states producing voltage vectors of either $+V_{dc}$ or $-V_{dc}$, and two null states generating voltage vectors with zero amplitude. In Figure 3, the switch states 000 and 111 represent the null states, while the space vector plane is divided into six equal sectors by the active states. This methodology employs a revolving reference vector, as depicted in Figure 3, sampled once during each sub-cycle, T_s [12]. The main objective is to estimate the vector of the reference voltage V_{ref} utilizing eight switching models.

Figure 3 illustrates that two of the potential output voltage vectors (V_1 and V_7) are null or zero vectors, represented by equal values in all three phases (000 or 111). The remaining six vectors ($\vec{V}_1, ..., \vec{V}_6$) are non-zero and are all spatially separated by 60°.

The null voltage vector time was arbitrary assumed to be divided equally between t_0 and t_7 for the SVPWM approach, meaning that $T_0 = T_7$.

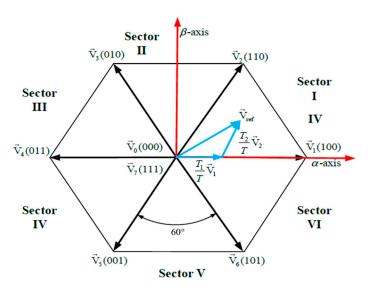


Figure 3. A typical SVPWM diagram for a voltage source inverter with two levels.

Voltage Vectors –	Switching Vectors			Line-to-Neutral Voltage			Line-to-Line Voltage		
	S_1	<i>S</i> ₂	S ₃	Van	V _{bn}	V _{cn}	V _{ab}	V_{bc}	Vca
$\overrightarrow{m{V}}_0$	0	0	0	0	0	0	0	0	0
$\overrightarrow{m{V}}_1$	1	0	0	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	V _{DC}	0	$-V_{DC}$
\overrightarrow{V}_2	1	1	0	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	0	V _{DC}	$-V_{DC}$
\overrightarrow{V}_3	0	1	0	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-V_{DC}$	V _{DC}	0
$\stackrel{ ightarrow}{V}_4$	0	1	1	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-V_{DC}$	0	V _{DC}
$\overrightarrow{m{V}}_5$	0	0	1	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	0	$-V_{DC}$	V_{DC}
\overrightarrow{V}_6	1	0	1	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	V _{DC}	$-V_{DC}$	0
$\overrightarrow{V_7}$	1	1	1	0	0	0	0	0	0

The following is used to calculate the sampling interval:

 $T_s = T_0 + T_1 + T_2 \tag{1}$

or

with

 $T_{mod} = T_1 + T_2 \tag{3}$

where T_{mod} is the modulation time; T_0 , $T_{1,}$ and T_2 are the time intervals; and T_s is the sampling interval. When examining the first sector, the reference voltage vector \vec{V}_{ref} may be presented as function vectors:

 $T_S = T_0 + T_{mod}$

$$\vec{V}_{ref} = \frac{T_1}{T_S}\vec{V}_1 + \frac{T_2}{T_S}\vec{V}_2 \tag{4}$$

$$\left| \overrightarrow{V}_{ref} \right| \begin{bmatrix} \cos \alpha \\ \sin \alpha \end{bmatrix} = \frac{T_1}{T_S} \left| \overrightarrow{V}_1 \right| \begin{bmatrix} \cos \left(0 \right) \\ \sin \left(0 \right) \end{bmatrix} + \frac{T_2}{T_S} \left| \overrightarrow{V}_2 \right| \begin{bmatrix} \cos \left(\pi/3 \right) \\ \sin \left(\pi/3 \right) \end{bmatrix}$$
(5)

(2)

Equation (5) can be divided into two parts and expressed as follows:

$$T_{S} \left| \overrightarrow{V}_{ref} \right| \cos \alpha = T_{1} \left| \overrightarrow{V}_{1} \right| \cos(0) + T_{2} \left| \overrightarrow{V}_{2} \right| \cos(\pi/3)$$
(6)

$$T_{S} \left| \vec{V}_{ref} \right| \sin \alpha = T_{1} \left| \vec{V}_{1} \right| \sin(0) + T_{2} \left| \vec{V}_{2} \right| \sin(\pi/3)$$
(7)

The sample interval equations are obtained by solving for T_2 using Equation (7), and then substituting the results in Equation (6).

$$T_1 = mT_s \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \tag{8}$$

$$T_2 = mT_s \frac{\sin\left(\alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \tag{9}$$

$$T_0 = T_S - T_1 - T_2 \tag{10}$$

The modulation index, $m = \frac{V_{ref}}{V_{dc}}$, is represented as $0 \le \alpha \le 60^\circ$, and T_S is the halfperiod for switching carriers. The following formulas represent the dwell periods for each sector:

$$T_1 = mT_S \sin\left(\frac{n\pi}{3} - \alpha\right) \tag{11}$$

$$T_2 = mT_s \sin\left(\alpha - \frac{\pi(n-1)}{3}\right) \tag{12}$$

Figure 4 shows the SVPWM output switching sequence in the first sector.

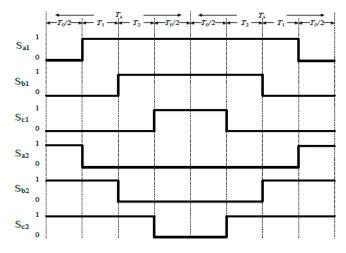


Figure 4. Output switching sequence at the first sector.

The switching periods for the upper and lower switches for each sector are summarized in Table 2 [13].

 Table 2. Switching time calculation for every sector.

Sectors	Upper Switches (S ₁ ,S ₃ ,S ₅)	Lower Switches (S ₄ , S ₆ ,S ₂)
Sector 1	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_0/2 S_6 = T_1 + T_0/2 S_2 = T_1 + T_2 + T_0/2$
Sector 2	$S_1 = T_1 + T_0/2$ $S_3 = T_1 + T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_2 + T_0/2$ $S_6 = T_0/2$ $S_2 = T_1 + T_2 + T_0/2$

Sectors	Upper Switches (S ₁ ,S ₃ ,S ₅)	Lower Switches (S ₄ , S ₆ ,S ₂)
Sector 3	$S_1 = T_0/2 S_3 = T_1 + T_2 + T_0/2 S_5 = T_2 + T_0/2$	$S_4 = T_1 + T_2 + T_0/2$ $S_6 = T_0/2$ $S_2 = T_1 + T_0/2$
Sector 4	$S_1 = T_0/2$ $S_3 = T_1 + T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1 + T_2 + T_0/2$ $S_6 = T_2 + T_0/2$ $S_2 = T_0/2$
Sector 5	$S_1 = T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1 + T_0/2$ $S_6 = T_1 + T_2 + T_0/2$ $S_2 = T_0/2$
Sector 6	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_0/2$	$S_4 = T_0/2 S_6 = T_1 + T_2 + T_0/2 S_2 = T_2 + T_0/2$

Table 2. Cont.

2.2. Direct Quadrature Zero Synchronous Reference Frame Methodology

The Direct Quadrature Zero (DQZ) synchronous reference frame methodology is a control technique widely used in power electronics, particularly in VSIs, to achieve the precise and efficient control of three-phase AC systems [14]. This methodology is widely applied in grid-connected renewable energy systems (such as wind and solar inverters), adjustable speed drives for motors, active power filters for harmonic mitigation, and other applications requiring the precise control of the AC voltage and the current waveform [15]. The DQZ synchronous reference frame methodology involves transforming the three-phase AC signals (typically voltages or currents) into a rotating reference frame aligned with the AC frequency of the system. This transformation simplifies the control of the VSIs by decoupling the components of interest (such as active power, reactive power, and harmonic components) from each other.

The three-phase AC signals are transformed from the time domain (a, b, c reference frame) to the rotating DQZ reference frame using Clarke and Park transformations [16]. Park transformation rotates the $\alpha\beta$ components to a stationary DQZ reference frame (d, q, 0), where d and q components represent the direct and quadrature components of the signals, respectively, and 0 represents the zero sequence component [17]. Clarke transformation converts three-phase quantities (a, b, c) into two-phase quantities (α , β), representing the symmetrical components of the AC signals. In the DQZ reference frame, control strategies such as proportional integral (PI) controllers or more advanced algorithms are applied to regulate the d and q components of the reference signals. These controllers adjust the switching patterns of the VSI's semiconductor devices typically insulated gate bipolar transistors (IGBTs) to generate the desired AC output voltage waveform, ensuring the precise control of the voltage magnitude, frequency, and waveform quality [18]. Figure 5 shows a space phasor with the $\alpha\beta0$ reference frame.

The revised three-phase current values (i_a , i_b , i_c) are shown in Figure 5 as projections onto the new reference axis (i_{α} , i_{β}). When a three-phase, three-wire system is balanced and the zero axis represents the common mode component, the total phase current is nullified. Thus, the variables α and β can fully characterize a system defined in the ABC reference frame.

The output variables ABC are described in Equation (13) below:

$$i_a = I_M \cos(\omega t); \ i_b = I_M \cos\left(\omega t - \frac{2\pi}{3}\right); \ i_c = I_M \cos\left(\omega t + \frac{2\pi}{3}\right)$$
 (13)

where *t* is the amount of time needed to reach steady state and ω is the constant synchronous frequency. Equation (14) expresses the $\alpha\beta0$ transformation in complex form, while Equation (15) expresses it in matrix form.

$$\vec{I}_{s} = i_{\alpha} + ji_{\beta} = \frac{2}{3} \left(i_{a} + i_{b}e^{\frac{j2\pi}{3}} + i_{c}e^{\frac{-j2\pi}{3}} \right)$$
(14)

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \\ i_{0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix}$$
(15)

The reference axis currents are i_{α} , i_{β} , and i_0 , while the three-phase currents are i_{α} , i_b , and i_c .

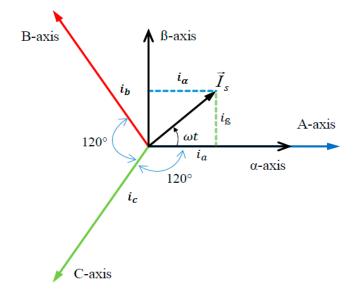


Figure 5. Space phasor and $\alpha\beta$ 0 reference frame.

Using Park transformation with a -90° shift, the frame rotates around the 0 axis at the same frequency as the sinusoids defining the phasors, while the system is in the $\alpha\beta0$ frame. As it can be seen in Figure 6, the component is transformed to Q axis, which is positioned 90° at a quadrature angle to the direct component, and the $-\beta$ component is transformed to the *d*-axis, which is in line with the rotating vector.

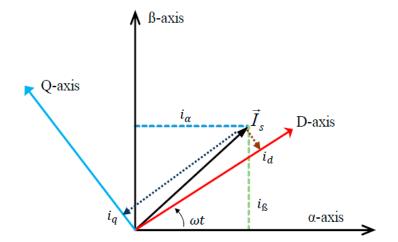


Figure 6. Space phasor and DQ0 reference frame.

Equations (16) and (17) express the DQ0 transformation in complex and matrix representations, respectively.

$$\vec{I}_s = i_d + ji_q = (i_\alpha + ji_\beta)e^{-j(\omega t - \frac{\pi}{2})}$$
(16)

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) & 0 \\ \cos(\omega t) & \sin(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix}$$
(17)

Consequently, the rotation generates DC values from the periodic signals. Since the spinning frame trails the a-axis by 90 degrees, at t = 0, the Q- and A-axes coincide. When I_s is precisely aligned with the reference angle ωt , $i_d = 1$, $i_q = 0$, and $i_0 = 0$ are the DQ0 components. The full transformations from DQ0 to ABC and their corresponding inverses are presented as follow:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$
(18)

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & 1 \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}$$
(19)

3. Design of the Control Loop for the Current in the S-Domain

The current control loop design in the S-domain for a three-phase two-level VSI is a crucial aspect of ensuring the precise and stable operation of the inverter. This design methodology leverages the classical control theory in the S-domain to achieve the effective regulation of the output currents of the inverter. According to Wencong et al., this control loop modifies the output voltage of the inverter to allow the injection of the necessary current in the utility grid [19]. The three-phase VSI is typically modeled using a set of differential equations that describe the relationship between the input DC voltage, the switching states of the inverter, and the output AC currents. These equations are transformed into the synchronous reference frame (dq-frame) to decouple the three-phase AC currents into two orthogonal components (*d*-axis and *q*-axis), simplifying the control design. The system dynamics are represented by transfer functions in the S-domain, which relate the control inputs (reference voltages) to the outputs (actual currents). For a VSI, the transfer function typically includes the LC filter dynamics of the inverter and the influence of the load impedance. Figure 7 illustrates the schematic representation of a three-phase, two-level VSC with an L filter. R_f and L_f represent the resistance and the inductance, respectively, between the converter switches and the PCC.

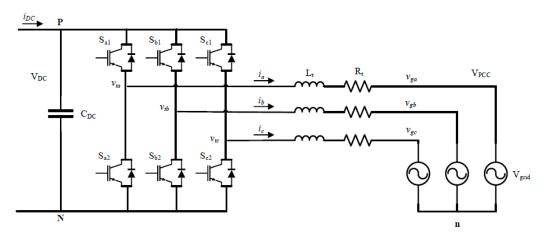


Figure 7. A two-level VSC circuit diagram with an L filter included.

A reduced equivalent per-phase circuit can be produced by applying the voltage law of Kirchhoff to the circuit shown above, as illustrated in Figure 8.

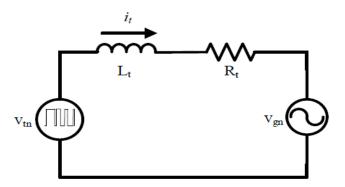


Figure 8. An L filter in a simplified VSC per-phase circuit.

The grid voltage, v_{gn} , is shown in Figure 8 as a relatively fixed component that may be considered disruptive. As a result, the current, i_{tn} , can be regulated by altering the output voltage of the inverter v_{tn} . Consequently, the VSC functions as an energy source that feeds electricity into the grid. The voltage law of Kirchhoff, when applied to the three circuits per phase, yields the following:

$$v_{tan} = L_f \frac{di_a}{dt} + R_f i_a + v_{gan}$$

$$v_{tbn} = L_f \frac{di_b}{dt} + R_f i_b + v_{gbn}$$

$$v_{tcn} = L_f \frac{di_c}{dt} + R_f i_c + v_{gcn}$$
(20)

The variables v_{tan} , v_{tbn} , and v_{tcn} represent the three per-phase inverter output voltages; L_f and R_f denote the inductance and resistance between the converter switches and the point of common coupling (PCC); v_{gan} , v_{gbn} , and v_{gcn} stand for the three per-phase grid voltages; and i_a , i_b , and i_c represent the three per-phase inverter currents. By consolidating all three equations from (20) into a single equation, we obtain the following:

$$v_{t,abc} = L_f \frac{di_{abc}}{dt} + R_f i_{abc} + v_{g,abc}$$
⁽²¹⁾

Equation (15) is used to translate Equation (21) into the reference frame $\alpha\beta 0$, which results in

$$v_{t,\alpha\beta} = L_f \frac{a_{\alpha\beta}}{dt} + R_f i_{\alpha\beta} + v_{g,\alpha\beta}$$
(22)

Using the reference frame dq0 in (16) and repeating the process for Equation (22), the result is $-i(\omega t - \frac{\pi}{2})$

$$v_{t,dq} = v_{t,\alpha\beta} e^{-j(\omega t - \frac{\gamma}{2})}$$

$$v_{t,dq} L_f \frac{di_{dq}}{dt} + R_f i_{dq} + v_{g,dq}$$
(23)

The *a*, *b*, *c* frame can be split into the two components, *d* and *q*, as was indicated in Section 2.1.

$$L_f \frac{dt_d}{dt} = v_{td} + L_f \omega i_q - R_f i_d - v_{gd}$$
⁽²⁴⁾

$$L_f \frac{di_q}{dt} = v_{tq} + L_f \omega i_q - R_f i_q - v_{gq}$$
⁽²⁵⁾

with $v_{td} = \frac{V_{DC}}{\sqrt{3}}m_d$ and $v_{tq} = \frac{V_{DC}}{\sqrt{3}}m_q$, where m_{dq} is the index of modulation, and $\frac{V_{DC}}{\sqrt{3}}$ is the SVPWM gain converter.

The i_d and i_q dynamics are related because of the $L_f \omega$ term found in Equations (24) and (25). To decouple the *d* and *q* subsystems and account for the grid disruption inputs v_{gd} and v_{gq} , the index of modulation for each must be stated as follows:

$$m_d = \frac{\sqrt{3}}{V_{DC}} \left(u_d - L_f \omega i_q + v_{gd} \right) \tag{26}$$

$$n_q = \frac{\sqrt{3}}{V_{DC}} \left(u_q - L_f \omega i_d + v_{gq} \right) \tag{27}$$

For the *d* subsystem, the anticipatory term is $-L_f \omega i_q + v_{gd}$, while for the *q* subsystem, it is $-L_f \omega i_d + v_{gq}$. Equation (26) can be substituted into (24), yielding

$$L_f \frac{di_d}{dt} = u_d - R_f i_d \tag{28}$$

Equation (27) can be substituted into (25) in the same way to obtain

1

$$L_f \frac{du_q}{dt} = u_q - R_f i_q \tag{29}$$

with u_q as the output of PI compensator.

The control systems of the current control loops are the same in the d and q axes, as seen in (28) and (29). Therefore, the linked compensators can be the same. As a result, only the current control compensator gains in the d-axis will be determined. When Equation (29) is transformed using the Laplace method, the following results are obtained:

$$L_f s I_d(s) = u_d(s) - R_f I_d(s)$$

$$I_d(s) = \frac{u_d(s)}{L_f + R_f}$$
(30)

The control plant can therefore be expressed as follows:

$$G_P(s) = \frac{1}{L_f s + R_f} \tag{31}$$

The following Equation (32) indicates that the compensator is a PI controller:

$$G_c(s) = \frac{k_p s + k_i}{s} \tag{32}$$

Figure 9 illustrates the transfer function of the closed loop in the *d*-axis:

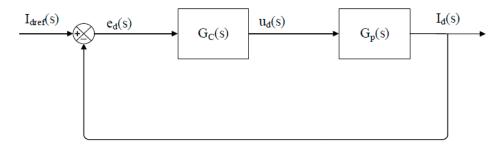


Figure 9. Current-controlled VSC system block diagram in simplified form.

Equation (33) gives the following open loop gain:

$$G_{ol}(s) = G_C(s)G_P(s) \tag{33}$$

By replacing the compensator and control plant Equations by their terms, Equation (33), will be: $(k) = k^{k}$

$$G_{ol}(s) = \frac{k_p s + k_i}{s} \times \frac{1}{L_f s + R_f} = \frac{k_p s + k_i}{L_f s^2 + R_f s} = \left(\frac{k_p}{L_f s}\right) \frac{s + \frac{\kappa_i}{k_p}}{s + \frac{R_f}{L_f}}$$
(34)

Once the terms $\frac{k_i}{k_p} = \frac{R_f}{L_f}$ are equalized by applying the pole cancelation approach, the open-loop gain Equation (34) is reduced from the second to the first order transfer function as follows:

$$G_{ol}(s) = \frac{k_p}{L_f s} \tag{35}$$

Equation (36) represents the current control gain in the closed loop in the *d*-axis:

$$G_{i}(s) = G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)}$$
(36)

Equation (35) can be substituted into (36) to obtain the following expression for the closed-look gain:

$$\frac{I_d(s)}{I_{dref}(s)} = G_i(s) = \frac{k_p}{k_p + L_f s}$$
(37)

By replacing $k_p = \frac{L_f}{\tau_i}$ and $k_i = \frac{R_f}{\tau_i}$, the closed-look gain will become

$$G_i(s) = \frac{1}{\tau_i s + 1} \tag{38}$$

The resultant closed-loop control constant time is written as τ_i . Therefore, the following formula provides the first-order settling time in the closed-loop system:

$$t_{i, settling} = 4.6\tau_i \tag{39}$$

4. Design of the Control Loop for the DC Bus Voltage in the S-Domain

For maintaining balanced power flow, the DC bus voltage control technique is essential. Implementing this control is imperative as it enables the voltage source converter to function as a rectifier, converting AC power to DC power and facilitating control of the DC link capacitor voltage to supply an output load. Moreover, for intermittent DC power sources such as PV systems, this control technique assists in adjusting the current control loop reference to regulate the input of DC power effectively [20]. The circuit from Figure 7 is shown in Figure 10, with a bleeding resistor R_B and extra feedback signals (i_{DC} and i_L) added to simplify DC control modeling.

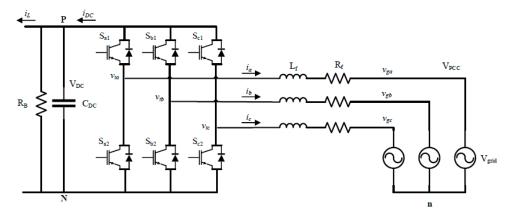


Figure 10. Two-level VSC with an L filter and a DC link circuit bleed resistor.

The resistance and inductance between the PCC and the inverter output are R_f and L_f . The fact that the active power transfer enables to charge and discharge the DC link capacitor, the circuit shown in the DQ synchronous reference frame configuration can only be modeled for the *d*-axis component. As a result, an instantaneous reactive current is not needed, neither the *q*-axis component for this procedure, as Figure 11 shows.

The following equations illustrate the voltage dynamic equation of the DC link capacitor:

$$i_{DC} = i_{bus} + i_{RB} + i_L$$

$$i_{bus} = i_{DC} - i_{RB} - i_L$$

$$C_{DC} \frac{dv_{DC}}{dt} = i_{DC} - \frac{v_{DC}}{R_B} - i_L$$
(40)

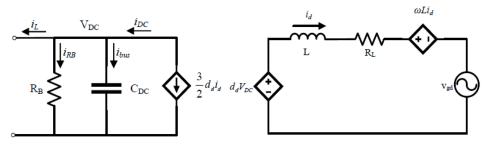


Figure 11. VSC *d*-axis component configuration with a bleed resistor and a L filter.

Equation (40) can be transformed using the Laplace transform to obtain

$$\begin{bmatrix} sC_{DC} + \frac{1}{R_B} \end{bmatrix} V_{DC}(s) = I_{DC}(S) - I_L(s)$$

$$V_{DC}(s) = \frac{1}{\left[sC_{DC} + \frac{1}{R_B} \right]} u_d(s) = \frac{R_B}{sC_{DC}R_B + 1} u_d(s)$$
(41)

The formula for calculating the PI compensator output, $u_d(s)$, is $u_d(s) = I_{DC}(s) - I_{DC}(s)$ $I_L(s)$, where $I_L(s)$ is the feedback term. This allows for the controller to avoid making up a measured value. Considering this, the control system is written as follows:

$$G_P = \frac{R_B}{sC_{DC}R_B + 1} \tag{42}$$

The relationship between these currents is represented as follows, assuming a converter without losses and the fact that the i_{DC} can only be directly controlled by the current pulled from the grid: P_3

$$\varphi = P_{DC} \tag{43}$$

The active power is given as

$$P_{3\varnothing} = \frac{3}{2} \left(v_{gd} i_d + v_{gq} i_q \right) \tag{44}$$

The DC bus power is obtained by replacing Equation (44) with (43), which yields the following:

$$\frac{3}{2}v_{gd}i_d = -i_{DC}V_{DC}$$
 (45)

The following Equation describes the relationship between the time constant τ_{DC} of the control loop for the DC bus voltage and the time constant τ_i of the current control loop:

 τ_i

$$\ll \tau_{DC}$$
 (46)

The relationship between these two control loops may be expressed by the following Equation (47) if the condition in Equation (46) is satisfied, $i_d = I_{dref}$, and the two control loops are decoupled.

$$I_{dref} = -\frac{2}{3} \frac{V_{DC}}{v_{gd}} I_{DC} \tag{47}$$

The inner gain coefficient is obtained from the relationship between I_{dref} and I_{DC} and is stated as follows:

$$K_{inner} = \frac{I_{DC}}{I_{dref}} = -\frac{3}{2} \frac{v_{gd}}{V_{DC}}$$

$$\tag{48}$$

Based on the following, it is presumed that the compensator is a PI controller expressed as

$$G_C(s) = \frac{k_p s + k_i}{s} \tag{49}$$

The selected method for DC voltage control adopts a cascade approach, including an outer loop for the voltage control of the DC bus and an inner loop for the current control. This tactic guarantees that the time reaction of current controller is faster than that for

the controller of the DC voltage in accordance with Equation (46). The DC voltage loop considers the current loop as a constant gain, which permits a gradual shift in the current reference, and hence an error-free response from the current controller. Consequently, the dynamics of the two circuits depicted in Figure 11 are effectively disconnected. Figure 12 shows a DC link voltage loop block diagram of a VSC system in a simplified form.

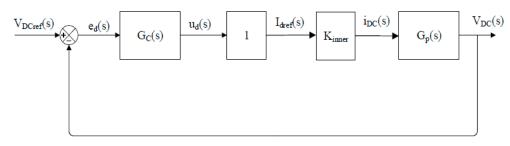


Figure 12. Simplified DC link voltage loop model of the VSC system.

Equation (50) provides the gain in the open loop based on Figure 12.

$$G_{ol}(s) = G_C(S)G_P(S)K_{inner}$$
⁽⁵⁰⁾

Equations (42) and (49) can be substituted into (50) to obtain the following:

$$G_{ol}(s) = \frac{k_p s + k_i}{s} \times \frac{R_B}{sC_{DC}R_B + 1} \times K_{inner} = \frac{K_{inner}R_B(k_p s + k_i)}{s^2 C_{DC}R_B + s}$$
(51)

With respect to the current control in *d*-axis, the closed loop gain is expressed in Equation (52):

$$G_{DC}(S) = G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)}$$
(52)

Equation (51) substituted into (52) will result in

$$G_{DC}(s) = \frac{K_{inner}(k_p s + k_i) / C_{DC}}{S^2 + \left(\frac{K_{inner}R_B k_p + 1}{C_{DC}R_B}\right)s + \frac{K_{inner}k_i}{C_{DC}}}$$
(53)

Seeing that the Equation (53) has a first-order numerator, a pre-filter will be established to eliminate this term, enabling the alignment of (53) with the standard second-order transfer function, which is:

$$G_{PF}(s) = \frac{G_{DC, desired}(s)}{G_{DC, old}(s)} = \frac{k_i}{\left(k_p s + k_i\right)}$$
(54)

The gain in closed loop of the current control in *d*-axis can be obtained by multiplying Equations (53) and (54). The result is as follows:

$$G_{DC}(s) = \frac{\frac{K_{inner}k_i}{C_{DC}}}{s^2 + \left(\frac{K_{inner}R_Bk_p + 1}{C_{DC}R_B}\right)S + \frac{K_{inner}k_i}{C_{DC}}}$$
(55)

The gain in closed loop of the current control in *d*-axis can be obtained by multiplying Equations (53) and (54). The result is as follows:

$$k_p = \frac{2\xi\omega_n C_{DC}R_B - 1}{K_{inner}R_B}$$
(56)

$$k_i = \frac{\omega_n^2 C_{DC}}{K_{inner}}$$
(57)

Thus, the following is the second closed-loop system settling time:

$$\tau_{DC} = \frac{1}{\zeta \omega_n}$$

$$t_{DC,setting} = 4.6 \times \tau_{DC}$$
 (58)

5. Design of the Control Loop for the AC Voltage in the S-Domain

When a fault or power outage prevents the main grid from supplying power, a VSC system in grid-forming mode creates a grid reference and makes it easier to transfer active or reactive powers during micro-grid operation in isolated mode. This enables the micro-grid to continue operating [21]. The three-phase VSI is modeled using differential equations that describe the relationship between the input DC voltage, the switching states of the inverter, and the output AC voltages. The dynamics of the VSI system, including the LC filter (which is typically used to smooth the inverter output), as presented in Figure 13, are represented in the S-domain by transfer functions [22].

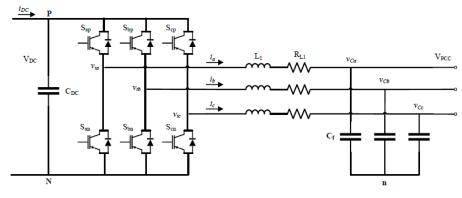


Figure 13. Two level VSC with an LC filter.

The resistances between the converter and the filter capacitor are presented as R_{L1} and L_1 . A condensed per-phase equivalent circuit produced by using the voltage law of Kirchhoff is shown in Figure 14.

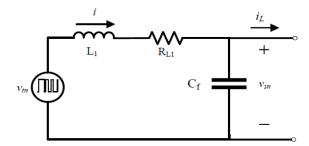


Figure 14. A VSC with an LC filter per-phase circuit in a simplified.

The phase currents for each of the three per-phase circuits can be obtained by using the current law of Kirchhoff as follows:

$$i_a = i_{Cfa} + i_{La}$$

$$i_b = i_{Cfb} + i_{Lb}$$

$$i_c = i_{Cfc} + i_{Lc}$$
(59)

Combining the three equations from (59) results in the following:

$$i_{abc} = i_{Cf,abc} + i_{L,abc} \tag{60}$$

Using the ABC- $\alpha\beta$ 0 transform on Equation (60), the following result is obtained:

$$i_{Cf,\alpha\beta} = i_{\alpha\beta} + i_{L,\alpha\beta} \tag{61}$$

Using Equation (16), the $\alpha\beta$ 0-*dq*0 transform can be converted to

$$i_{Cf,dg} = i_{Cf,\alpha\beta} e^{-j(\omega t - \frac{\pi}{2})} \tag{62}$$

$$i_{C,dq} = i_{dq} - i_{L,dq} \tag{63}$$

Consequently, as described in Section 2.1, the a, b, c frame reference may be divided into d and q components and cascaded via the current control loops in d and q axes, resulting in

$$C_f \frac{dv_{sd}}{dt} = C_f \omega v_{sq} + i_d - i_{Ld} \tag{64}$$

$$C_f \frac{dv_{sq}}{dt} = -C_f \omega v_{sd} + i_q - i_{Lq} \tag{65}$$

The existence of the $C_f \omega$ terms in Equations (64) and (65) causes the v_{sd} and v_{sq} dynamics to be coupled. The feedforward terms $\left(-C_f \omega v_{sq} + i_{Ld}\right)$ for the *d*-axis component and $\left(C_f \omega v_{sd} + i_{Lq}\right)$ for the *q*-axis component are introduced in order to decouple them and account for the load disturbance inputs i_{Ld} and i_{Lq} . Furthermore, the control units of the *d*-axis and *q*-axis components are the same, as shown in Equations (64) and (65); thus,

$$\frac{dV_{sd}}{dt} = \frac{1}{C_f} [u_d] \tag{66}$$

 u_d is the PI compensator output. Equation (66) is solved by applying the Laplace transform, which yields the following:

$$V_{sd}(s) = \frac{u_d(s)}{sC_f} \tag{67}$$

As a result, the following is the control plant:

$$G_P(s) = \frac{1}{sC_f} \tag{68}$$

Furthermore, it is presumed that the control loop time constant of the AC voltage, τ_v , will be five times greater than that of the current control loop, τ_i . If this assumption is met, the two control loops will be decoupled. The circumstance is as follows:

$$\ll \tau_v$$
 (69)

Therefore, the inputs of the current control loops are presented in Equations (70) and (71), and $I_{dq}(s) = I_{dqref}(s)$ for the control loop of AC voltage.

 τ_i

$$I_{dref}(s) = u_d(s) - C_f \omega V_{sq}(s) + I_{Ld}(s)$$

$$\tag{70}$$

$$I_{qref}(s) = u_q(s) + C_f \omega V_{sd}(s) + I_{Lq}(s)$$
(71)

Equation (72) gives the PI controller gain.

$$G_C(s) = \frac{k_p s + k_i}{s} \tag{72}$$

Since the control plants of Equation (68) for the d and q components are the same, the corresponding compensators may also be the same. With reference to Figure 15, the only information that needs to be collected next is the gains of the voltage control compensators in d-axis. The following is the open loop gain:

$$G_{ol}(s) = G_C(s)G_P(s) \tag{73}$$

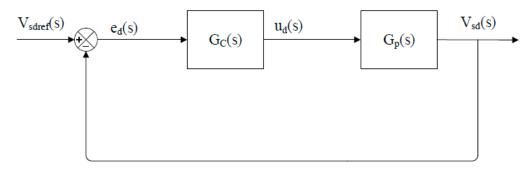


Figure 15. A block diagram for the VSC system AC voltage loop in a simplified form.

 $G_C(s)$ and $G_P(s)$ can be substituted with their corresponding values to obtain the following result:

$$G_{ol}(s) = \frac{k_p s + k_i}{s} \times \frac{1}{sC_f} = \frac{k_p s + k_i}{s^2 C_f}$$
(74)

The gain of the current control in *d*-axis in closed loop can be represented as follows:

$$G_{v}(s) = G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)}$$
(75)

When Equation (74) is substituted into (75), this results in

$$G_v(s) = \frac{\frac{(k_p s + k_i)}{C_f}}{s^2 + \left(\frac{k_p}{C_f}\right)s + \frac{k_i}{C_f}}$$
(76)

The VSC system AC voltage loop block diagram in a simplified form is shown in Figure 15.

Given that the first-order numerator of Equation (76) must be cancelled, a pre-filter needs to be developed in order to allow for Equation (76) to correspond to the conventional transfer function of the second order. As stated below, a pre-filter is required.

$$G_{PF}(s) = \frac{G_{DC, desired}(s)}{G_{DC, old}(s)} = \frac{k_i}{k_p s + k_i}$$
(77)

The following is the result of multiplying Equations (76) and (77):

$$G_v(s) = \frac{k_i}{s^2 C_f + k_p s + k_i} \tag{78}$$

By resolving the results of the denominator coefficients of Equation (78), the gains of the proportional and integral controllers are solved for

$$k_p = 2\xi \omega_n C_f \tag{79}$$

$$k_i = \omega_n^2 C_f \tag{80}$$

As a result, the control loop time constant of the AC voltage is provided as

$$\tau_v = \frac{1}{\xi \omega_n} \tag{81}$$

To decouple the two control loops, the system settling time for this second order in the closed loop is considered to be five times longer than the existing control loop settling time. In other words,

$$t_{v,settling} = \frac{4.6}{\xi\omega_n} = 4.6 \times 5 \times \tau_i = 5 \times t_{i,settling}$$
(82)

6. Discussion

This Discussion section explores the key aspects of the basic circuit model of VSCs. The different methodologies and control strategies employed in VSCs, including the SVPWM methodology, the DQZ synchronous reference frame methodology, the design of the current, the DC bus voltage, and the AC voltage control loops in the S-domain, are presented in Table 3.

Table 3. Summary of the basic circuit model of voltage source converters.

SVPWM methodology	SVPWM is a widely used technique for controlling VSCs because it can produce excellent output waveforms with less harmonic distortion. By effectively synthesizing the desired output voltage vector, SVPWM enables the precise control of the VSC output. However, challenges, such as computational complexity and switching frequency constraints, need to be carefully addressed to ensure an optimal performance.			
DQZ synchronous reference frame methodology	The DQ0 synchronous reference frame methodology provides a powerful tool for analyzing and controlling VSCs, particularly in grid-connected applications. By transforming the three-phase system into a two-dimensional space with direct (<i>d</i>) and quadrature (<i>q</i>) axes, this methodology simplifies the control and modeling processes. It allows for the accurate representation of the system dynamics and facilitates the design of control algorithms, enhancing the overall performance and stability of VSC-based systems.			
Design of the control loop for the current in the S-domain	Effective current control is crucial for ensuring accurate and dynamic response in VSCs, especially in applications requiring the precise regulation of current flow. By designing current control loops in the S-domain, engineers can leverage advanced control techniques to achieve desired performance objectives, such as fast response, low overshoot, and robust stability. Implementing sophisticated control algorithms, such as proportional integral controllers or model predictive control (MPC), can further improve the current control loops efficiency in VSCs.			
Design of the control loop for the DC Bus voltage in the S-domain	The control loop for DC bus voltage plays a critical role in maintaining stable operation and ensuring reliable performance of VSCs. By regulating the DC bus voltage, this control loop enables efficient energy conversion and smooth power transfer between the VSC and the grid or load. Designing the DC bus voltage control loop in the S-domain allows for the precise tuning of controller parameters and dynamic response characteristics, ensuring optimal performance under varying operating conditions and load profiles.			
Design of the control loop for the AC voltage in the S-domain	In grid-connected VSC applications, the control loop for the AC voltage is essential for regulating the output voltage to meet grid requirements, such as voltage magnitude and frequency. By designing the control loop for the AC voltage in the S-domain, engineers can develop robust control strategies to maintain grid stability, mitigate voltage harmonics, and ensure the seamless integration of renewable energy sources. Advanced control techniques, such as predictive control and adaptive control, can be employed to enhance the AC voltage control loop efficiency and flexibility in VSCs.			

7. Conclusions

The basic VSC circuit model with an output LC filter has been presented in this paper. The main power interface between distributed generators and the micro-grid is the AC-DC converter. Two forms of operation for a voltage source converter have been observed. It acts as an active rectifier when utilized as a DC bus control. It uses a variety of control loops to operate as an inverter when in the grid-feeding and grid-forming modes. A thorough manual that covers a variety of techniques has also been introduced, including the SVPWM, the DQZ synchronous frame, and the phase lock loop. In addition, this paper serves as a comprehensive guide to understanding the basic circuit model of VSCs, methodologies for their control, and techniques for their accurate modeling. By providing insights into the fundamental principles and practical considerations associated with VSCs, this paper aims to contribute to the advancement of VSC-based power electronics applications and their integration into modern power systems for enhanced efficiency,

reliability, and sustainability. Case studies and simulations need to be conducted to illustrate the efficacy and accuracy of the presented methodologies and control strategies in analyzing VSC-based power electronics applications.

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