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Review

Slew-Rate Enhancement Techniques for Switched-Capacitors Fast-Settling Amplifiers: A Review

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Abstract: This review is aimed at the integrated circuit design community and it explores slew-rate enhancement techniques for switched-capacitor amplifiers, with a primary focus on optimizing settling time within power constraints. Key challenges are addressed, including the selection between single-stage and two-stage amplifiers, along with the utilization of advanced circuit-level techniques for slew-rate enhancement. Presently, there exists a gap in comprehensive discussion, with reliance primarily on two Figures of Merit aimed at assessing power efficiency under specific capacitive loads. However, these metrics fail to adequately assess the performance of the existing slew-rate enhancer solutions at different values of capacitive loads. As a consequence, the designer lacks clear guidelines in practical situations. This review provides a state-of-the art mapping under a figure of merit dedicated to assess the whole settling delay, and also introduces a novel performance metric which highlights the role of the circuital architectures, regardless of external operating conditions. By offering a thorough examination, this review seeks to steer future research in switched-capacitor amplifier design, thereby facilitating informed decision-making and fostering innovation in the field.

Keywords: slew-rate enhancement; settling; switched-capacitors; operational transconductance amplifier; figure of merit

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1. Introduction

The Switched-Capacitor (SC) technique has gained widespread attention since the late 1970s [1] to implement fundamental analog functions in integrated circuits. Its enduring popularity is rooted in the precise frequency responses and gain accuracy it offers when implementing analog filters. As of today, SC circuits are regularly employed into various domains beyond traditional analog filtering applications. For example, we find plenty of literature regarding SC design of sample-and-hold circuits, track-and-hold [2], analog-to-digital (ADC), and digital-to-analog (DAC) converters, with special emphasis on Delta-Sigma modulators (ΔΣMs) [3,4] and sensor interfaces [5].

Important factors that catalyzed the adoption of SC techniques are their optimal match with low-cost CMOS technology:

1. High-linearity capacitors, ranging from few tens of femto-farads to hundreds of pico-farads, can be reliably realized in CMOS technologies, either as metal-insulator-metal (MIM) or metal-oxide-metal (MOM) structures.
2. Versatile switches are realized with MOS transistors.
3. The amplifiers involved in the SC circuits are loaded capacitively, hence simple Operational Transconductance Amplifier (OTA) structures are employed with respect to general-purpose Operational Amplifier (OpAmp) circuits.
4. MOS devices at the input of the amplifiers do not draw DC bias currents, and hence charge transfer is precisely controlled over a wide range of clock frequencies.
5. In contrast to traditional time-continuous operation, the SC approach offers discrete-time signal processing. The impact of non-linearity effects on the precision of the

system is minimal, considering that system precision is evaluated at the end of discrete time phases, during which the amplifier output should be able to settle. The settling performance is often evaluated at the end of each phase, in terms of relative error with respect to an ideal response, determined by a capacitance ratio. Conversely, in continuous-time systems, non-linearity effects must be minimized throughout the entire transient duration. This distinction is crucial in making design choices for SC circuits, where non-linear circuit schemes are often adopted.

Despite the mentioned advantages, the design of SC circuits comes with various challenges:

1. Maximize both the DC-gain and unity-gain bandwidth (UGB) of the OTA to meet specific precision specifications [6,7].
2. Reduce charge injections resulting from transitions in the control signals that command the switches [8].
3. Minimize noise introduced during signal processing in the charge domain [9]. At the same time, maximize the maximum input signal to improve the signal-to-distortion and noise ratio of the system.
4. Settling speed is often traded with power consumption: numerous advanced circuital techniques have been proposed in the literature to obtain more beneficial balance.

Extensive studies on the first two challenges exist in numerous scientific works including the already cited references, and for brevity, they will not be addressed further. This review focuses on the latter two challenges. The objective of this review is to provide an initial tool for navigating the intricate landscape of optimizing the settling time of amplifiers for SC circuits, offering an update until 2024. Additionally, the review critically revisits techniques introduced in recent years concerning settling time enhancement and explores the associated trade-offs with power consumption. The target audience for this review encompasses junior IC designers seeking a succinct exploration of slew-rate enhancement techniques for SC circuits. It also extends to expert professionals who may benefit from a critical discussion on this topic.

Within the myriad of circuit designs incorporating SCs and an OTA, the parasitic-insensitive integrator stands out as one of the most commonly employed. Figure 1 illustrates a standard parasitic-insensitive fully-differential SC integrator, which will serve as a standard case study for analyzing the behavior and merit parameters of various OTA topologies explored in this review. The field of application of an SC integrator is vast: it can be employed in very-low frequency applications such as in temperature smart sensors, up to baseband signal processing in communication systems, operating at hundreds of megahertz. Indeed, meeting high-speed requirements aligns with the maximum transition frequency permitted by the technology at hand: higher bandwidth corresponds to more advanced CMOS technological nodes. However, technological nodes below 20 nm introduce significant phenomena like self-heating and aging, particularly noticeable during low-voltage operation. Although these effects are not addressed in this review, it is anticipated that they will become prominent in the coming years, prompting the development of new design methodologies and circuits. The general approach outlined here, concerning the capacitor network formed by C_1, C_2, and C_3, facilitates the extension of the discussion to vastly different fields of applications. For instance, in typical ADC settings, C_3 is typically in the same order of magnitude as C_1, C_2 capacitors , whereas in Liquid Crystal Display (LCD) driver applications, $C_3 \gg C_1, C_2$.

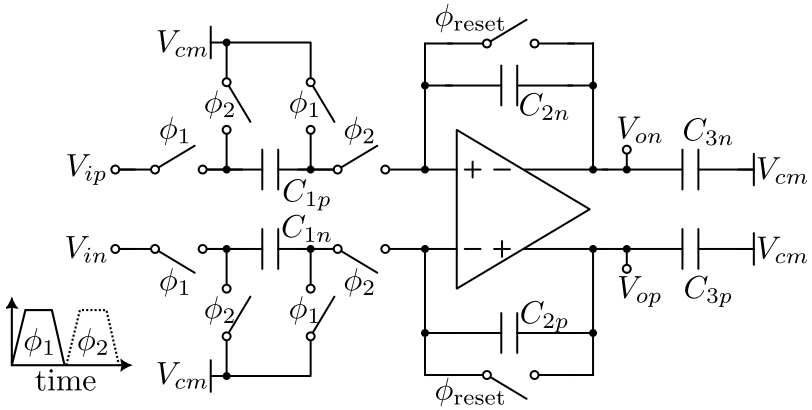

Figure 1. Schematic diagram of an inverting fully-differential SC integrator. Nominally $C_{1p} = C_{1n} = C_1$, $C_{2p} = C_{2n} = C_2$, $C_{3p} = C_{3n} = C_3$. Capacitors C_{3p} and C_{3n} represent the capacitive loads applied to the integrator. Phase ϕ_{reset} is used to establish the initial conditions of the integrator state variable. The differential input of the integrator is represented by $V_{ip} - V_{in}$, while the differential output is represented by $V_{op} - V_{on}$. For simplicity, the output and the input common mode voltages are identical and equal to V_{cm}. In this configuration, the output is valid at the end of ϕ_2.

2. Settling Time and Power Optimization

Figure 2 illustrates the settling process at the differential output of the SC integrator of Figure 1. In this plot, the integration phase, ϕ_2, starts at $t = 0$ and its duration is equal to t_S. Two scenarios are depicted:

(i) a small output voltage upset, denoted as $V_o^{(1)}(t)$;

(ii) a large output voltage upset, denoted as $V_o^{(2)}(t)$.

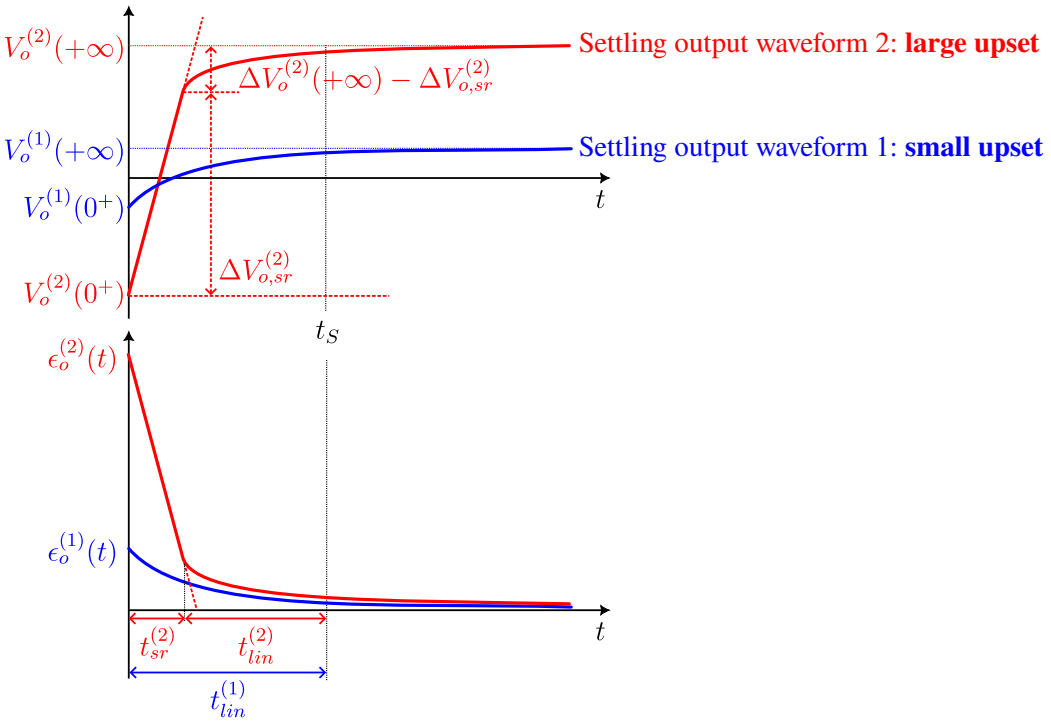

Figure 2. Chronograph of the differential output voltage $V_o(t)$ [from (3)] the relative error $\epsilon_o(t)$ [from (7)] for a small input step and for a large input.

In scenario (i), where the SC integrator experiences relatively minor variations across its nodes, the system is typically analyzed through its equivalent linearized circuit. Here, $t_{\text{lin}}^{(1)}$, coinciding with t_S, denotes the analytical approach used to determine $V_o^{(1)}(t)$.

Conversely, in scenario (ii), the transient waveform exhibits two distinct regions:

1. In the initial region, denoted by $t_{sr}^{(2)}$, the output voltage ($V_o^{(2)}(t)$) shows its maximum slope ($\frac{dV_o^{(2)}(t)}{dt}$), which in this phase is practically independent of the input signal.
2. In the subsequent region, as $V_o^{(2)}(t)$ approaches its final value $V_o^{(2)}(+\infty)$, the behavior resembles that of scenario (i).

The complex behavior observed during large output upsets stems from the maximum available current at the OTA output, denoted as I_{omax}. Throughout t_{sr}, the OTA supplies I_{omax} to the output, driving the equivalent capacitive load, C_{LE}, observed at the differential outputs of the OTA:

$$C_{LE} = C_3 + \beta_{FB} C_1; \quad \beta_{FB} = \frac{C_2}{C_1 + C_2}. \tag{1}$$

Here, β_{FB} denotes the feedback factor due to C_1 and C_2. It is noteworthy that, for $t > t_{sr}$, the slope of the output voltage is consistently smaller than the initial slope, indicating that the output current provided by the OTA is less than I_{omax}.

The values of both $V_o(0^+)$ and $V_o(+\infty)$ in Figure 2 depend on several factors: (i) on the charge present within C_2 before the onset of ϕ_2 (resulting in an output voltage of $V_o(0^-)$) and (ii) the charge sampled within C_1, equal to $C_1 V_{id}$, with $V_{id} = V_{ip} - V_{in}$, at the end of ϕ_1:

$$V_o(+\infty) = V_o(0^-) + \frac{C_1}{C_2} V_{id}; \quad V_o(0^+) = V_o(0^-) - \frac{1}{1 + C_3/(\beta_{FB} C_1)} V_{id}. \tag{2}$$

In these equations, we considered the OTA gain high enough to allow for finite-gain effects to be neglected (Finite-gain effects are not considered in this analysis. The interested reader who wants to delve into this subject can refer to essential books for SC design such as [1,5], as well as more application-specific literature: [3,4] for ADCs, [6,7,10] for SC filters) and the OTA input capacitance to be negligible with respect to C_1 [10,11] (This latter condition will be removed in the analysis developed in Section 2.1). We can observe that the asymptotic output upset, $\Delta V_o(+\infty) = V_o(+\infty) - V_o(0^+)$, is proportional to V_{id} through a coefficient that depends only on the capacitor network around the OTA:

$$\Delta V_o(+\infty) = \left(\frac{C_1}{C_2} + \frac{1}{1 + C_3/(\beta_{FB} C_1)} \right) V_{id} = k_C V_{id}, \tag{3}$$

where:

$$k_C = \frac{C_1}{C_2} + \frac{1}{1 + C_3/(\beta_{FB} C_1)}. \tag{4}$$

Ideally, the integrator output step would be dependent only on the C_1/C_2 ratio, such as the following:

$$\Delta V_o^\star(+\infty) = \frac{C_1}{C_2} V_{id}. \tag{5}$$

The relationship between the actual and the ideal step is easily found elaborating (3) and (5):

$$\Delta V_o^\star(+\infty) = \alpha_C \Delta V_o(+\infty), \quad \text{where:} \quad \alpha_C = \frac{C_1}{k_C C_2} = \frac{C_1(C_2 + C_3) + C_2 C_3}{(C_1 + C_2)(C_2 + C_3)}. \tag{6}$$

The coefficient α_C is non-zero positive and less than one. It solely describes the ratio between the ideal integrator coefficient and the actual coefficient, which is slightly larger due to the presence of C_3.

At this point, we focus on the error affecting the output voltage when a finite time interval t_S is considered. To this purpose, the output relative error $\epsilon_o(t)$ is defined as follows:

$$\epsilon_o(t) = \frac{V_o(+\infty) - V_o(t)}{\Delta V_o^\star(+\infty)} = \frac{V_o(+\infty) - V_o(t)}{\alpha_C \Delta V_o(+\infty)}, \tag{7}$$

which is schematically illustrated in Figure 2. We are interested in ϵ_S, corresponding to ϵ_o evaluated at t_S:

$$\epsilon_S = \epsilon_o(t_S) = \frac{V_o(+\infty) - V_o(t_S)}{\Delta V_o^{\star}(+\infty)} = \frac{V_o(+\infty) - V_o(t_S)}{\alpha_C \Delta V_o(+\infty)}. \tag{8}$$

Next, we consider the case of a small output upset, as in case (1) of Figure 2. If the OTA is a dominant-pole system, a single time constant, τ, is needed to closely approximate the output waveform:

$$V_o^{(1)}(t) = V_o^{(1)}(0^+)\, e^{-t/\tau} + V_o^{(1)}(+\infty)\left(1 - e^{-t/\tau}\right). \tag{9}$$

The time constant τ is related to the gain-bandwidth product of the loop gain (For one-pole systems, characterized by an open-loop pole f_p and DC gain $A_0 \gg 1$, it is well known that $\tau^{-1} = (1 + \beta_{\mathrm{FB}} A_0) f_p \approx 2\pi\beta_{\mathrm{FB}} \cdot \mathrm{GBW}$, where GBW is the gain-bandwidth product: $\mathrm{GBW} = A_0 f_p$. In Section 2.1, a design-oriented expression of τ is found for a simple single-stage OTA architecture. Very high-frequency designs ($t_S \ll 1$ ns) are often characterized by scarce adherence to dominant-pole models: in this case, specialized models need to be developed. This aspect, however, falls outside the scope of this review). The corresponding error can be calculated applying (8):

$$\epsilon_S^{(1)} = \frac{1}{\alpha_C} e^{-t_S/\tau}. \tag{10}$$

Interestingly, this result indicates that, as long as the system does not enter slew-rate conditions, the relative error remains constant and is determined only by the ratio t_S/τ. This outcome was expected since the circuit model we adopted is linear. An important consequence of this assumption is that the integrator does not introduce distortion as long as V_{id} remains small enough. By elaborating Equations (1)–(3), (9), and imposing $dV_o/dt < I_{omax}/C_{LE}$, it can be found that this condition holds as long as the following inequality is verified:

$$V_{id} < \frac{\tau I_{omax}}{k_C C_{LE}}. \tag{11}$$

The inequality (11) provides a constraint on the maximum allowable value of V_{id}, determined by the characteristics of the capacitive feedback network (k_C, C_{LE}) and the OTA (I_{omax} and τ), without entering slew-rate conditions.

In contrast, case (2) of Figure 2 is distinguished by an initial slew-rate period, $t_{sr}^{(2)}$, and the respective relative error can be expressed as (The expression can be easily found from the relation in (9) by applying a time-shift of $t_{sr}^{(2)}$. Consequently, $V_o^{(2)}(t_{sr})$ is to be substituted to $V_o^{(2)}(0^+)$. This term is easily found as $V_o^{(2)}(t_{sr}) = V_o^{(2)}(0^+) + t_{sr}^{(2)} I_{omax}/C_{LE}$):

$$\epsilon_S^{(2)} = \frac{1}{\alpha_C}\left(1 - \frac{I_{omax}}{C_{LE}} \frac{t_{sr}^{(2)}}{\Delta V_o^{(2)}(+\infty)}\right) e^{-(t_S - t_{sr}^{(2)})/\tau} = \alpha_{sr}^{(2)} \cdot e^{t_{sr}^{(2)}/\tau} \cdot \epsilon_S^{(1)}, \tag{12}$$

where:

$$\alpha_{rs}^{(2)} = 1 - \frac{I_{omax}}{C_{LE}} \frac{t_{sr}^{(2)}}{\Delta V_o^{(2)}(+\infty)} = 1 - \frac{\Delta V_{o,sr}^{(2)}}{\Delta V_o^{(2)}(+\infty)}. \tag{13}$$

In (12), two major terms need to be considered:

- The $\alpha_{rs}^{(2)}$ term reflects the residual voltage interval to be covered by the OTA after it ends the slewing phase. In this term, $I_{omax} t_{sr}^{(2)}/C_{LE}$ corresponds to the portion of the voltage upset related to the slewing phase, $\Delta V_{o,sr}^{(2)}$, also indicated in Figure 2. Intuitively, $\alpha_{sr}^{(2)}$ results in a decreasing function of V_{id}, since the residual voltage tends

to very small values as $\Delta V_o(+\infty)$ is increased. However, $\alpha_{sr}^{(2)}$ will never be zero, since a certain amount of linear settling is always due. Notably, $t_{sr}^{(2)}$ results are inversely proportional to I_{omax}, and hence $\alpha_{sr}^{(2)}$ does not depend on the design choices related to I_{omax}.

- The most important term in (12) is represented by the exponential grow determined by the t_{sr}/τ ratio, causing distortion to rapidly grow with V_{id}, regardless of the partial compensation due to the $\alpha_{sr}^{(2)}$ term.

As seen from (11), the V_{id} limit can be increased either by increasing I_{omax} or τ. The latter choice is in contrast with maximum settling time requirements. On the other hand, increasing I_{omax} only during t_{sr} represents a viable solution. Slew-rate enhancing techniques are devoted to reduce t_{sr}/τ in order to maintain acceptable distortion even in the presence of large V_{id} values. The following section delves into analytical aspects of OTAs in order to identify a power-linearity trade-off in the SC integrator.

2.1. Simplified Settling Model

Optimizing the settling time of the SC integrator depicted in Figure 1 within a predetermined power budget is a common challenge for designers. In this pursuit, designers frequently encounter constraints related to the dimensions of capacitors C_1, C_2, and C_3. These constraints stem from precision considerations in relation to the kT/C noise limit and the available supply voltage, V_{DD}. This optimization challenge has been extensively studied in the literature, with contributions from various researchers [12–18]. For clarity in the subsequent discussion, a brief overview of the elementary model proposed by these authors is presented here. To streamline the analysis, the circuit in Figure 1 is simplified to the configuration shown in Figure 3. In this simplified representation, the evolution of the integrator output, V_o, is determined by the equivalent step at the input, V_{id}. The idealized OTA model involves a few key parameters: G_m, I_{omax}, and V_{dmax}. The transconductance G_m characterizes the OTA behavior when operating for $|V_i| < V_{dmax}$. Here, V_{dmax} defines the maximum value of the input differential voltage where the OTA output currents remain sensitive to V_i. Outside this range, the maximum available current at the output is I_{omax}. Importantly, G_m is associated with the small-signal settling behavior of the OTA, while I_{omax} is related to the OTA slew-rate behavior. In an ideal scenario:

$$I_o = \begin{cases} G_m V_i & \text{for} \quad |V_i| < V_{dmax} \\ \text{sign}(V_i) \cdot I_{omax} & \text{for} \quad |V_i| \geq V_{dmax} \end{cases}. \tag{14}$$

The parameters G_m, V_{dmax}, and I_{omax} are contingent on the specific OTA topology and the corresponding design choices. The subsequent discussion will explore the relationship of these parameters with specific OTA topologies. The static supply current drawn by the OTA is denoted as I_{sup}. Any discontinuities, arising when $I_{omax} > G_m V_{dmax}$, are also incorporated into the $I_o(V_i)$ characteristics to account for the settling behavior of OTAs with highly non-linear circuits as the Parallel-type Slew Rate Enhancer (PSRE) circuits, as discussed in Section 3.6.

The analysis of the settling transient is complex due to the non-coincidence of the OTA differential voltage input, V_i, with the input step V_{id}. We assume a perfect virtual short-circuit between the OTA inputs at the steady state ($V_i = 0$). However, an instant after the step is applied, V_i jumps to the value $c_1 V_{id}$, where c_1 is a voltage divider coefficient determined by the capacitor network formed by C_1, C_2, C_3, C_P [15]:

$$V_i(0^+) = c_1 V_{id}; \quad c_1 = \frac{C_1}{C_1 + C_P + \frac{C_2 C_3}{C_2 + C_3}}. \tag{15}$$

The value of $V_i(0^+)$ establishes the starting point of the settling transient, and the OTA finds itself operating either in the linear region if $|V_i(0^+)| < V_{dmax}$ or in the slew-rate region if $|V_i(0^+)| \geq V_{dmax}$. The coefficient c_1 is close to unity in the ideal conditions of

an unloaded OTA ($C_3 = 0$) and zero input parasitic capacitance ($C_P = 0$). In practice, $0 < c_1 < 1$.

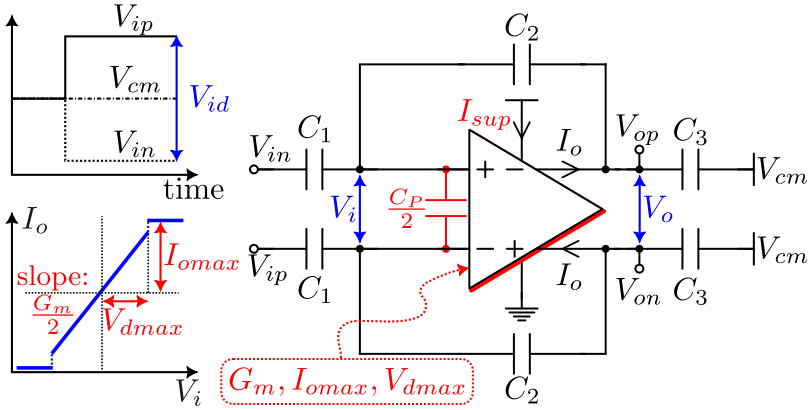

Figure 3. Schematic diagram of a fully-differential SC integrator during the settling phase. The capacitor C_P is associated to the OTA input device parasitic capacitance. The OTA has the idealized $I_o(V_i)$ characteristic shown in the inset plot. I_o represent the differential-mode current at the output of the OTA while V_i represent the differential voltage at the input of the OTA. This idealized characteristic is fully described by the set of the following three parameters: G_m, I_{omax}, V_{dmax}. I_{sup} indicates the current drawn from the supply voltage.

For a single-stage OTA, the expression of the settling time, t_{set}, given a settling precision specification, ϵ_S, can be expressed as the sum of the slew-rate period, t_{sr}, and a linear-settling period, t_{lin}:

$$t_S(V_{id}) = t_{sr} + t_{lin} = \begin{cases} t_{sr}(V_{id}) = \max\left[0, \quad \frac{c_1 C_{IE}}{I_{omax}}\left(|V_{id}| - \frac{V_{dmax}}{c_1}\right)\right] \\ t_{lin}(V_{id}) = \frac{C_{IE}}{G_m} \cdot \min\left[\ln\frac{c_1 c_2}{\epsilon_S}, \quad \ln\frac{c_1 c_2}{\epsilon_S} - \ln\frac{c_1|V_{id}|}{V_{dmax}}\right] \end{cases} \tag{16}$$

The expressions of various terms in the equation (c_1, c_2, C_{IE}) are detailed in Table 1. Clearly, the C_{IE}/G_m term represents the time-constant τ found in (9). Straightforward algebraic manipulations lead to the following:

$$\tau = \frac{1}{G_m}\left(C_1 + C_P + \frac{C_3}{\beta^\star_{\text{FB}}}\right), \quad \text{where} \quad \beta^\star_{\text{FB}} = \frac{C_2}{C_1 + C_P + C_2}. \tag{17}$$

This equation explicitly indicates the role of the feedback factor (With respect to the expression of β_{FB} found in (1), C_P has not been neglected. It is important to remark that $\beta^\star_{\text{FB}}$ and β_{FB} assume the same conceptual role, and are here distinguished only to highlight the eventual influence of C_P. In the following discussion, we will employ β_{FB}, keeping in mind that $\beta^\star_{\text{FB}}$ should be used instead in all cases where C_P cannot be neglected with respect to C_1). $\beta^\star_{FB}$ applies in determining the τ (for a single-stage OTA).

Table 1. Parameters of the simplified settling model for single-stage OTAs.

Parameter	Expression	Meaning
ϵ_S		Target settling error (%) [(8)]
C_{IE}	$(C_1 + C_P)(1 + C_3/C_2)$	Equiv. input capacitance
c_1	$[C_P(1 + C_3/C_2) + C_3]/[C_{IE} + C_3]$	Capacitive-network coeff. 1
c_2	$1 + (C_2 + C_P)/C_1$	Capacitive-network coeff. 2

The model described by Equation (16) serves as a qualitative, high-level design tool and cannot substitute transistor-level simulations. Notably, the model exhibits significant inaccuracies in both large-signal and small-signal aspects:

1. Abrupt transitions between the slew-rate and linear regions.
2. Oversimplified modeling of G_m and V_{dmax}.
3. Inability to capture the effects of non-dominant singularities associated with OTA internal nodes (The presence of non-dominant singularities is typically addressed by introducing the phase margin parameter. In an ideal one-pole system, the phase margin assumes a value of 90 degrees. In practical designs, a phase margin degradation of up to 20 degrees is often tolerable without significantly affecting settling time. This aspect is discussed in Section 2.2 when two-stage architectures are introduced).

Despite these evident shortcomings, Equation (16) remains useful for illustrating specific phenomena emerging during the settling process. This includes the dependence of t_S on input amplitude and the influence of G_m and I_{omax}.

Equation (16) clearly indicates that the slew phenomenon occurs when $|V_{id}| > V_{dmax}/c_1$. Consequently, SC integrators dealing with small input voltage steps do not derive significant benefits from the adoption of slew-rate enhancement techniques. In practical applications, this corresponds to scenarios where ΔΣ Modulators employ multi-bit quantisers or Finite Impulse Response (FIR) filters in the feedback paths [19]. More commonly, straightforward and simpler implementations with single-bit quantisers are employed. This choice implies higher values of $|V_{id}|$ to be considered. As $|V_{id}|$ starts to increase, the contribution of t_{sr} may dominate over t_{lin} in the overall transient process.

This phenomenon is illustrated in Figure 4a, where Equation (16) has been numerically evaluated for three distinct design cases, A, B, and C. The numerical values in this example mimic a sub-unit integrator coefficient ($C_1/C_2 = 0.125$), which is common in single-bit ΔΣMs. In case A, $I_{omax} = G_m V_{dmax}$, while in case B, I_{omax} is four times the value of the previous case while maintaining G_m. The comparison between A and B exemplifies the contrast between a standard OTA and an advanced OTA featuring slew-rate enhancement techniques. As will be clarified later, these techniques result in higher I_{omax} availability without ideally increasing static power consumption. Hence, in this idealized experiment, both OTAs in cases A and B have the same I_{sup}. In contrast, OTA in case C has the same standard topology as OTA A, with G_m and I_{omax} scaled by a factor of two. Consequently, OTA C doubles the power consumption of OTAs A and B.

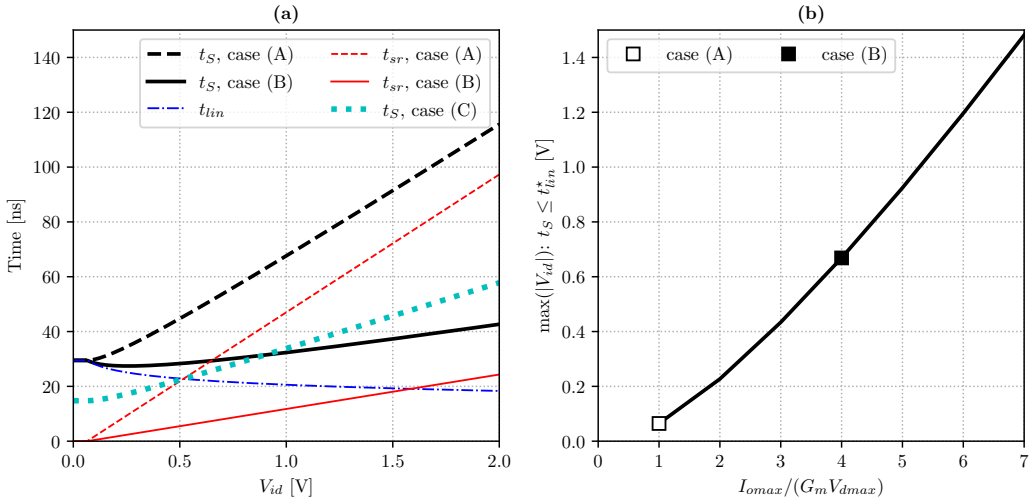

Figure 4. Numerical results for the settling-time model of Equation (16) with the following values: C_1 = 4 pF, C_2 = 32 pF, C_3 = 1 pF, C_P = 0.2 pF, ϵ_S = 100 ppm, V_{dmax} = 50 mV. Design case (A) features G_m = 1.33 mS, I_{omax} = 66.7 µA, Design case (B) features G_m = 1.33 mS, I_{omax} = 266.7 µA, Design case (C) features G_m = 2.67 mS, I_{omax} = 133.3 µA. Subplot (**a**) shows the t_S, t_{lin} and t_{sr} behavour as function of V_{id}. Subplot (**b**) shows the maximum $|V_{id}|$ for $t_S \leq t^\star_{lin}$ as a function of the slew-rate enhancing ratio $I_{omax}/(G_m V_{dmax})$, where $t^\star_{lin}$ is defined as $t^\star_{lin} = t_{lin}(V_{id} = V_{dmax})$.

As anticipated, OTA B outperforms OTA A in terms of settling time for $|V_{id}| > V_{dmax}/c_1$, effectively expanding the range of input signals where the settling is acceptable (see Figure 4b). Moreover, OTA B surpasses OTA C, especially for $|V_{id}| > 0.9$ V. Notably, this achievement is realized with a moderate slew-rate enhancement ratio, $K_{SRE} = I_{omax}/(G_m V_{dmax})$, set at 4.

As already mentioned, the model has been developed for single-stage OTAs. The most simple example of such an OTA is shown in Figure 5a. For this configuration, V_{dmax} coincides with the theoretical input differential voltage that completely imbalances the differential pair in strong inversion (M1-M2) biased at I_0. It can be derived from the EKV model equations [20], as follows:

$$V_{dmax} = \sqrt{\frac{2nI_0}{\beta_{in}}}, \quad \beta_{in} = \mu_p C_{ox} \left(\frac{W}{L}\right)_{1,2}. \tag{18}$$

Here, W/L is the aspect ratio of the input PMOS devices (M1, M2), μ_p is their mobility, and C_{ox} is the gate oxide capacitance per unit area. On the other hand, M1 and M2 are characterized also by $g_{m,in}$, producing small-signal differential currents conveyed to the output nodes through current mirrors formed by M3–M5 and M4–M6. If those mirrors have a current amplification of k_m, the resulting G_m and I_{omax} are easily found:

$$G_m = k_m g_{m,in}; \quad I_{omax} = k_m I_0. \tag{19}$$

The circuit in Figure 5b is a classical Miller-compensated two-stage OTA. Its analysis will be developed in the following section, together with considerations regarding the power efficiency of two-stage designs.

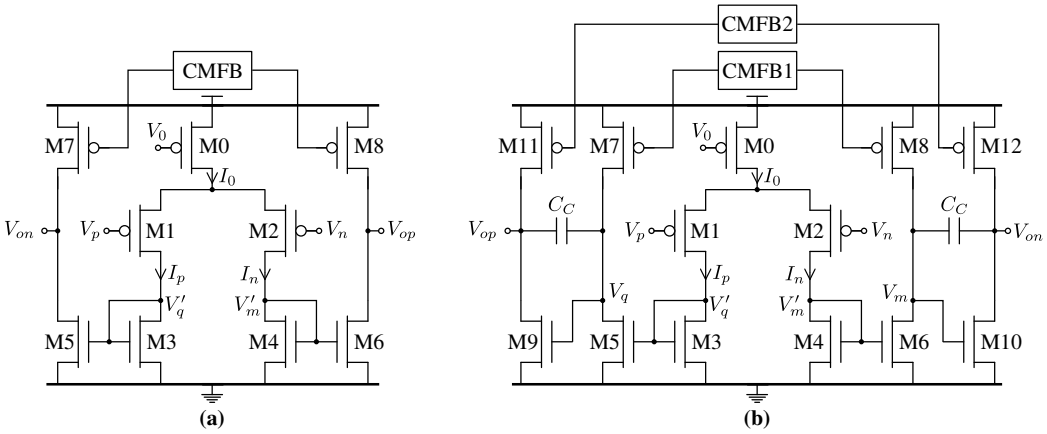

Figure 5. Schematic diagrams of (**a**), a PMOS-input mirror OTA; (**b**), a two-stage Miller-compensated PMOS-input OTA.

2.2. Considerations on Single-Stage and Two-Stage OTA Architectures

For OTAs designed to be used in place of operational amplifiers, the number of stages has a direct consequence on the maximum DC gain that can be attained, especially in the case of a resistive load or, equivalently, a resistive feedback network that has to be driven. In low voltage applications, where the voltage headroom is insufficient for cascode stages, multi-stage OTAs are a mandatory choice to maintain a sufficient DC gain even in the case of purely capacitive loads. Conversely, the effect of the number of stages on the slew-rate performance is not straightforwardly clear, and a comprehensive analysis is required to demystify some common misconceptions. In this section, we will limit the analysis to the comparison between single and two-stage OTAs, focusing on the trade-off between slew-rate and quiescent power consumption (Multi-stage architectures can be further considered based on the considerations that will be discussed for the two-stage OTAs. The interested reader may refer to dedicated works regarding the analysis of settling transients of multi-stage OTAs [17,21–24]).

To this aim, it is convenient to express the maximum output current of a single-stage OTA, I_{omax}, and its overall transconductance, G_m, as a function of the quiescent supply current, I_{sup}, by the following relationships:

$$I_{omax} = k_I I_{sup}; \quad G_m = \frac{I_{sup}}{V_{TE}}, \tag{20}$$

where k_I strongly depends on the OTA topology, while voltage V_{TE} plays the role of the inverse of the g_m/I_D parameter in single mosfets.

For a single-stage OTA, the slew rate can be simply related to the maximum output current by

$$s_r = \frac{I_{omax}}{C_{LE}} = \frac{k_I I_{sup}}{C_{LE}}. \tag{21}$$

Equation (21) suggests that the current *vs.* slew-rate trade-off can be well represented by the $s_r C_{LE}/I_{sup}$ efficiency factor. For a single-stage OTA, this factor coincides with k_I. A two-stage amplifier can be modeled by the simple single-ended circuit of Figure 6, which is representative also of differential/fully-differential architectures when only the differential mode is considered. Components in red in Figure 6 indicate the capacitive feedback network, which is equivalent to that of Figure 3. The slew rate is the minimum between the two values s_{r1} and s_{r2}, related to the input and output stage, respectively, given by

$$s_{r1} = \frac{k_{I1} I_{sup1}}{C_C}; \quad s_{r2} = \frac{k_{I2} I_{sup2}}{C_C + C_{LE}}. \tag{22}$$

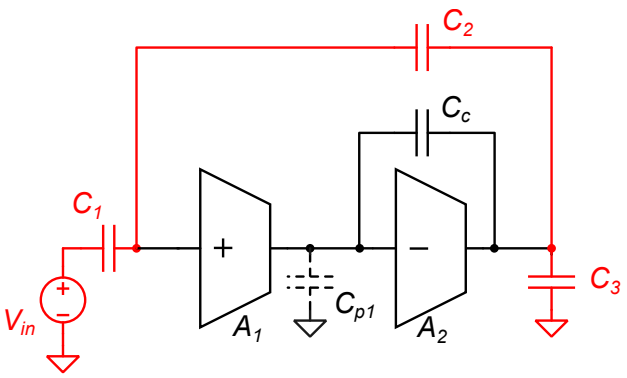

Figure 6. Simplified single-ended equivalent circuit of a two-stage amplifier with capacitive feedback.

We will focus on cases where s_{r1} is smaller or equal to s_{r2}, so that the slew rate coincides with s_{r1} (dominance of s_{r1}). From (22), the following condition on C_C can be derived:

$$C_C \geq \frac{C_{LE}}{\frac{k_{I2} I_{sup2}}{k_{I1} I_{sup1}} - 1} \tag{23}$$

The advantage of making s_{r1} dominating stands in its expression: notice that the load capacitance is not present. Properly choosing $C_C \ll C_{LE}$, it should be possible to obtain relatively large slew rates vs. supply current efficiencies even in the presence of a large load capacitance. Equation (23) suggests that a C_C value much smaller than C_{LE} can be obtained, with no penalty in terms of I_{sup2}, using a class-AB second stage, resulting in a very large k_{I2} coefficient, while the first stage is a conventional class-A configuration. Very effective class-AB output stages are based on the popular Monticelli's solution [25], but alternatives compatible with very low supply voltages are present in the literature [26,27]. In practice, stability issues prevent increasing s_{r1} without also increasing the static current absorption of the second stage, limiting the real advantage that can be obtained with small C_C values.

Well-known considerations on the open-loop frequency response impose the following:

$$\frac{G_{m2}}{C_{LE}} = k_\phi \beta_{\mathrm{FB}} \frac{G_{m1}}{C_C}, \tag{24}$$

where β_{FB} is the feedback factor previously defined in (1) while k_ϕ is a parameter that sets the phase margin. The formal definition of k_ϕ is [28]:

$$k_\phi = \frac{f_{p2}}{\mathrm{GBW}}, \tag{25}$$

where f_{p2} is the entity of the second pole while GBW is the gain-bandwidth product of the OTA. A typical choice is $k_\phi = 3$ to obtain a phase margin of nearly 70 degrees, which guarantees that no peaking is present in the frequency response when the OTA is configured as a unity-gain buffer. At the same time, the choice of $k_\phi = 3$ also corresponds to a damping factor of 0.87, which avoids overshoots in response to step-like input stimuli [29]. Although a single time-constant behavior (as in (9)) is not rigorous, it can be considered a valid first-order approximation for the remainder of the discussion of this review.

Using (20) to express G_{m1} and deriving G_{m2} from (24), it is possible to obtain a relationship between the supply currents of the first and second stages:

$$I_{sup2} = k_\phi \beta_{\mathrm{FB}} \frac{V_{TE2}}{V_{TE1}} \frac{C_{LE}}{C_C} I_{sup1}. \tag{26}$$

Finally, considering that the total current absorption of the two-stage amplifier is $I_{sup1} + I_{sup2}$ and expressing I_{sup1} as a function of s_{r1} using (22), the total current absorption I_{tot} can be calculated as a function of the slew-rate:

$$I_{tot} = \frac{s_r C_{LE}}{k_{I1}} \left(k_\phi \beta_{\mathrm{FB}} \frac{V_{TE2}}{V_{TE1}} + \frac{C_C}{C_{LE}} \right). \tag{27}$$

Note that the first factor in (27), namely $s_r C_{LE}/k_{I1}$, is the power consumption of a single-stage OTA with output current efficiency k_{I1} that directly drives the load capacitance. The terms in round brackets represent the effect of having a two-stage architecture. With the arguments exposed above and taking into account condition (23), it is possible to make the ratio C_C/C_{LE} much smaller than one. As far as the remaining term in the round brackets, to obtain a real advantage from a two-stage architecture, we need to make

$$V_{TE1} > k_\phi \beta_{\mathrm{FB}} V_{TE2} \tag{28}$$

Satisfying (28) means making the first stage widely suboptimal regarding its capability of converting the supply current into its effective transconductance. This can be detrimental when there are strict thermal noise specifications. It is worth observing that for single-stage amplifiers commonly used (used as stand-alone OTAs or to compose two-stage amplifiers), voltages V_{TE} are proportional to the overdrive voltages of the input devices (for mosfets operating in strong-inversion). Considering the constraints that apply to overdrive voltages, it is clear that in many cases of interest the factor in round brackets in (27) is close to one or even greater than one. We can conclude this analysis by stating that, taking into account constraints that frequently occur in OTA design, a two-stage architecture does not offer important advantages with respect to single-stage OTAs in terms of slew-rate *vs.* current consumption trade-off. An important exception is represented by the case of OTAs that have to be used with a very low feedback factor (i.e., with $\beta_{\mathrm{FB}} \ll 1$). This is the case, for example, of high-gain switched-capacitors amplifiers. Inspection of (27) reveals that in such cases it is possible to obtain a significant advantage (i.e., a smaller supply current) over a single-stage architecture. Unfortunately, in switched-capacitors integrators used in $\Delta\Sigma$Ms, it is much more likely to have β_{FB} factors close to one.

Clearly, class-AB solutions that were mentioned as a requirement for the second stage to make s_{r1} dominant and then validate the subsequent analysis can be used also for single-stage OTAs to boost k_I in (21) and, consequently, the efficiency.

The analysis conducted in Section 2.1 can be partially adapted to describe the settling behavior of the two-stage OTA of Figure 5b. The second stage, implemented through transistors M9, M10, M11, and M12, as well as the C_C compensation capacitors, also introduces additional degrees of freedom in the design. In the case of a dominant-pole design, relations in (16) can be adjusted as follows:

$$t_S = t_{sr} + t_{lin} = \begin{cases} t_{sr} = \max\left[0, \quad \dfrac{c_1 C_C}{I_{omax1}}\left(|V_{id}| - \dfrac{V_{dmax1}}{c_1}\right)\right] \\ t_{lin} = \dfrac{C_C}{G_{m1}} \cdot \min\left[\ln\dfrac{c_1 c_2}{\epsilon_S}, \quad \ln\dfrac{c_1 c_2}{\epsilon_S} - \ln\dfrac{c_1|V_{id}|}{V_{dmax1}}\right] \end{cases}. \tag{29}$$

Notably, the most important design parameters V_{dmax1}, G_{m1} and I_{omax1} are referred to the first stage, which is now loaded by C_C. The derivation of (29), however, neglects a number of important effects due to the non-dominant singularities. In [21], analytical aspects are fused with behavioral modeling in order to provide guidelines for rational design.

Section 3.1 is dedicated to review the most noticeable techniques used to implement differential-type Class-AB stages that are suitable to be employed both as single-stage OTAs or as the first stage in multistage OTA architectures.

2.3. Figures of Merit (FoMs)

Two commonly used Figures of Merit (FoMs) for capacitively loaded OTAs are known in the literature: *FOMS* and *FOML*. They are defined as follows:

$$FOMS = C_{LE}\frac{\text{GBW}}{P}; \quad FOML = C_{LE}\frac{s_r}{P}, \tag{30}$$

where C_{LE}, the gain-bandwidth product GBW and the slew rate s_r are confronted against $P = V_{DD} \cdot I_{sup}$ which represents the total static power consumption of the OTA. *FOMS* primarily describes the small-signal power efficiency, whereas *FOML* primarily characterizes the large-signal power efficiency. In simpler terms, *FOMS* and *FOML* aim to gauge the efficiency of achieving a specific gain-bandwidth product and slew rate, respectively, within defined power and load capacitance constraints. However, these FoMs have limitations as they separately address either small-signal or large-signal transients. In reality, both types of transients influence the settling time, as elaborated in Section 2.

A straightforward classification of the state-of-the-art, based solely on *FOMS* and *FOML*, would result in the tabular output as shown in Table 2 (Reference pool: [15,26,30–84]). This approach, however, is overly simplistic and does not ensure that a solution optimal for a specific loading condition or maximum input step maintains the same power efficiency (either in terms of small signal or large signal) to meet varying requirements.

A more contextualized comparison is offered when different loading conditions are distinguished: in this regard the state-of-the-art designs have been plotted on the *FOMS*-C_{LE} and *FOML*-C_{LE} planes in Figure 7. Each point on the plots represents a specific design operating under particular conditions. In cases where the same design is reported with different operating conditions, a line has been drawn to group such instances. Additionally, specific graphic markers have been employed to indicate whether the design utilizes a single-stage, two-stage, or three-stage architecture.

The designs depicted in the plots incorporate advanced slew-rate enhancement techniques, which will be elaborated upon at the circuit level in Section 3. However, the apparent scattered distribution of the designs in Figure 7 does not facilitate the identification of the effectiveness of the various circuit techniques.

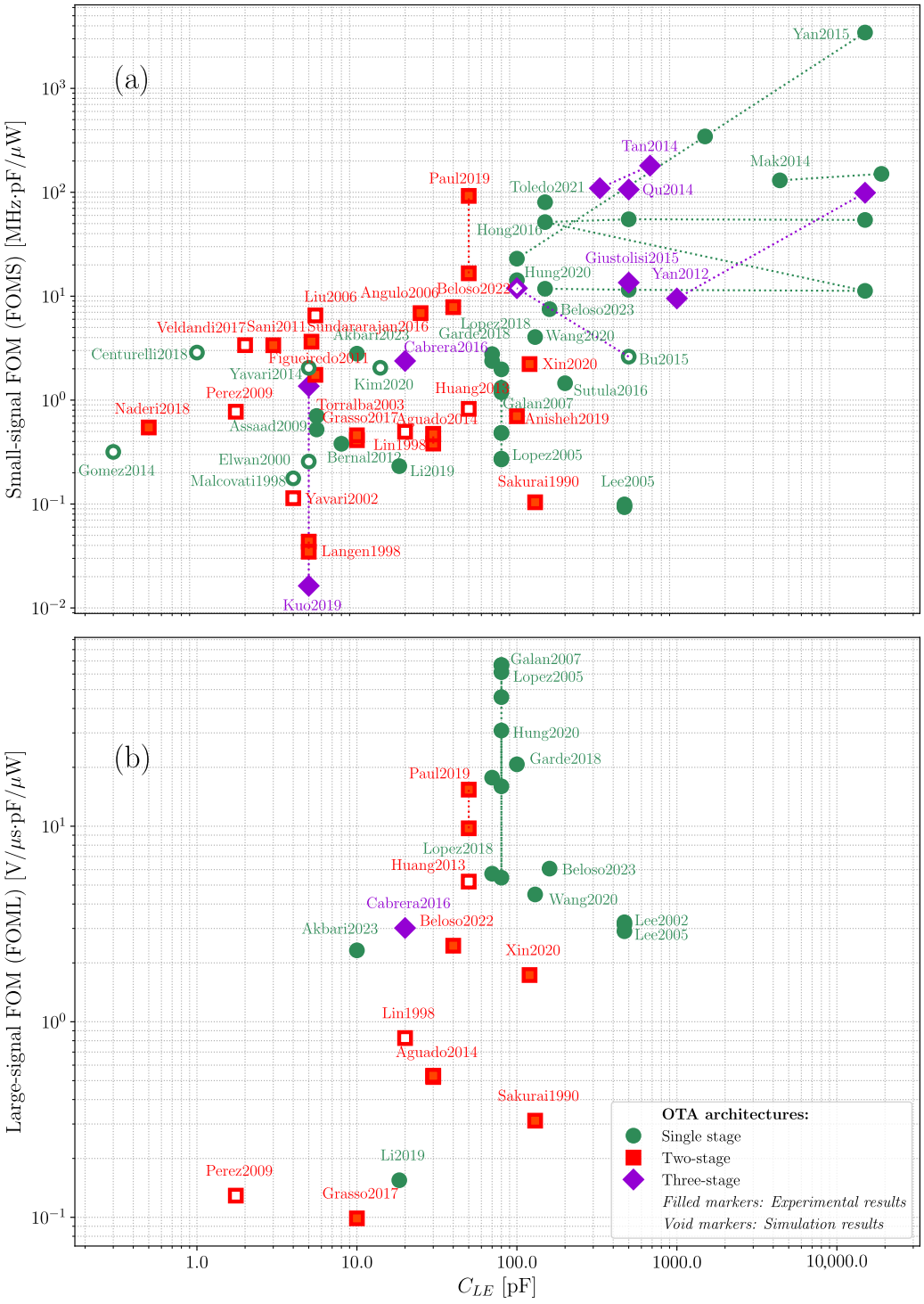

Figure 7. Mapping of state-of-the-art SC circuits: (**a**) *FOMS* vs. C_{LE}; (**b**) *FOML* vs. C_{LE}. Reference pool: [15,26,30–84].

Table 2. Top performers in terms of *FOMS* and *FOML*.

Ref.	FOMS [MHz·pF/µW]	Ref.	FOML [V/µV·pF/µW]
[66]	180.44	[39]	66.67
[64]	130.19	[38]	66.67
[65]	109.39	[40]	45.71
[63]	106.35	[33]	20.72
[44]	80.23	[42]	17.71
[40]	22.97	[85]	15.38
[26]	16.61	[26]	9.75
[33]	14.25	[30]	6.07
[75]	13.52	[41]	5.72
[36]	11.79	[72]	5.21

The situation changes if a more comprehensive FoM is introduced, specifically designed to highlight the whole settling behavior:

$$FOM = C_{LE}\frac{1}{P \cdot t_S}, \tag{31}$$

resulting in the panorama of Figure 8. To the best of the authors' knowledge, this FoM was introduced for the first time in [85] in the field of drivers for LCD applications. A trend line is also depicted in the plot, representing the state-of-the-art frontier. This configuration explicitly highlights the challenge of designing efficient SC circuits as C_{LE} approaches the values of non-dominant parasitic capacitors. To aid in the interpretation of the plot, two regions have been delineated using a C_{LE} value of 10 pF as a boundary. Interestingly, the most efficient designs in the region where $C_{LE} < 10$ pF are primarily based on two-stage architectures, whereas single-stage and three-stage configurations dominate in the region where $C_{LE} > 10$ pF.

However, previous FoMs do not take into account the role played by the amplitude of the input voltage step, V_{id}, in affecting settling performances. Depending on the value of V_{id}, determined by the intended application, the output voltage transient may either be entirely linear or exhibit slew-rate effects. Therefore, considering the diversity of SRE applications targeted by the works considered in this review, we hereby introduce a new FoM, denoted as FOM^*, defined as follows:

$$FOM^* = \frac{C_{LE}V_{id}}{t_S I_{sup}}, \tag{32}$$

where I_{sup} indicates the integrator static supply current. Conversely with respect to previous FoMs, FOM^* is a dimensionless quantity. Moreover, under simplified assumptions, it can be shown that FOM^* is a function of only topology-related parameters. Specifically, by simply assuming the output transient to be dominated by the slew-rate effect ($t_{sr} \gg t_{lin}$), up until reaching the required settling accuracy, the proposed FoM can be rearranged into

$$FOM^* = \frac{\beta_{FB}}{c_1(1-\epsilon_S)} \cdot \frac{I_{omax}}{I_{sup}} \tag{33}$$

Evidently, dependencies with respect to the main degrees of freedom of the SC integrator design (such as I_{sup}, C_L, and V_{id}) vanish. Residual dependencies only involve the settling accuracy specification (ϵ_S) (This term is $\ll 1$, however, hence its influence is negligible in practical cases), parameters related to the capacitive feedback network (β_{FB}, c_1), and the OTA efficiency in terms of maximum output current (I_{omax}/I_{sup}). Clearly, as far as real circuit operation scenarios are concerned (where the linear settling phase is also relevant), (33) results in an oversimplified expression of FOM^*; yet, the proposed FOM^* can be expected to hold its link to the intrinsic slew-rate efficiency of the SRE-assisted OTA.

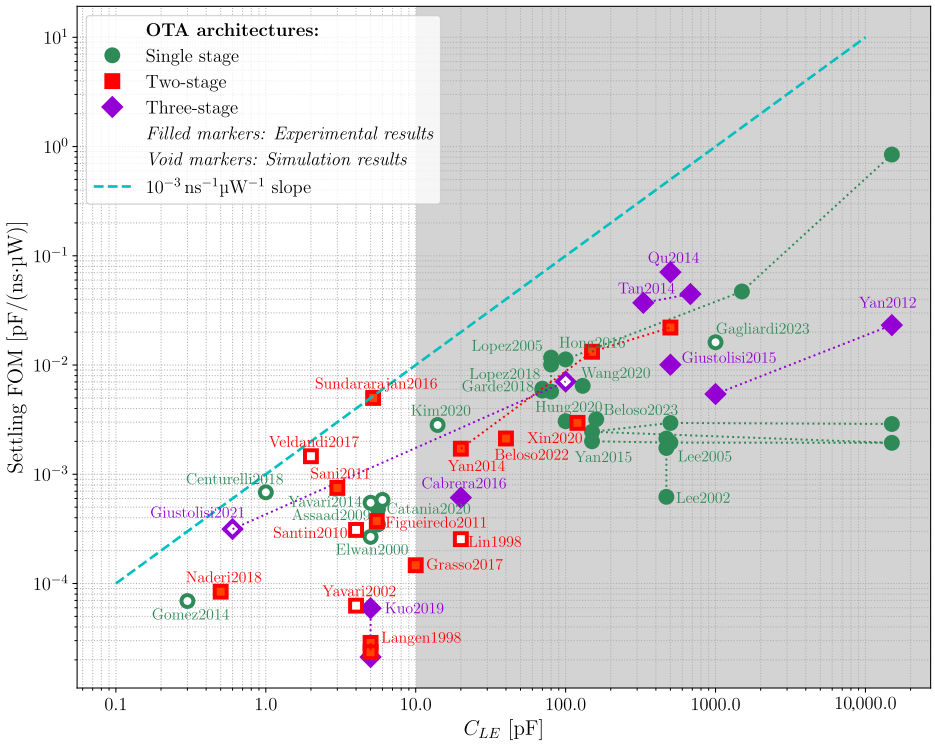

Figure 8. Mapping of state-of-the-art SC circuits: *FOM* vs. C_{LE}. References: [15,26,30,32,33,36,39–43,45–52,54,55,60–63,65,68–70,74–81,83].

The state-of-the-art designs are mapped into the plot of Figure 9. As in the previous case, a design front is evident, reinforcing the thesis of the difficulty of reaching high efficiency when small C_{LE} are targeted.

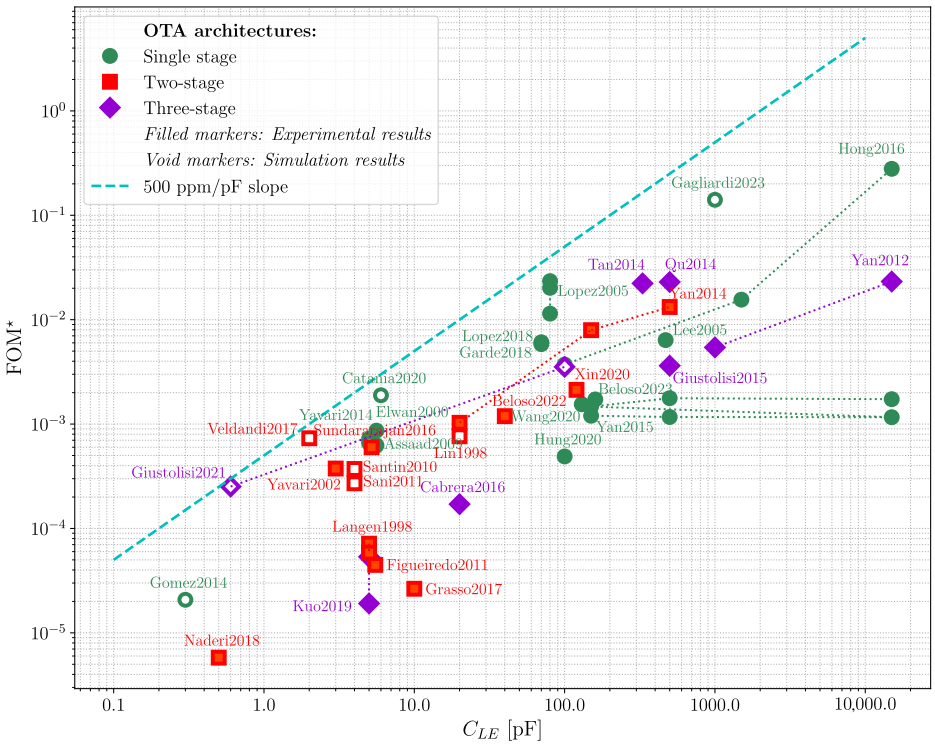

Figure 9. Mapping of state-of-the-art SC circuits: FOM^* vs. C_{LE}. References: [15,26,30,33,36,39–43,45,47–52,54,55,60–63,65,68,69,74–81,83].

3. Advanced OTAs

3.1. Cells and Methods for OTA Enhancement

The main functional components of the simple mirror-based OTA are identified in Figure 10. They consist of the biasing, the transconductive core, and the current mirroring section. For the standard OTA, the biasing is fixed to I_0 (Class-A operation), the transcodunductive core is based on the input differential pair, and the current mirroring section is implemented by the use of standard current mirrors.

Advanced OTA architectures modify one or more of the aforementioned functional components in order to enhance both the G_m and/or the I_{omax} parameters discussed in the simplified model of Section 2.1: the Flipped-Voltage Follower circuit, discussed in Section 3.2, allows Class-AB biasing; the current-recycling and the mirror-nesting techniques, presented in Section 3.3, are devoted to enhance the steering capability of the transconductive core; non-linear current mirrors, described in Section 3.4, are employed to implement Class-AB operation at the output branches of the gain stage only. Furthermore, Compound Body-biased Mosfets, discussed in Section 3.5, are included in this discussion as an interesting technique when targeting low-voltage applications. Finally, Parallel-type Slew-Rate Enhancers, which operate as auxiliary circuits around the main OTA, are discussed in Section 3.6.

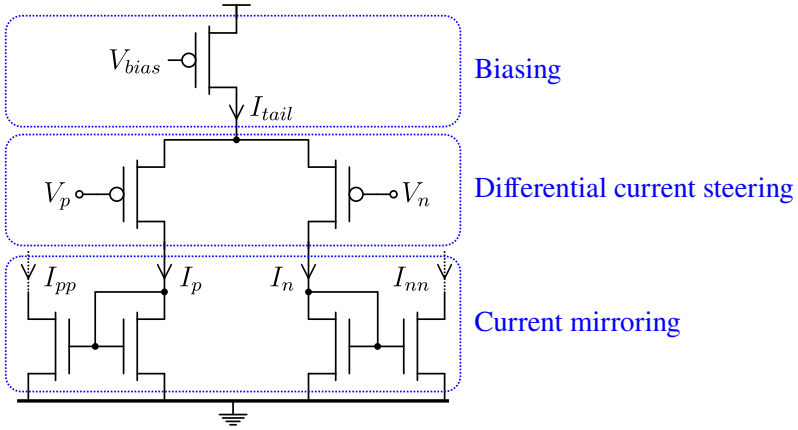

Figure 10. Schematic diagram of the functional parts of a mirror-based OTA.

For the explanation of the advanced subcircuits, the simple yet powerful EKV model is employed, which is able to capture both strong and weak inversion operation of the MOS transistor in an amenable design-oriented fashion [20]. In this model, V_T, U_t, n, and β stand for the threshold voltage, thermal potential, subthreshold slope, and current factor, respectively.

3.2. Flipped Voltage Follower (FVF) Cell

The Flipped-Voltage Follower (FVF) is a versatile cell formally described in [86], although it was already introduced in [87]. Among the many uses that this cell can offer, we will focus on its use as (i) current buffer loop for class-AB current biasing and (ii) low-voltage current mirror. These functionalities are illustrated in Figure 11a and Figure 11b, respectively.

Looking at Figure 11a, two distinct FVFs are present: FVF1 is composed by M0c-M01-M0a, while FVF2 is composed by M0d-M02-M0b. Both FVF1 and FVF2 will be referred to as PMOS-FVFs to distinguish them from the complementary implementation (NMOS-FVF) of Figure 11b. M0a and M0b set the bias currents I_0 of FVF1 and FVF2, respectively. Thanks to the loop around M01-M0c (M02-M0d), a constant V_{GS} is set for M01 and M02, regardless of the current absorbed at the sources of M1 and M2.

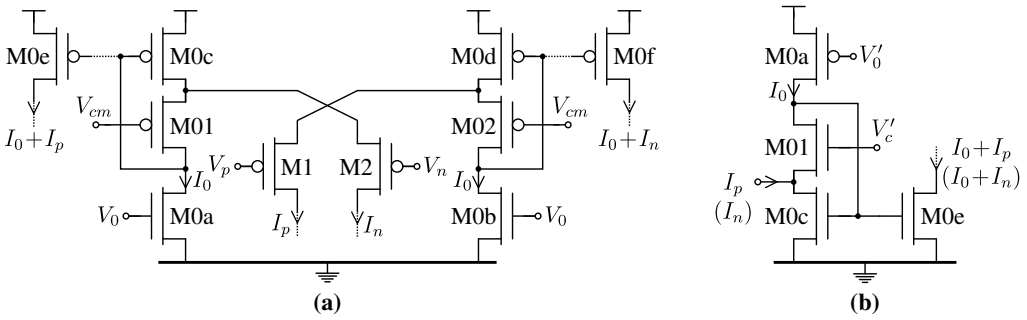

Figure 11. Schematic diagrams of Flipped Voltage Follower employed as (**a**) current buffer loop for class-AB current biasing, (**b**) low-voltage current mirror.

Assuming V_p and V_n to follow $V_i = V_p - V_n$ and $V_{cm} = \frac{1}{2}(V_p + V_n)$, the drain currents of the PMOS input devices, M1 and M2, can be found as follows:

$$I_p(V_i) = \frac{\beta}{2n}\left(-\frac{V_i}{2} + \sqrt{\frac{2nI_0}{\beta_0}}\right)^2, \quad I_n(V_i) = \frac{\beta}{2n}\left(\frac{V_i}{2} + \sqrt{\frac{2nI_0}{\beta_0}}\right)^2. \tag{34}$$

In these expressions, β is related to M1 and M2, while β_0 is related to M01 and M02. While the quiescent operating current of M1 and M2 is set to be $(\beta/\beta_0)I_0$, its magnitude grows quadratically with $|V_{id}|$, hence implementing a compact class-AB biasing of the transcoductive core of the OTA. Eventually, M0e and M0f can be added to the structure to provide a copy of I_p and I_n directly to OTA output branches. The circuit is able to operate with V_{DD} as low as $|V_T| + 2|V_{DSsat}|$. However, V_{cm} needs to be set in order to maintain M0c and M0d in the saturation region of operation. For the PMOS-FVFs, this limit is also expressed by $V_{cm} < V_{DD} - |V_T| - 2|V_{DSsat}|$.

The FVF structure illustrated in Figure 11b implements a low-voltage current mirror. It is able to absorb high-dynamic currents I_p, I_n, eventually sourced from the transconductive core of Figure 11a, and to mirror towards the output device M0e.

A possible limitation concerning the FVF is the fact that voltages V_{cm} and V_c' need to be extracted from the inputs V_p and V_n by dedicated auxiliary circuits in order to maintain the correct biasing of the OTA, thus increasing its complexity. In some implementations, the gates M01 and M02 are connected to V_n and V_p, respectively, simplifying the extraction of V_{cm} and incrementing also the class-AB current boosting, at the cost of even more limited input range. Regarding offset and input-referred noise, the configuration depicted in Figure 11 is evidently less effective than a standard differential pair, primarily due to the increased number of mismatch and noise contributors. Designers are therefore advised to carefully consider this aspect.

3.3. Current Recycling and Mirror Nesting

The current recycling technique was originally proposed in [49] in order to enhance both the transconductance and the slew-rate of a standard folded-cascode OTA. The transcoductive core of the circuit is illustrated in Figure 12a. New design parameters, related to geometrical ratios between the involved transistors, are introduced in this structure: k_a, k_b, n_a, m_a. These parameters affect both the bias and the signal-dependent components of the currents in the branches. The input pair bias current provided by M0 is now considered to be equal to $2(k_a + k_b)I_0$. In the following, we consider (M1a, M2a) and (M1b, M2b) as composed by a k_a-parallel and k_b-parallel, respectively, of identical (unitary) transistors. Each unitary transistor is biased, ideally, by a current equal to I_0. The small-signal transconductance of unitary transistors will be referred to as g_{m0}. As indicated in Figure 12a, the bias current component in the folded branches (e.g., through MC3 and MC4) is as follows:

$$I_{\text{bias}} = \left(\frac{n_a}{m_a}k_a - k_b\right)I_0, \tag{35}$$

which clearly imposes the following constraint: $k_b < \frac{n_a}{m_a} k_a$. On the other hand, G_m and I_{omax} are easily found by circuit inspection as follows:

$$G_m = \left(\frac{n_a}{m_a} k_a + k_b \right) g_{m0}, \quad I_{omax} = 2(k_a + k_b) \frac{n_a}{m_a}. \tag{36}$$

The portion of the static supply current drawn by the transcoductive core results is as follows:

$$I_{sup,\text{core}} = 2 \frac{n_a}{m_a} k_a I_0. \tag{37}$$

At this point, simple efficiency metrics can be introduced:

$$\eta_{G_m} = \frac{G_m}{I_{sup,\text{core}}} \frac{I_0}{g_{m0}} = \frac{1}{2} \left(1 + \frac{m_a}{n_a} \frac{k_b}{k_a} \right); \quad \eta_{\text{SR}} = \frac{I_{omax}}{I_{sup,\text{core}}} = 1 + \frac{k_b}{k_a}. \tag{38}$$

These metrics show that the slew-rate efficiency, η_{SR}, of the recycling folded cascode can be increased by increasing k_b/k_a. Since the bias constraint imposes $n_a/m_a > k_b/k_a$, the transconductance efficiency, η_{G_m}, tends to saturate for large values of k_b/k_a. Moreover, large n_a/m_a ratios tend to erode the OTA phase margin due to the zero-pole doublet associated to the current mirrors formed by M3a–M5a and M4a–M6a. In practice, the set of parameters $(k_a = 1, k_b = 1, m_a = 1, n_a = 3)$ is often used.

The transconductive core of the circuit in Figure 12b follows a similar principle. Differently from the previous case, the low-impedance nodes are all constituted by input sections of NMOS current mirrors. This peculiarity allows for repeating the same structure iteratively, furtherly boosting the transconductance and slew-rate efficiencies with respect to the standard current-recycling technique. Such a circuit topology is known as nested-mirror OTA. Similar considerations as for the recycling folded cascode apply also in this case, with the only difference that here one more zero-pole doublet is introduced for each nesting iteration. The structure was introduced in [88] and later expanded to multiple (>2) nesting iterations in [36], becoming a de facto reference structure for very large output capacitive loads.

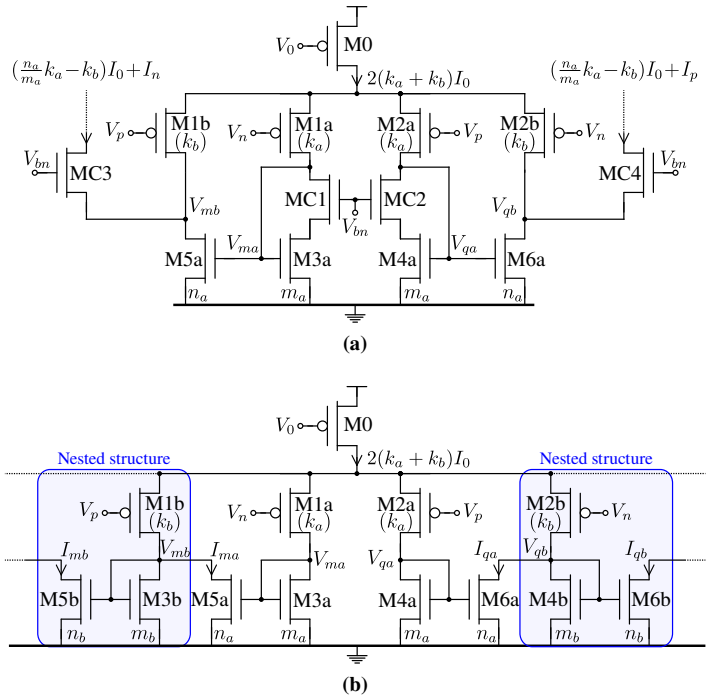

Figure 12. Schematic diagrams of: (**a**) transconductive core of the PMOS-input recycling folded cascode OTA, (**b**) transconductive core of the PMOS-input nested-mirror OTA.

3.4. Non-Linear Current Mirrors

Non-linear current mirrors are used to enhance the current mirroring section of the OTA of Figure 10. These mirrors intentionally establish a non-linear connection between the input current, I_1, and the output current of the mirror, I_2. This deliberate non-linearity is introduced to realize a specific $I_2(I_1)$ characteristic, often designed to exhibit a super-linear behavior. This feature is used to deliver high-class AB currents to the output of the OTA, without resorting to high-current amplification ratios of the current mirror, which would also result in amplification of the static bias currents.

Various techniques can be employed to achieve a non-linear $I_2(I_1)$ characteristic. To present a comprehensive overview, let us examine the current mirror cells depicted in Figure 13. In Figure 13a, a controlled voltage generator, V_C, is placed in series with the input section gate voltage, V_G. Referring to a general case, regardless of the circuital implementation of V_G, we assume $V_C(I_1)$ is such that $dV_C/dI_1 > 0$ in all the operation intervals of interest of I_1. In this analysis, the drain of M2 is set to a suitable voltage in order to maintain the saturation region, $V_{D2} > V_G + V_C - V_T$. Since the source and bulk terminals of M1 and M2 are grounded, I_1 and I_2 are determined by their respective gate voltages, V_G and $V_G + V_C$. By means of a simple mathematical analysis, we find:

$$\frac{dI_2}{dI_1} = 1 + \frac{dV_C}{dV_G} = 1 + \frac{dV_C}{dI_1}\frac{dI_1}{dV_G} = \begin{cases} 1 + \frac{dV_C}{dI_1}\sqrt{\frac{2\beta I_1}{n}} & \text{(strong inversion)}, \\ 1 + \frac{dV_C}{dI_1}\frac{I_1}{nU_t} & \text{(weak inversion)}. \end{cases} \tag{39}$$

Hence, $I_2(I_1)$ shows a super-linear characteristic, by virtue of the only condition $dV_C/dI_1 > 0$.

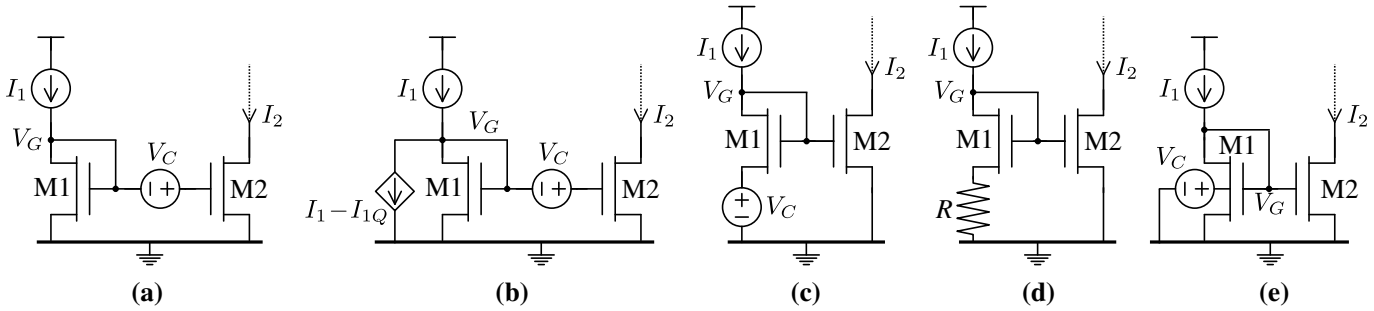

Figure 13. Schematic diagrams of non-linear current mirror configurations: (**a**) gate-series $V_C(I_1)$; (**b**) same as previous but with constant V_G; (**c**) source-series $V_C(I_1)$; (**d**) trivial implementation of the previous by the means of a resistor; (**e**) body modulation at the input device.

The circuit in Figure 13b introduces a minor modification compared to Figure 13a. In this configuration, V_G remains constant at the quiescent value established by I_{1Q}, regardless of variations in I_1. This circuit is introduced to mirror the circuit implementation depicted in Figure 14a, which will be discussed later.

In the source-series V_C configuration depicted in Figure 13c, we can apply considerations that are analogous to those already discussed for the gate-series configuration in Figure 13a. Meanwhile, in Figure 13d, a straightforward implementation utilizes a resistor. For this specific scenario, $V_C = RI_1$, leading to $dV_C/dI_1 = R$. However, this solution is sub-optimal for low-current (low-power) circuits, where a large value of R is required to achieve a significant class-AB boosting effect. In such cases, R can be replaced by triode-operating MOSFETs [89].

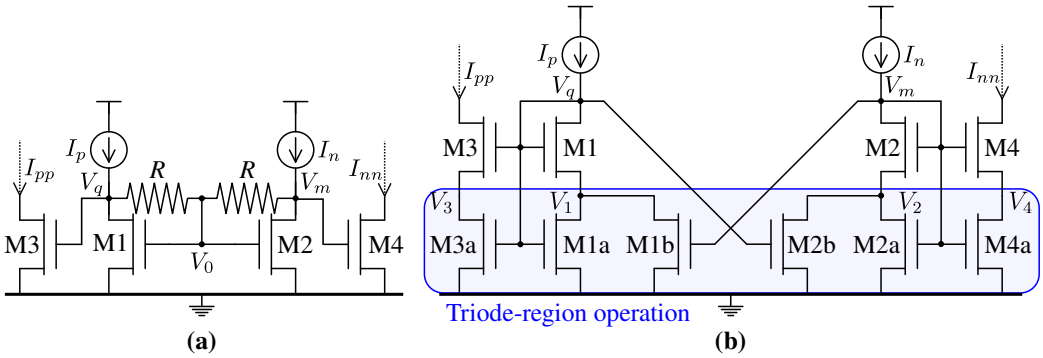

Figure 14. Schematic diagrams of differential non-linear currents mirrors: (**a**) structure based on local common-mode feedback circuit (LCMF) and (**b**) structure based on the non-linear source degeneration.

Finally, Figure 13e illustrates a scheme that realizes body modulation at the input device. Clearly, this technique can be implemented only if the active devices can be put in an isolated well. Both I_1 and $V_C(I_1)$ are forced by the external circuits: V_G increases if either I_1 or V_C increases. As a consequence, I_2 increases as well, tracking the increments of both I_1 and V_C. Simple algebraic manipulations lead to the following:

$$I_2(I_1) = \begin{cases} \frac{\beta_2}{2n}\left(\sqrt{\frac{2nI_1}{\beta_1}} + V_C(I_1)\right)^2 & \text{(strong inversion)}, \\ I_1 \exp\left(\frac{V_C(I_1)}{nU_t}\right) & \text{(weak inversion)}. \end{cases} \tag{40}$$

These expressions also follow the relationships outlined in (39). An important consideration in body biasing is the potential turn-on of the body-well junction when V_C increases excessively. This must be avoided, as it would lead to increased power consumption without providing any additional boost to the output current I_2.

Two significant implementations of the aforementioned techniques are presented in Figure 14a and Figure 14b, respectively. Both circuits employ a differential configuration in order to provide a compact implementation of the control voltage generator V_C.

The circuit in Figure 14a is known as local common-mode feedback circuit (LCMF) and it is related to the configuration discussed in Figure 13b. Here, V_0, corresponding to the gate voltage of the input devices, M1 and M2, is kept constant, provided that the input currents I_p and I_n have a constant common mode. In the quiescent operation point $I_p = I_n$, hence $V_q = V_m = V_0$. Additionally, the quiescent point of the output currents, I_{pp} and I_{nn}, is nominally identical, defined according to the model of a standard current mirror. Any differential component flows through the $2R$ series, creating an imbalance between V_q and V_m, expressed by the following equations:

$$V_q = V_0 + R(I_p - I_n), \quad V_m = V_0 - R(I_p - I_n), \tag{41}$$

which triggers the class-AB boosting of the output currents, discussed earlier. The choice of the R resistors values is crucial and should align with the bias levels of the quiescent currents. If R is too low with respect to $1/g_{m1,2}$, it results in weaker class-AB boosting. Conversely, if R is excessively high, the nodes at the drain terminals of M1 and M2 start to be affected by inertial effects, potentially compromising the OTA phase margin.

The implementation in Figure 14b provides a compact realization of the principle explained in Figure 13c [90]. Devices M1, M2, M3, and M4 operate in saturation and are nominally identical, while devices M1a, M2a, M3a, M4a, M1b, and M2b typically operate in the triode region. The drain voltages of the latter group of devices are labeled as V_1, V_2, V_3, and V_4, as illustrated in Figure 14b. Additionally, these devices are characterized by the following aspect ratios: A for M1a and M2a, B for M1b and M2b, and $C = A + B$ for M3a and M4a.

Assuming ideal matching of the devices, operated with $I_p = I_n$, and considering the electrical and geometrical symmetry of the circuit, it can be shown that $I_{pp} = I_{nn}$, $V_q = V_m$, and $V_1 = V_2 = V_3 = V_4$. Any imbalance in the input currents will manifest as an imbalance between V_q and V_m, as well as between the drain voltages of the triode-operating devices. While V_3 depends only on V_q and V_4 depends only on V_m, V_1 and V_2 depend on both V_q and V_m. As a result, any imbalance between V_q and V_m breaks the electrical symmetry of the mirrors, leading to non-linear characteristics in the resulting output currents with respect to the input currents (This consideration can be easily translated to input-referred offset worsening as far as mismatch is considered. Again, the designer is warned to carefully check this aspect).

Detailed analysis can be retrieved from the original work [35]. Here, our analysis is limited to the case of perfectly balanced differential driving:

$$I_p = I_{cm} + I_{dm}/2; \quad I_n = I_{cm} - I_{dm}/2, \tag{42}$$

where I_{cm} represents the fixed common-mode current, and I_{dm} represents the variable differential-mode current. This driving scheme mimics the standard class-A differential pair circuit.

At this point, we observe that, despite their non-linear behavior, the triode-operating devices can be treated as source-degeneration resistors. Focusing on the current mirror composed by M1 and M3, we can identify the following degeneration resistors: $R_3(V_q)$, corresponding to M3a, $R_{1a}(V_q)$, corresponding to M1a, and, finally, $R_{1b}(V_m)$, corresponding to M1b. Since R_3 and R_1 are connected to the same controlling voltage V_q, the ratio $R_{1a}/R_3 = C/A = 1 + B/A$ depends only on the aspect ratios of the transistors.

As V_m decreases, concurrently with an increase in V_q, it follows that $R_{1b} > R_{1a}$. This mechanism, involving M1b, results from a positive feedback path. However, this is counterbalanced by the parallel negative feedback path involving M1a. As M1a and M1b are related to the geometrical parameters A and B, the amount of positive feedback becomes a degree of freedom in the hands of the designer.

Eventually, as I_{dm} increases, the $V_q - V_m$ imbalance reaches a condition where $R_{1b} \gg R_{1a}$: at this point, the source degeneration of M3 and M1 is determined only by R_3 and R_{1a}, respectively. Since $R_{1a} > R_3$ by geometrical construction, I_{pp} will be greater than I_p by an amount related to B/A, i.e., the amount of positive over negative feedback. An excess of positive feedback may induce latching problems as well as slow response of the Class-AB currents, degrading the settling period. The exact relationship between I_{pp} and I_p, as derived in [35], depends on the operation region of the devices.

3.5. Compound Body-Biased Mosfets

The compound body-biased MOSFETs (CBBM) technique, introduced in [78], aims to enhance the transistor intrinsic DC gain without compromising the frequency response. This technique is not directly linked to slew-rate enhancing per se. However, since it can be amalgamated with the previous circuital techniques in low-voltage scenarios, it deserves to be discussed in this review.

The CBBM technique employs a pair of stacked MOSFETs, MA and MB, as illustrated in Figure 15. The configuration resembles a pseudo-cascode structure, with the only difference being that the bulk terminal of MA is utilized to bias MB into the saturation region. In a standard pseudo-cascode compound, $V_B = 0$, forcing MB to operate in the triode region. However, in the CBBM structure, $V_B > 0$ to reduce the effective threshold voltage of MA. When V_B reaches a proper value, $V_{B,\min}$, V_X becomes high enough to allow MB to exit the triode region. It is important to note that setting $V_B > 0$ implies that the technology allows for isolated wells. Consequently, a maximum value of V_B, denoted as $V_{B,\max}$, must be observed to avoid the turn-on of the body-well junctions. Therefore, this technique is viable only if $V_{B,\min} < V_{B,\max}$.

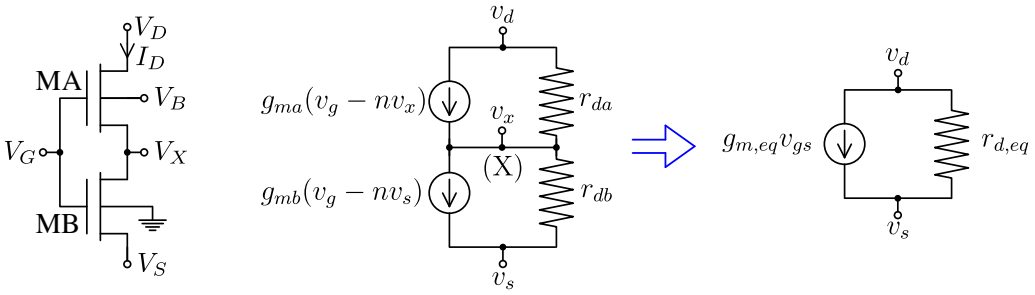

Figure 15. Schematic diagrams of the compound body-biased MOSFET (CBBM): (**a**) basic structure and (**b**) small-signal circuits.

In the upcoming discussion, we will demonstrate how $V_{B,\min}$ can be established through design considerations by manipulating the sizing of MA and MB. We will focus on two distinct design cases: (i) both MA and MB operating in strong inversion, and (ii) both MA and MB operating in weak inversion. While mixed cases are also analyzable, they will not be covered in this text. To facilitate our discussion, we will adhere to the following simple convention: β_A and I_{SA} will be assigned to MA, while β_B and I_{SB} will be assigned to MB. ISA and I_{SB} indicate the weak-inversion specific currents of the two transistors.

Now, we can express the following equations, assuming $V_S = 0$ (i.e., the CBBM source node corresponds to our reference node):

$$I_D = \begin{cases} \frac{\beta_A}{2n}[V_G - V_T - nV_X + (n-1)V_B]^2 = \frac{\beta_B}{2n}(V_G - V_T)^2 & \text{(strong inversion)} \\ I_{SA} e^{\frac{V_G - V_T}{nU_t}} e^{-\frac{V_X}{U_t}} e^{\frac{\eta - 1}{\eta}\frac{V_B}{U_t}} = I_{SB} e^{\frac{V_G - V_T}{nU_t}} \left(1 - e^{-\frac{V_X}{U_t}}\right) & \text{(weak inversion)} \end{cases} \tag{43}$$

For MB to operate in the saturation region, we can elaborate Equation (43) to explicitly express V_X:

$$V_X = \begin{cases} \dfrac{(n-1)V_B - (\sqrt{\beta_B/\beta_A} - 1)(V_G - V_T)}{n} \geq V_G - V_T & \text{(strong inversion)} \\ U_t \ln\left(\dfrac{1}{I_{SA}/I_{SB} + e^{-\frac{n-1}{n}\frac{V_B}{U_t}}}\right) \geq 4U_t & \text{(weak inversion)} \end{cases} \tag{44}$$

The inequalities of Equation (44) can be elaborated to find expressions for $V_{B,\min}$:

$$V_{B,\min} = \begin{cases} \left(1 + \frac{\sqrt{\beta_B/\beta_A}}{n-1}\right)(V_G - V_T) & \text{(strong inversion)} \\ \frac{n}{n-1} U_t \ln\left(\frac{1}{I_{SA}/I_{SB} + e^{-4}}\right) & \text{(weak inversion)} \end{cases} \tag{45}$$

In the weak inversion case, a further condition applies: $I_{SA} < (1 - e^{-4})I_{SB}$ to ensure $V_{B,\min} > 0$.

The advantages of the CBBM structure are evident when analyzing the small-signal parameters of the circuit. Referring to Figure 15b, we aim to derive the equivalent small-signal parameters $g_{m,eq}$, $r_{d,eq}$ and g_x from the small-signal parameters of MA and MB. Through simple analytical considerations, we find:

$$g_{m,eq} \approx g_{mb}, \quad r_{d,eq} \approx n g_{ma} r_{da} r_{db}, \quad g_x \approx n g_{ma}. \tag{46}$$

The expressions have been simplified considering the usual inequalities $g_{ma}, g_{mb} \gg 1/r_{da}, 1/r_{db}$. We also observe that the node X can be used to provide a low-impedance path (g_x) for further flexibility. This node has been used in [78] to implement a (pseudo) cascode frequency compensation of a two-stage OTA. Based on (46), it is clear that as MB enters the saturation region, it dominates the overall transconductance. At the same time, its output impedance is magnified as in a traditional cascode configuration, hence boosting the intrinsic gain of the compound. Although the CBBM structure is not intrinsically related to slew-rate enhancing nor to transconductance boosting, we believe that future work exploring amalgamation of this technique with other techniques exposed here may result in high-performance OTA subunits.

3.6. Parallel-Type Slew-Rate Enhancer (PSRE)

The parallel slew-rate enhancer (PSRE) approach is schematically depicted in Figure 16a. The PSRE establishes a parallel path for signal propagation across the OTA only during the slewing transient. During this part of the settling transient, the PSRE is turned-on and delivers high currents at the output nodes, effectively enhancing the system slew-rate. Conversely, the PSRE is completely turned-off during the last part of the transient, when the OTA enters its linear response region. Consequently, the precise adjustment of the residual output voltage is delegated to the main OTA. Importantly, the adoption of PSREs does not impact the DC gain, offset, or noise of the OTA, effectively isolating the slew-rate from other specifications.

In practice, to avoid lags in the activation of the PSRE, which directly sums up to the settling time, part of the PSRE is kept turned-on, i.e., it works in Class-A. This fact leads to t_{set} optimization scenarios, concerning the supply current distribution between the main OTA and the PSRE, when a total static current budget is assigned.

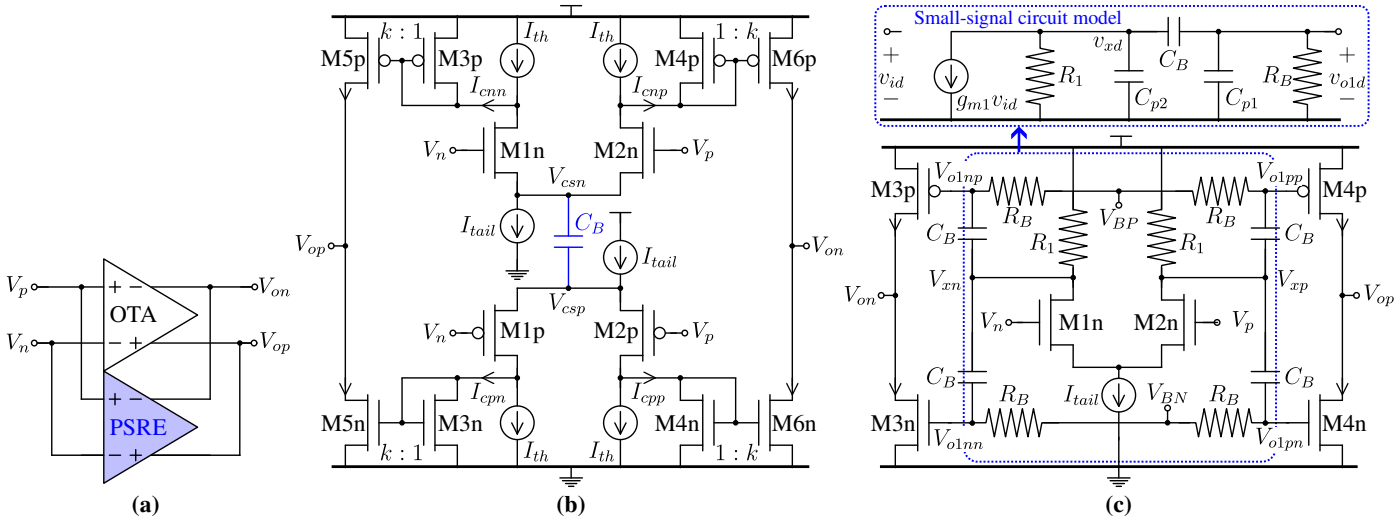

Figure 16. Schematic diagrams of (**a**) OTA+PSRE configuration; (**b**) Implementation of a PSRE based on current mirrors, enhanced by the boost capacitor C_B; (**c**) Implementation of a class-B PSRE based on *RC*-bias ties.

An important aspect to consider when a PSRE is used is that its output currents are not intrinsically balanced around a common mode. Common-mode components may arise from V_{DS} effects at the output transistors of the PSRE, as well as from internal mismatch between current mirroring blocks. Therefore, output common mode regulation is left to the main OTA, which in general is already equipped with this functionality. However, as the PSRE peak output currents increase, their common mode also increases. Consequently, the OTA-PSRE combination may require some additional, but generally simple, design step to attain the correct settling behavior.

Figure 16b,c shows two different implementations of the PSRE, respectively, based on current mirrors and on a class-B output stage.

The PSRE in Figure 16b is activated when the absolute value of the input differential voltage surpasses a certain activation threshold, e.g., $|V_p - V_n| \geq V_A$, while if $|V_p - V_n| < V_A$, then the PSRE operates in its deadzone, not providing any output current due to its output devices being turned-off. The first concept of this kind of circuit was introduced by Nagaraj in [91]. When the PSRE operates within the deadzone, all the available current provided by the differential pair is absorbed by the shunt current sources I_{th}. To this purpose, the condition $I_{th} > I_{tail}/2$ needs to be set by design. Hence, within the deadzone, the current mirrors Mm3p-Mm5p, Mm4p-Mm6p, Mm3n-Mm5n, and Mm4n-Mm6n are off and the output nodes are rendered in high impedance. When the input pair is fully unbalanced by a large input voltage, a non-zero current is conveyed into the selected mirrors if $I_{tail} > I_{th}$. Hence, the circuit is constrained by the following inequalities: $I_{tail}/2 < I_{th} < I_{tail}$, which can be satisfied by the mismatch-robust choice of $I_{th} = \frac{3}{4} I_{tail}$. For this choice, $V_A \approx 1.855\sqrt{2nI_{tail}/\beta}$ if the PSRE input pair is operated in strong inversion, or $V_A \approx 1.099 n U_t$, if operated in weak inversion. Furthermore, it is convenient to set the V_{dmax} of the PSRE slightly less than V_A in order to ensure that, outside of the deadzone, the PSRE delivers the maximum current to the output, which will result in $I_{omax,\mathrm{PSRE}} = k(I_{tail} - I_{th}) = kI_{tail}/4$.

As the desired output voltage level is approached, marked by the condition $|V_p - V_n| = V_A$, the SRE output devices deactivate, causing the SRE outputs to transition to high impedance. Hence, neglecting inertial effects, the system obtains the maximum benefit if V_A is set to be equal (or even less) than the V_{dmax} of the OTA.

Neglecting inertial effects (hence neglecting also the effects of the C_B element in Figure 16b), a high overall slew-rate is obtained by simply increasing the mirror amplification factor k instead of increasing the PSRE static current consumption ($I_{sup,\mathrm{PSRE}} = 2I_{tail}$). In such simplified conditions, an optimization of t_S for a given current budget, $I_{sup} = I_{sup,\mathrm{OTA}} + I_{sup,\mathrm{PSRE}}$, is possible. In the first place, let us introduce η as follows:

$$\eta = \frac{I_{sup,\mathrm{PSRE}}}{I_{sup,\mathrm{OTA}}} \implies I_{sup} = (1+\eta) I_{sup,\mathrm{OTA}}. \tag{47}$$

Secondly, we relate $I_{sup,\mathrm{OTA}}$ to the G_m and $I_{omax,\mathrm{OTA}}$ of the OTA block, as well as $I_{sup,\mathrm{PSRE}}$ to $I_{omax,\mathrm{PSRE}}$ of the PSRE:

$$G_m = \frac{V_{TE,\mathrm{OTA}}}{I_{sup,\mathrm{OTA}}}; \quad I_{omax,\mathrm{OTA}} = k_{\mathrm{OTA}} I_{sup,\mathrm{OTA}}; \quad I_{omax,\mathrm{PSRE}} = k_{\mathrm{PSRE}} I_{sup,\mathrm{PSRE}}. \tag{48}$$

From the previous discussion, we are already able to calculate

$$k_{\mathrm{PSRE}} = \frac{I_{omax,\mathrm{PSRE}}}{I_{sup,\mathrm{PSRE}}} = \frac{kI_{tail}/4}{2I_{tail}} = \frac{k}{8}, \tag{49}$$

while $V_{TE,\mathrm{OTA}}$ and k_{OTA} are contingent upon the specific OTA topology. In particular, $V_{TE,\mathrm{OTA}}$ assumes the same role in defying the G_m efficiency of the OTA as in (20), previously discussed in Section 2.2.

We are interested in the case where a maximum $|V_{id}|$ causes the system to produce a combination of slewing and linear settling phases in the output transient. Moreover, we indicate as $t_{S,\max}$ the settling time related to the maximum input step, $|V_{id}|_{\max}$. In these conditions, Equation (16) can be rewritten as follows:

$$t_{S,\max} = \frac{c_1 C_{IE}}{I_{omax}} \left(|V_{id}|_{\max} - \frac{V_{dmax}}{c_1} \right) + \frac{C_{IE}}{G_m} \left(\ln \frac{c_2 V_{dmax}}{\epsilon_S |V_{id}|_{\max}} \right), \tag{50}$$

where the maximum output current during the slewing period is given as follows:

$$I_{omax} = I_{omax,\mathrm{OTA}} + I_{omax,\mathrm{PSRE}}. \tag{51}$$

Considering Equations (47), (48), (50) and (51), we can express $t_{s,\max}$ as follows:

$$t_{S,\max} = (1+\eta)\left(\frac{t_1}{k_{\mathrm{OTA}} + \eta k_{\mathrm{PSRE}}} + t_2\right), \text{ where: } \begin{cases} t_1 = \frac{C_{IE}}{I_{sup}} \cdot (c_1 |V_{id}|_{\max} - V_{dmax}) \\ t_2 = \frac{C_{IE}}{I_{sup}} \cdot \left(V_{TE,\mathrm{OTA}} \ln \frac{c_2 V_{dmax}}{\epsilon_S |V_{id}|_{\max}}\right) \end{cases} \tag{52}$$

The settling time $t_{S,\max}$ can be minimized looking at the derivative with respect to η:

$$\frac{\partial t_{S,\max}}{\partial \eta} = 0 \implies \eta_{\mathrm{opt}} = \frac{1}{k_{\mathrm{PSRE}}}\left(-k_{\mathrm{OTA}} + \sqrt{\frac{t_1}{t_2}(k_{\mathrm{PSRE}} - k_{\mathrm{OTA}})}\right). \tag{53}$$

A valid η_{opt} is found for $k_{\mathrm{PSRE}} > k_{\mathrm{OTA}}(1 + k_{\mathrm{OTA}} t_2/t_1)$. In practice, this condition implies a minimum $k(= 8k_{\mathrm{PSRE}})$ to be employed.

Up to this point, inertial effects of PSRE have been neglected. However, the settling time is affected also by the turn-on and the turn-off lags of the PSRE output mirrors. These lags are more evident as k is increased excessively. This effect can be seen by looking at the total gate capacitance of the PSRE output mirror, C_G, which is dominated by the gate-source and the gate-drain parasitic capacitances of the output device (whose overall area is proportional to k). The charge and discharge process of such a capacitance can be modeled considering the non-linear differential equation described in [92] and characterized by a time constant τ that can be expressed as follows:

$$\tau = \frac{C_G}{g_{m0}} = \frac{C_{G0}(1+k)}{g_{m0}}, \tag{54}$$

where g_{m0} and C_{G0} are, respectively, the transconductance and the gate capacitance associated to the input transistor of the mirror. It is worth noting that τ clearly refers to a linearized circuit model, which can, however, serve as a first-order approximation of the actual solutions derived from the large-signal model of the current mirror [92].

Since the PSRE activation is linked to a large-signal step, sensed either at the inputs or at the clock edge, dynamic biasing schemes are also possible for this circuit [93]. Following this idea, a capacitance boosting technique is proposed in [15] by adding the capacitor C_B between the source terminals of the complementary input differential pairs of the original Nagaraj's PSRE, as illustrated in Figure 16b. The boosting effect provided by C_B can be analyzed as follows: the steady-state value of the common source voltages (V_{csn0}, V_{csp0}) are determined by the input common mode V_{ic} and I_{tail}. Hence, C_B is charged at $C_B(V_{csn0} - V_{csp0})$. At the onset of an input voltage step (either positive or negative), V_{csn} is pulled up by a voltage difference ΔV_{csn}, while V_{csp} is pulled down by ΔV_{csp}. This causes C_B to promptly absorb an amount of charge $\Delta Q_B = C_B(\Delta V_{csn} + \Delta V_{csp})$. Depending on the sign of the input voltage step, one of the following low-impedance paths is enabled: (i) M2n and M1p (positive input steps), or (ii) M1n and M2p (negative input steps). The low-impedance paths facilitate the transit of ΔQ_B towards one of the respective output mirror sections. This mechanism effectively helps prompt turn-on of the corresponding mirror by charging their respective C_G. The larger the voltage step, the more efficient the charge injection mechanism, hence a larger slew-rate boosting is obtained.

It is worth noting that the turn-off mechanism is much less efficient with respect to the turn-on mechanism, even in the presence of C_B: at the transition of the PSRE back into the deadzone region, V_n and V_p have similar values, and the initial state of charge of C_B is mostly restored by the I_{tail} sources. The fraction of I_{tail} that reaches the output mirror sections is then combined with I_{th} to provide a net current that discharges C_G, turning off the output mirrors. Hence, while the C_B significantly shortens the turn-on

delay of the PSRE, it leaves almost unvaried the turn-off delay. In practical designs, the use of C_B is beneficial for moderate values of k, contingent upon the predominance of the turn-off delay, which in change is still strongly dependent on I_{tail} (hence, on the static power consumption). The value of η_{opt} found in Equation (53) can serve as a starting point before further optimization of both k and η is conducted.

The PSRE depicted in Figure 16c was first introduced in [52,94] for high-speed SC pipeline ADC applications, operating beyond 100 MHz sampling rates. Such a circuit resembles a two-stage OTA setup. The initial stage, comprising M1n-M2n and R_1, operates as a low-gain preamplifier, while the subsequent stage consists of an RC-bias tie push-pull arrangement [58,95]. The output stage, devoid of any DC coupling, features output push-pull pairs (M3p-M3n, M4p-M4n) that are AC coupled through capacitive-resistive networks formed by C_B and R_B. DC biasing is ensured thanks to R_B resistors providing bias voltages V_{BP} and V_{BN}. In this specific setup, these voltages are adjusted to maintain the output transistors in cut-off during steady-state conditions, thereby implementing class-B operation. This is crucial to prevent DC-gain degradation of the main OTA.

When considering the linearized equivalent circuit for differential signals, we can express the transfer function as follows:

$$H(s) \approx \frac{A_1\, s/\omega_1}{(1+s/\omega_1)(1+s/\omega_2)}, \quad \text{where:} \quad \begin{cases} A_1 = g_{m1}R_1 \\ \omega_1 \approx 1/(R_B C_B) \\ \omega_2 \approx 1/[R_1(C_{p1}+C_{p2})] \end{cases}. \tag{55}$$

$H(s)$ express the transfer function across the preamplifier, operating in class-A, loaded by the RC-bias tee. The small-signal circuit model of the preamplifier is also shown in Figure 16c. C_{p1} and C_{p2} represent the parasitic capacitive loading at internal nodes. The approximated expressions of $H(s)$, ω_1, and ω_2 are obtained considering $C_{p1}, C_{p2} \ll C_B$ and $R_1 \ll R_B$. Insofar, $\omega_1 \ll \omega_2$, and at intermediate frequencies the voltage gain is flat and determined by A_1. In the design case of [52], ω_2 is set to be $\times 60$ larger than ω_1. The step response at the input of the class-B amplifier can be found as follows:

$$V_{o1d}(t) \approx V_{o1d}(0^+)\left(e^{-\omega_2 t} - \frac{\omega_2}{\omega_1}\, e^{-\omega_1 t}\right). \tag{56}$$

The step response behavior is then determined by two components, these being the $e^{-\omega_1 t}$ term and the $e^{-\omega_2 t}$ term as the slow and the fast components, respectively. The slow response is, however, attenuated by the ratio $\omega_2/\omega_1 \gg 1$; hence, by design, its amplitude can be set below the activation threshold of the output transistors by choosing proper values of V_{BP} and V_{BN}. Thereby, only the fast component is processed by the PSRE.

The additional voltage required to activate the output transistors forms the basis of the deadzone mechanism, which is subsequently attenuated by the gain of the preamplifier. However, the preamplifier gain cannot be excessively high, as the input-referred deadzone needs to exceed the combined offsets of the main OTA and the PSRE. Failure to meet this condition would result in the system being unable to activate for neither positive nor negative input steps (Clearly, the width of the deadzone, or even its presence, is strongly affected by device mismatch. The latter can be expected to be large, since minimization of internal delays of the PSRE imposes the use of minimum length devices. This is a critical aspect of the PSRE that has to be addressed in the design phase by means of statistical analysis and/or Monte Carlo simulations).

4. Conclusions

In this review, we delved into the intricate landscape of slew-rate enhancement techniques for switched-capacitor amplifiers. A simplified settling model was introduced to provide a rational framework for understanding these advanced circuital techniques. Through this model, we elucidated the roles of small-signal and large-signal characteristics of amplifiers, shedding light on their influence on settling behavior.

Discussions were centered around power efficiency, particularly comparing single-stage and two-stage OTAs to offer practical guidelines for optimizing settling behavior under power constraints. An exhaustive review of state-of-the-art designs was conducted, initially using standard Figures of Merit regarding power efficiency. However, we also identified their scalability limits concerning the capacitive loading applied to amplifiers. A clear vision of the effectiveness of advanced slew-rate enhancer techniques is evident when considering the settling-time-based metrics. Based on this result, we introduced a novel Figure of Merit, which also takes into account the entity of the equivalent input step-like signal. This novel Figure of Merit allowed us to identify a design frontier, clearly illustrating the trade-offs between power efficiency and capacitive loading.

Finally, a detailed discussion at the transistor level of advanced circuit techniques was undertaken, revealing the strengths and weaknesses of each solution. By providing a comprehensive overview of these techniques and their implications, this review aims to guide future research in the field of switched-capacitor amplifier design.

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