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Review

Recent Progress of Non-Volatile Memory Devices Based on Two-Dimensional Materials

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Abstract: With the development of artificial intelligence and edge computing, the demand for high-performance non-volatile memory devices has been rapidly increasing. Two-dimensional materials have ultrathin bodies, ultra-flattened surfaces, and superior physics properties, and are promising to be used in non-volatile memory devices. Various kinds of advanced non-volatile memory devices with semiconductor, insulator, ferroelectric, magnetic, and phase-change two-dimensional materials have been investigated in recent years to promote performance enhancement and functionality extension. In this article, the recent advances in two-dimensional material-based non-volatile memory devices are reviewed. Performance criteria and strategies of high-performance two-dimensional non-volatile memory devices are analyzed. Two-dimensional non-volatile memory array structures and their applications in compute-in-memory architectures are discussed. Finally, a summary of this article and future outlooks of two-dimensional non-volatile memory device developments are given.

Keywords: non-volatile memory; random access memory; two-dimensional materials; compute-in-memory; in-memory sensing and computing

Citation: Pan, J.; Wang, Z.; Zhao, B.; Yin, J.; Guo, P.; Yang, Y.; Ren, T.-L. Recent Progress of Non-Volatile Memory Devices Based on Two-Dimensional Materials. *Chips* **2024**, *3*, 271–295. https://doi.org/10.3390/chips3040014

Academic Editors: Gianluca Giustolisi and Elisabetta Moisello

Received: 1 August 2024
Revised: 18 September 2024
Accepted: 19 September 2024
Published: 24 September 2024

1. Introduction

The advent of two-dimensional (2D) materials has been used in a new era of possibilities in the field of nanoelectronics, offering the prospect of revolutionary advances in device performance and miniaturization. These materials, including graphene, transition metal dichalcogenides (TMDs), and black phosphorus (BP), exhibit distinctive electrical characteristics that make them highly suitable for next-generation electronic devices [1]. Among the numerous potential applications, non-volatile memory (NVM) devices based on 2D materials have drawn significant interest due to their potential to transform data storage technologies.

NVMs are capable of retaining information without the need for an external power source. NVM devices based on traditional materials are constrained by limitations such as scalability issues. In contrast, 2D materials offer a promising alternative due to their atomic-thin structures and immunity to short-channel effects [2–4]. The fundamental principles of 2D NVM include charge trapping, ferroelectricity, magnetic, and phase-change, which enable efficient and reliable data storage [5–8].

The performance of 2D NVM is evaluated based on several criteria, including retention time, endurance, switching speed, energy consumption, etc. These performance metrics are critical for the practical implementation of 2D NVMs in modern electronics [9,10]. Recent studies have demonstrated performance improvements in 2D NVMs, promoting the applications of 2D NVMs in real cases.

For commonly used von Neumann architecture, the performance of electronics is limited by the data transition process between computing and memory units. To address

this issue, in-memory computing architectures have been developed in recent years. The integration of 2D NVM arrays for in-memory computing enables data processing directly within the memory units, thereby enhancing computational efficiency and facilitating in-memory sensing [11].

This paper reviews recent progress in NVM devices based on 2D materials. The principles of 2D NVMs are discussed, detailing the underlying mechanisms that enable their functionality. The performance criteria essential for evaluating these devices are examined, highlighting the advances in achieving superior memory characteristics. The applications of 2D NVM arrays for in-memory computing are explored. Finally, the conclusion of this paper and outlook of 2D NVMs for future development are provided.

2. Two-Dimensional Material Overviews

2.1. Two-Dimensional Semiconductor Materials

In recent decades, the discovery of transition metal dichalcogenides (TMDs, MX_2, where M denotes a transition metal element and X represents a chalcogen element) and other materials has led to the observation of remarkable electrical properties [12]. Two-dimensional semiconductor materials are amenable to large-scale growth, which allows them to have the potential to develop NVM arrays in integrated circuits [13].

Two-dimensional semiconductor materials are used for transistor channel materials, including molybdenum disulfide (MoS_2) [2], tungsten diselenide (WSe_2) [14], molybdenum ditelluride ($MoTe_2$) [15], etc. Transistor devices with 2D semiconductor channels have various structures, including single-gate structures [16], dual-gate structures [17], split-gate structures [18], etc. A typical structure of a 2D dual-gate transistor is shown in Figure 1a. Since the Schottky barrier between 2D materials and the contact metal is relatively large, the contact resistance is a critical issue that should be addressed to enhance the performance of 2D semiconductor devices. Many strategies have been investigated to reduce the contact barriers, including semimetallic bismuth contact [19], Yttrium doping [20], chemical synthesization and integration [21], etc. An example of a strategy to reduce the contact resistance is shown in Figure 1b, where UV/ozone treatment is conducted to the WSe_2 channel, and the Schottky barrier and contact resistance are reduced [22].

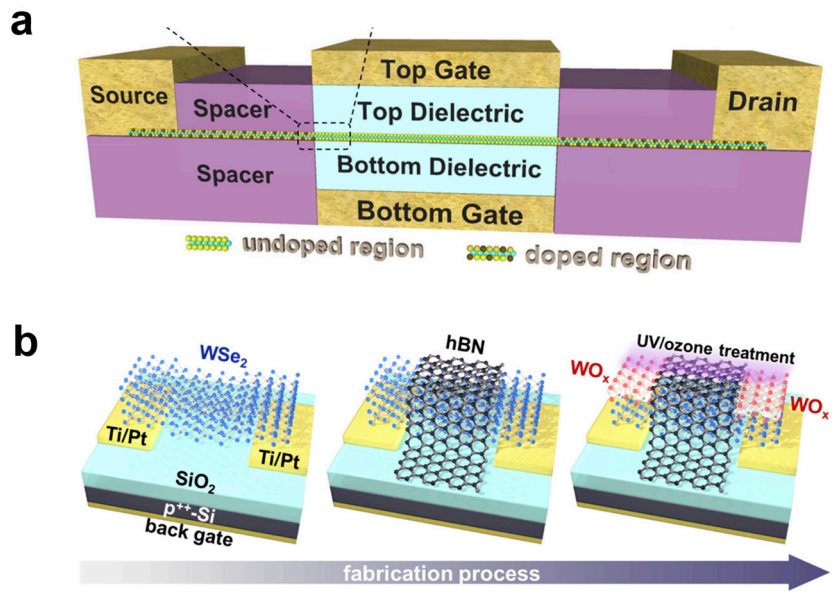


Figure 1. Devices based on 2D semiconductor materials: (**a**) A dual-gate 2D FET structure. Reproduced with permission [23], Copyright 2015, IEEE. (**b**) A 2D WSe_2-based FET with UV/ozone treatment. Reproduced with permission [22], Copyright 2021, American Chemical Society.

2.2. Two-Dimensional Insulator Materials

Hexagonal Boron Nitride (h-BN) is a commonly used 2D insulator material that has been investigated in recent years. Knobloch et al. evaluated the potential limitations of h-BN as an insulator in complementary metal-oxide-semiconductor (CMOS) devices based on 2D materials, emphasizing the challenges associated with leakage currents (Figure 2a) [24]. Many applications of h-BN have been discovered in recent years; Resistive Random Access Memory (RRAM) is one of the most popular candidates [25,26]. Yu-an et al. demonstrate the scalable ways to fabricate metal/h-BN/metal vertical memristors. These devices have been proven to have ultra-low power consumption that surpasses traditional memristors with HfO_x as the middle layer [26]. Afshari et al. manufactured a type of memristor using h-BN as it is a better option for switching layers compared to conventional oxide-based materials [25]. Their group have also been looking into hardware implementation on 2D h-BN memristor arrays. Dot-product computation and logistic regression have been verified to be applicable on devices with fantastic research data collected [27].

Apart from h-BN, some studies have focused on replacing old dielectric materials with new 2D insulator materials and trying to manufacture atomically thin layers as easily as possible. Zhao et al. value Bi_2O_2Se single-crystalline film as another kind of 2D insulator material and illustrate how to synthesize it. They further fabricated β-Bi_2SeO_5/Bi_2O_2Se heterostructures by leveraging large-scale UV-assisted intercalative oxidation (Figure 2b), realizing memristors with splendid self-rectifying resistive switching performance, ultrafast resistive switching, and low power consumption [28].

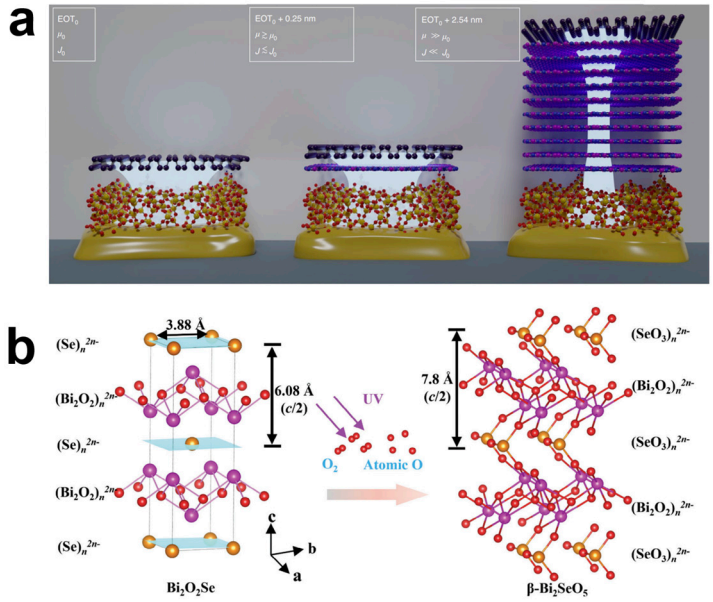


Figure 2. Properties of 2D insulator materials: (**a**) h-BN interlayers. Reproduced with permission [24], Copyright 2021, Springer Nature. (**b**) Unit cells of Bi_2O_2Se crystal and β-Bi_2SeO_5 crystal. Reproduced with permission [28], Copyright 2024, American Chemistry Society.

2.3. Two-Dimensional Ferroelectric Materials

Two-dimensional ferroelectric material is a kind of 2D material with the characteristic of spontaneous polarization, which means that electrical polarization can be spontaneously formed in the absence of an applied electric field [29]. Studies have been conducted to discover the atomic arrangement and charge distribution of 2D ferroelectric materials. Liu et al. identified monolayer γ-GeSe as a 2D ferroelectric material with out-of-plane polarization and demonstrated that it can acquire itinerant ferromagnetism upon hole doping, thereby illustrating the potential for the development of new materials with both ferroelectric properties [30]. Zhu et al. demonstrated that charge doping can effectively tune the ferroelectricity of 2D materials, thereby suggesting new possibilities for novel

ferroelectric devices [31]. Typical representatives such as In_2Se_3 and $CuInP_2S_6$ have already been proven to be an essential part of devices in future generations. Hou et al. examined the in-plane strain-modulated photoresponsivity of α-In_2Se_3, a 2D vdW ferroelectric semiconductor, underscoring the possibility of high-performance nanodevices based on 2D materials (Figure 3a) [32]. In a further illustration of the prospective utility of 2D ferroelectric materials, Li et al. presented an electronic synapse based on $CuInP_2S_6$, which could have considerable implications for the advancement of neuromorphic computing systems [33]. Li et al. reported an enhanced bulk photovoltaic effect in 2D ferroelectric $CuInP_2S_6$ and demonstrated a crossover from 2D to 2D bulk photovoltaic effect, indicating the potential application of ultrathin 2D ferroelectric materials in third-generation photovoltaic cells (Figure 3b) [34].

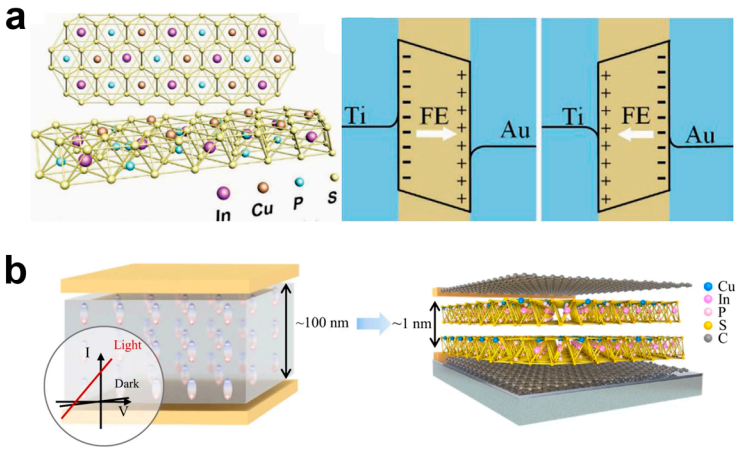


Figure 3. Electrical polarization inside 2D ferroelectric materials: (**a**) Diagram of 2D ferroelectric $CuInP_2S_6$ crystal and energy diagram for the $CuInP_2S_6$ diode. Reproduced with permission [32], Copyright 2020, Wiley-VCN. (**b**) Comparison of three-dimensional and two-dimensional bulk photovoltaic effect devices. Reproduced with permission [34], Copyright 2021, Springer Nature.

2.4. Two-Dimensional Magnetic Materials

Recent advancements in the field of 2D materials have paved the way for the exploration of novel magnetic phenomena and their applications in random access memory (MRAM) [35]. As early as 2017, 2D crystals including CrI_3 and $Cr_2Ge_2Te_6$ were observed to have magnetic properties (Figure 4a,b) [36–38]. These materials, with their well-defined layer thickness and atomically flat surfaces, allow for the manipulation of magnetic properties through electrical gating and strain engineering. Other 2D magnetic materials have also been gradually identified, such as Fe_3GeTe_2 [39]. The challenges of scalability [38], ambient stability [37], and Curie temperature [40] remain significant hurdles for the practical applications of 2D magnetic materials. With the continuous development of growth techniques and characterization methods, such as molecular beam epitaxy and scanning single-spin magnetometry, it is expected that these challenges will be overcome [36].

2.5. Two-Dimensional Phase-Change Materials

Great interest has been drawn to 2D phase-change materials. Two stable states of these materials can represent “0” and “1”, allowing them to be the crucial part of phase-change memory (PCM). Recent research has uncovered several 2D materials with phase-change behavior, such as InSeX (Figure 5a) [41]. InSeX can also be changed between crystalline and amorphous phases under a melt-quench-recrystallization mechanism [42]. TMD materials including molybdenum diselenide ($MoSe_2$), $MoTe_2$, and tungsten disulfide (WS_2) can undergo phase transitions (Figure 5b) [43]. Density functional theory (DFT) calculations have revealed that $MoTe_2$ can switch between semiconducting 2H and semimetallic 1T′ phases through mechanical strain, with the transition temperature and strain magnitude dependent on the material’s composition and the presence of adsorbed atoms or

molecules [44]. Vertical lamellar $MoSe_2$ films can undergo reversible phase transitions from the conducting 1T phase to the semiconducting 2H phase, facilitated by all-solid-state reversible intercalation of Cu cations [45].

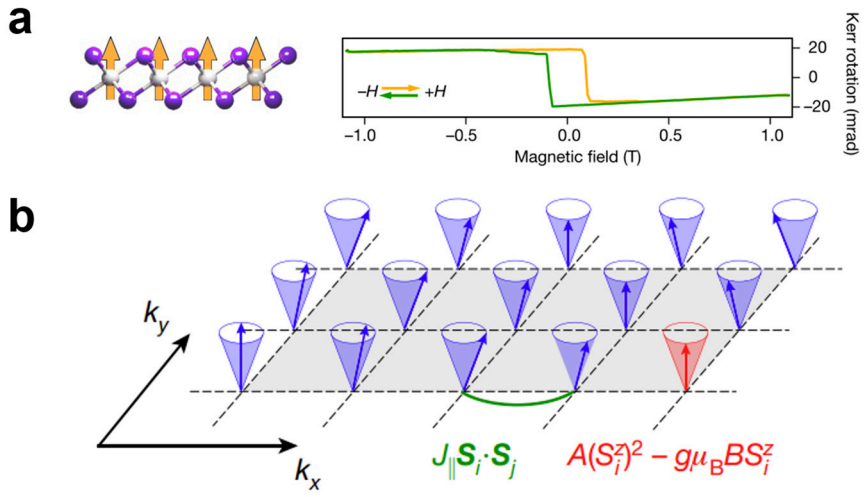


Figure 4. Structures and spin orientation of 2D magnetic materials: (**a**) Diagram of the CrI_3 structure noting the spin orientation and Kerr rotation signal of a thin bulk CrI_3 crystal generated by the magnetic field. Reproduced with permission [36], Copyright 2017, Springer Nature. (**b**) Ferromagnetic spin-wave oscillations in the two-dimensional material. Reproduced with permission [37], Copyright 2017, Springer Nature.

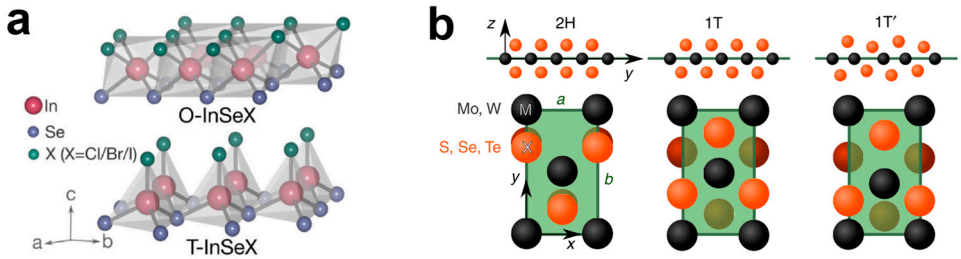


Figure 5. Structures of 2D phase-change materials: (**a**) Diagram of O-InSeX and T-InSeX (X=Cl, Br, I). Reproduced with permission [41], Copyright 2023, Elsevier Ltd. (**b**) Diagram of three crystalline phases of 2D group VI TMDs. Reproduced with permission [43], Copyright 2014, Springer Nature.

3. Two-Dimensional Non-Volatile Memory Principles

3.1. Two-Dimensional Resistive Random Access Memory

Two-dimensional resistive random access memory (RRAM) is a type of non-volatile memory with resistance switching behavior. Two-dimensional RRAM has attracted considerable interest within the field of next-generation non-volatile memory research. Many researchers focus on resistive switching behavior and try to improve the speed of 2D RRAM. Zhang et al. demonstrated an electric-field-induced structural transition in vertical $MoTe_2$- and $Mo_{1-x}W_xTe_2$-based RRAM devices, showcasing reproducible resistive switching within 10 ns (Figure 6a) [46]. Tang et al. emphasized the importance of 2D semiconductors in modulating switching characteristics through sulfur vacancy diffusion for the development of high-density and reliable RRAMs for memory-based computing (Figure 6b) [47].

Apart from a single RRAM device, the integration of 2D RRAM and transistors is investigated. Sivan et al. introduced a hybrid integration of 2D material-based 1T1R RRAM cells, combining WSe_2 p-field-effect transistors (p-FETs) with solution-processed WSe_2 RRAMs [48]. The low-temperature co-integration process yielded enhanced performance and reduced switching energy. Yang et al. integrated molybdenum disulfide transistors with metal-oxide RRAM to create 2T2R ternary content-addressable memory (TCAM) cells

for parallel data search applications (Figure 6c) [49]. These cells exhibited comparable resistance ratios to commercial TCAMs while reducing the transistor count and eliminating standby power consumption.

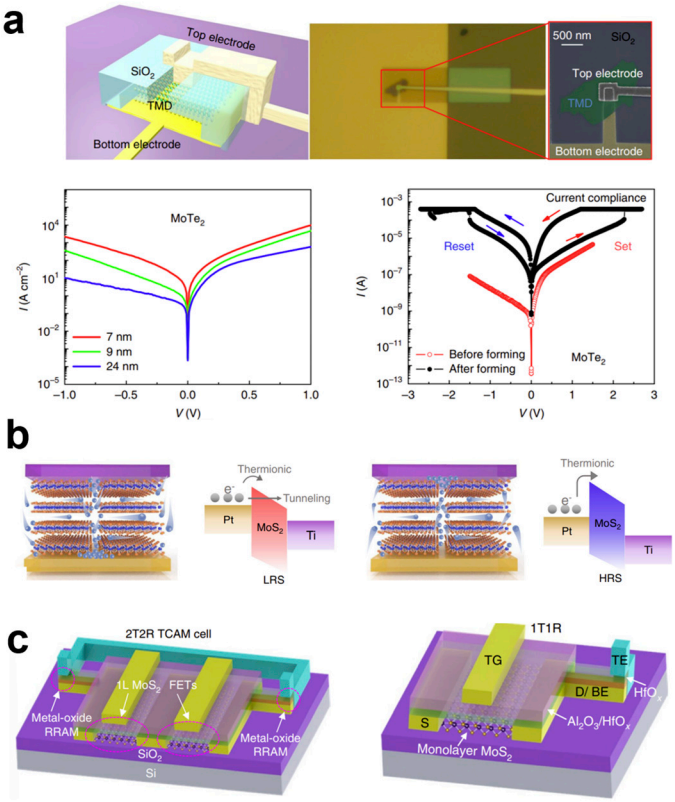


Figure 6. Schematics of state-of-the-art 2D RRAM: (**a**) Vertical $MoTe_2$- and $Mo_{1-x}W_xTe_2$-based resistive memory. Reproduced with permission [46], Copyright 2019, Springer Nature. (**b**) Diagrams of the set/reset processes. Reproduced with permission [47], Copyright 2019, Springer Nature. (**c**) Schematics of the 2T2R and 1T1R structures based on MoS2 FETs and HfO_x-based RRAMs. Reproduced with permission [49], Copyright 2022, Springer Nature.

3.2. Two-Dimensional Ferroelectric Memories

The potential of ferroelectric memories for non-volatile storage and compatibility with integrated circuits has attracted the attention of researchers. Devices have been designed and illustrated through experiments in recent years. Wang et al. reported a 2D α-In_2Se_3 ferroelectric semiconductor channel device, and demonstrated its functions on non-volatile memory and neural computation [6]. Shen et al. put forth the concept of doping engineering in a 2D ferroelectric tunnel junction as a means of achieving a low thickness [50]. Luo et al. investigated the potential of dual-ferroelectric-coupling-engineered 2D transistors for in-memory computing, combining non-volatile logic gates and artificial synapses (Figure 7b) [51]. Jiang et al. devised an asymmetric ferroelectric-gated 2D transistor with self-rectifying photoelectric memory and artificial synapse functionality (Figure 7b) [52]. Kim et al. presented a scalable CMOS back-end-of-line-compatible AlScN/2D channel ferroelectric field-effect transistor, showcasing stable retention and endurance features suitable for integration with silicon complementary metal-oxide-semiconductor logic [53].

3.3. Two-Dimensional Magnetic Random Access Memory

Apart from RRAM and FeRAM, magnetic random access memory (MRAM) has also become a solution to the performance bottleneck. Two-dimensional magnetic vdW crystals are shown in Figure 8a [38]. The atomically thin crystalline materials exhibit magneto-optic and magnetoelectric effects. 2D magnetic crystals, including 2D ferromagnets and

2D antiferromagnets with various intra- and inter-plane magnetic configurations, can display a wide range of magneto-optic and magnetoelectric phenomena. Through spin-transfer torque (STT), spin–orbit torque (SOT), and other sorts of writing methods, the spin state of magnetic 2D materials can be shifted, which means that data stored inside 2D MRAM can be programmed (Figure 8b) [54]. Many studies are conducted to realize programming at room temperature. Wang et al. demonstrate the room-temperature magnetization switching driven by SOT in a full vdW heterostructure by an optimized epitaxial growth method [55]. Pan et al. reported all-2D magnetoresistive memory devices based on $WTe_2/Fe_3GaTe_2/BN/Fe_3GaTe_2$ heterostructure, which can read and write data through the orbit-transfer torque (OTT) effect at room temperature [56].

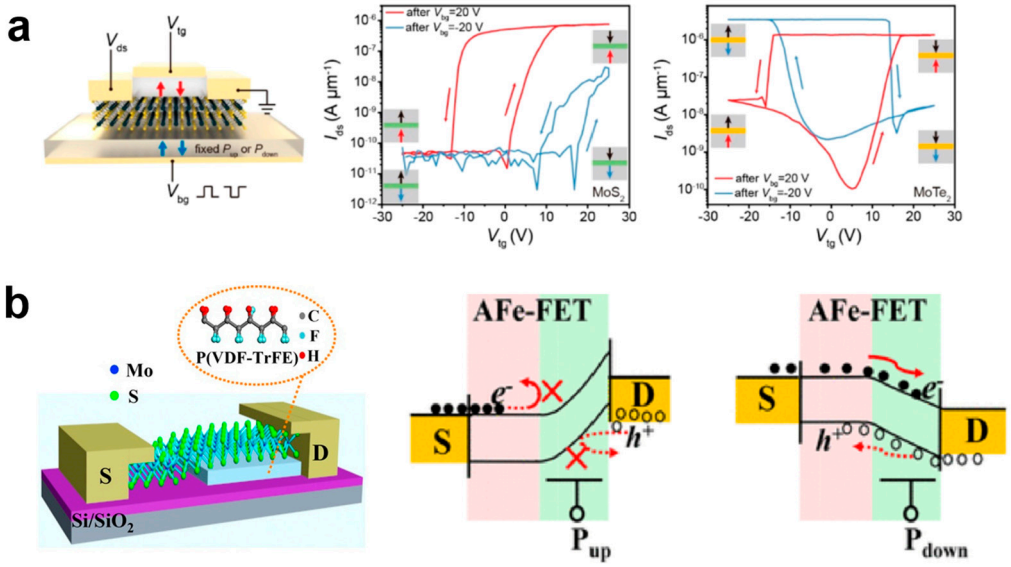


Figure 7. Schematic of state-of-the-art 2D FRAM: (**a**) A dual-gate 2D FeFET controlled by independent TG and BG voltage. Reproduced with permission [51], Copyright 2022, American Chemical Society. (**b**) An asymmetric ferroelectric-gated 2D transistor. Reproduced with permission [52], Copyright 2022, American Chemical Society.

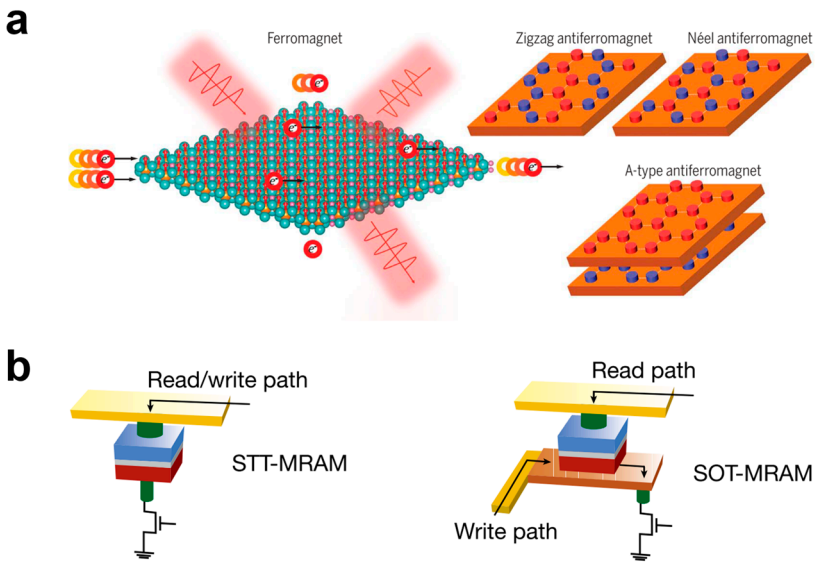


Figure 8. Two-dimensional MRAM materials and typical writing method: (**a**) Diagram of 2D magnetic crystals. Reproduced with permission [38], Copyright 2019, American Association for the Advancement of Science. (**b**) Schematics of STT-MRAM and SOT-MRAM. Reproduced with permission [54], Copyright 2022, Springer Nature.

3.4. Two-Dimensional Phase-Change Memories

Both the choice of phase transition mechanism and device structure significantly impact the performance and functionality of 2D phase-change memory (PCM). The foundation of PCRAM lies in the reversible phase transitions between amorphous and crystalline states of chalcogenide materials. Two-dimensional vdW TMDs are promising to be used for PCM (Figure 9) [57]. These materials exhibit tunable electronic properties and the ability to achieve moderate phase-change temperatures. The unique properties of 2D vdW TMDs, including their ultra-low melting point and high crystallization temperature, make them attractive candidates for advanced PCRAM applications [57–59]. The field of phase-change memory is rapidly advancing, with innovative materials and device architectures pointing to exciting directions for the future development of highly reliable non-volatile memory solutions. These advancements open doors for new applications in data storage, neuromorphic computing, and beyond.

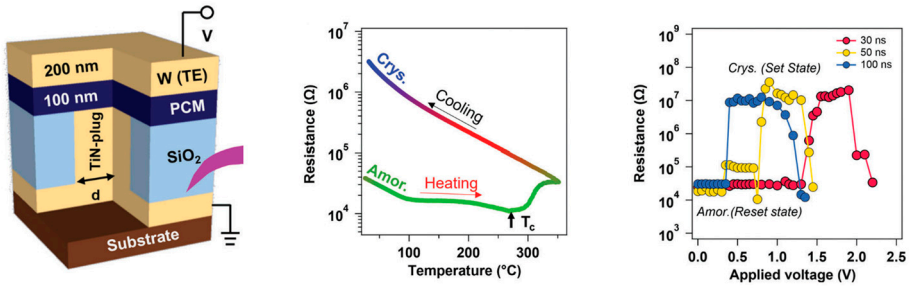


Figure 9. Schematic of a cross-section of the phase-change memory device. Temperature dependence of the sheet resistance of a $NbTe_4$ thin film, measured at a heating rate of approximately 15 °C/min. Resistance as a function of applied voltage pulse in a NbTe4-based memory cell, with fixed pulse widths of 30, 50, and 100 ns. Reproduced with permission [57], Copyright 2023, Wiley-VCN.

3.5. Two-Dimensional Floating Gate Memories

Floating gate memory utilizes a floating gate to store charge, enabling the retention of data even in the absence of supply. The atomic-scale thickness, absence of dangling bonds, and enhanced electrostatic control of 2D materials create interfaces free from trapped charges, enhancing the performance of floating gate memory devices [60]. The utilization of 2D materials as the channel of floating gate memories, such as TMDs like MoS_2 and WSe_2, offers several key advantages for floating gate memory development.

Research efforts have focused on utilizing various 2D material heterostructures to construct floating gate memory devices. Researchers have presented MoS_2/BN/graphene heterostructure-based floating gate memory and demonstrated outstanding non-volatile memory characteristics [61–63]. The device presented by Li et al. simulates basic synaptic functions and achieves high recognition accuracy in handwritten numeral recognition tasks (Figure 10a) [63]. Li et al. explore a graphene-BP/h-BN/graphene heterostructure-based floating gate memory with ambipolar characteristics, allowing it to act as a diode and exhibit reverse rectifying behavior [64]. This heterojunction offers dual-mode non-volatile memory functionality and can be utilized in memory inverter circuits and logic rectifiers. Zha et al. demonstrate a Te-based floating gate memory with MoS_2 channel that exhibits non-volatile electronic memory behaviors under intense electrical/optical stimuli with 10^8 extinction ratio, 100 ns switching speed, more than 4000 cycle endurance, and 4000 s retention time (Figure 10b) [65]. This demonstrates the potential of 2D floating gate memory technology for building computing systems with stable data storage.

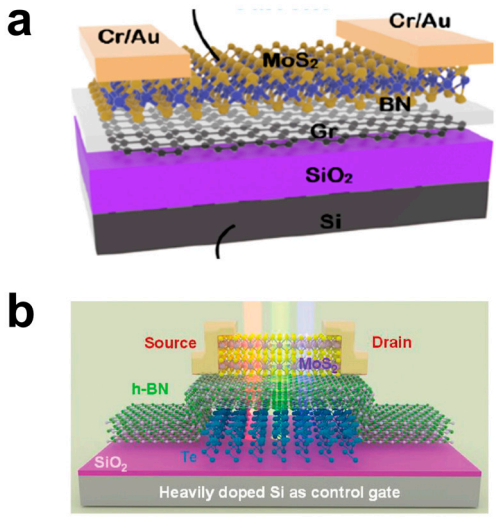


Figure 10. Schematics of floating gate memories: (**a**) Diagram of a 2D floating gate memory device based on MoS_2/h-BN/graphene structure. Reproduced with permission [63], Copyright 2024, American Chemical Society. (**b**) Diagram of a floating gate memory device with the ability to sense red, green, and blue light signal. Reproduced with permission [65], Copyright 2023, Wiley-VCH.

4. Performance Criteria for Two-Dimensional Non-Volatile Memories

For the performance criteria for 2D NVMs, the specifications during the operations of each single device and performance in system-level architectures need to be considered. Power consumption evaluates the energy efficiency, and data processing speed determines the maximum working frequency. For memory switching cycles, a large switching ratio and high endurance are expected so that the device can work for many cycles. Multi-level NVMs have been developed in recent years to extend the information storage capacity compared to binary memories. Memories with high retention are needed for long-term data storage without refreshments, and low variations are required for stable values in different cycles and different devices. Most application systems of NVMs are implemented by memory arrays, so integration levels with multiple devices are considered for system-level implementations. This section discusses some of the performance criteria that have been mentioned before and analyzes the works that have achieved high performance in recent years. Summary of recently developed 2D NVMs are listed in Table 1.

Table 1. Summary of typical two-dimensional non-volatile memory devices.

Ref.	Material	Type	Energy	Speed	Retention	Endurance	Variations	Integration
[66]	h-BN	Resistive switching device	–	200 ns	–	$>2 \times 10^3$	Cycle-to-cycle variation of 1.53% Device-to-device variation of 5.74%	High yield of 98% High density of 150 nm × 150 nm
[11]	MoS_2, WSe_2/h-BN	Resistive switching device	–	–	~10^2 s	$>10^3$	–	Monolithic 3D integration
[67]	h-BN	Resistive switching device	2 pJ	120 ps	~10^8 s	6×10^2	–	–
[6]	α-In_2Se_3	Ferroelectric device	40−234 fJ	40 ns	~10^3 s	5×10^2	–	–
[68]	MoS_2/HZO	Ferroelectric device	22.7 fJ bit^{-1} μm^{-2}	4.8 ns	~10^8 s	$>10^{13}$	Device-to-device variation of 19%	Two-layer crossbar arrays
[69]	Parallel-stacked bilayer BN	Ferroelectric device	–	<1 ns	~10^6 s	$>10^{11}$	–	–
[70]	MoS_2 channel with HfO_2/Pt/HfO_2 or Al_2O_3/Pt/Al_2O_3	Floating gate device	–	~20 ns	~10^8 s	$>10^5$	–	Integration of 1024 devices with yield of 98%

Table 1. *Cont.*

Ref.	Material	Type	Energy	Speed	Retention	Endurance	Variations	Integration
[71]	MoS_2/h-BN /graphene	Floating gate device	18 fJ	40 ns	~10^4 s	>10^5	Cycle-to-cycle variation: conduction difference ΔG < 0.1 nS	–
[72]	BP/Al_2O_3/BP	Floating gate device	<1 fJ	10 ns	–	5×10^3	–	–

4.1. Energy Consumption

Energy consumption is a crucial performance criterion for integrated circuit chips, especially for edge computing scenarios, including automatic driving vehicles, wearable electronics, and the Internet of Things, as energy supply is limited in those scenarios [73,74]. NVMs are promising for low-power devices, since the energy loss for maintaining the stored data is saved, compared to volatile memories like static random access memory (SRAM) and dynamic random access memory (DRAM) that need consistent voltage supply or data retention operations. Strategies for decreasing energy consumption have been developed recently based on the properties of two-dimensional materials.

Most energy loss of NVMs is from the write and read processes. For RRAM devices, large currents (typically larger than 10 μA) should go through the devices during write and read processes to ensure non-volatile data set behavior. Jian et al. analyzed the effect of the interstice radius between van der Waals (vdW) layers on reducing the driving force for the formation of RRAM conductive filaments, and proposed an ultra-low set power (10^{-10} W) and high switching ratio (10^6) RRAM with a 2D SnS_2 layer based on the large vdW interstice radius of the SnS_2-based structure (Figure 11a) [75]. Two-dimensional insulators including h-BN have superior performance for low-power RRAMs. Kang et al. developed a He^+ implanted h-BN RRAM and obtained sub-pW power consumption with a 10^8 switching ratio by defect implanting engineering [76]. Low-power two-dimensional floating memory devices have also been developed in recent years. Tang et al. developed an all-2D van der Waals materials artificial synapse with a MoS2 channel, h-BN oxide, and graphene floating gate, and achieved energy-efficient memory switching of 18 fJ for a single pulse [71]. Xiong et al. proposed a floating gate device with a BP/Al2O3/BP structure and flexible substrate (Figure 11b) [72]. This device can be operated in ~10 ns pulses and has low energy consumption of less than 1 fJ per spike.

4.2. Data Processing Speed

Due to the state switching properties, many NVM devices have relatively larger set and reset time than volatile memories like SRAM and DRAM, which have less than 10 ns access time [77]. Since 2D material architectures are developed later than other material architectures, the data processing speed of 2D NVMs is a critical issue to be addressed for wider applications for next-generation memory devices.

Two-dimensional floating gate memories are promising for fast NVM devices. vdW heterojunctions of 2D materials have superior properties such as atomically sharp interfaces that facilitate the write and read speed of floating gate memories [78–80]. Wang et al. reported a semi-floating-gate-controlled lateral homojunction structure made of 2D vdW heterostructures with an ultra-fast programming time of about 20 ns for floating memory applications (Figure 12a) [81]. This design is 10^7 times faster than other 2D homojunctions and can be used to perform in-memory logic operations. An ultra-fast 2D floating memory with 20 ns programming time, multi-bit storage capacity, and more than 10 years of data retention based on MoS_2/h-BN/MLG/h-BN/MLG vdW heterostructures was also developed later [82]. Ferroelectric memory devices can achieve fast programming speed by means of replacing normal channel materials with 2D ferroelectric semiconductors that have inherent out-of-plane and in-plane polarization directions [83]. Wang et al. developed a 2D ferroelectric α-In_2Se_3 memory device for NVM applications and neuromorphic computing

(Figure 12b) [6]. The programming time is only 40 ns with large hysteresis windows and data retention. Two-dimensional RRAMs can achieve much higher data processing speed, due to the fast state switching of atomic thick layer of 2D insulators. Nibhanupudi et al. proposed a 120 ps switching speed memristor device based on atomically thin sheets of 2D h-BN, which can be set by ultra-short (120 ps–3 ns) voltage pulses (Figure 12c) [67]. The ultra-fast 2D memristor reaches the speed of state-of-the-art volatile memories and is promising for fast data processing scenarios.

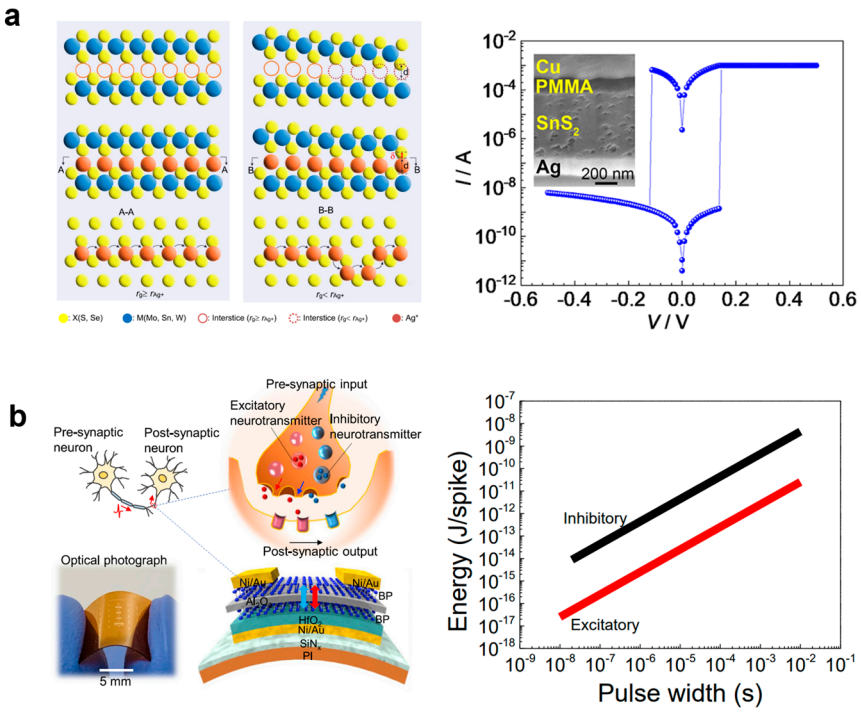


Figure 11. Low-power NVMs: (**a**) Low-power RRAM device based on the large vdW interstice radius of the 2D SnS_2 structure. Reproduced with permission [75], Copyright 2022, American Chemical Society. (**b**) Energy-efficient 2D floating gate memory device based on $BP/Al_2O_3/BP$ heterostructure with flexible substrate. Reproduced with permission [72], Copyright 2022, Elsevier.

4.3. Retention

Retention is to evaluate the duration of the device state that can persist without significant degradation or relaxation [9]. A high retention means that the memory device can store the information without refreshing for a long time. A stable value of the NVM device with negligible time decay is necessary for long-term memories and in-memory computing. Among different types of 2D NVMs, 2D ferroelectric memories have the potential to develop high-retention NVM devices. Xiang et al. fabricated a ferroelectric transistor based on a MoS_2 channel and ferroelectric HfO_2 ($Hf_{0.5}Zr_{0.5}O_2$, HZO) oxide for neuromorphic computing (Figure 13a) [84]. An ultralong retention of at least 10 years was achieved. Ning et al. developed a duplex two-dimensional material structure with HfO_2 and HZO oxide layers and a monolayer MoS_2 channel to construct an in situ learning in-memory computing architecture, and more than 10 years of retention was achieved [68].

Other than developing long-retention memory devices, memory devices with short retention have also been investigated and applied to various scenarios. Sun et al. fabricated SnS-based two-dimensional memristors for language recognition [85]. Due to charge trapping and photogating effects, short-term conduction state retention is achieved by both electrical and optical stimuli. Chen et al. developed optoelectronic graded neurons based on MoS_2 charge-trapping transistors (Figure 13b) [86]. The charge trapping at the interface between the MoS_2 channel and oxide enables the device to have short-term retention, and an in-sensor motion perception system is constructed.

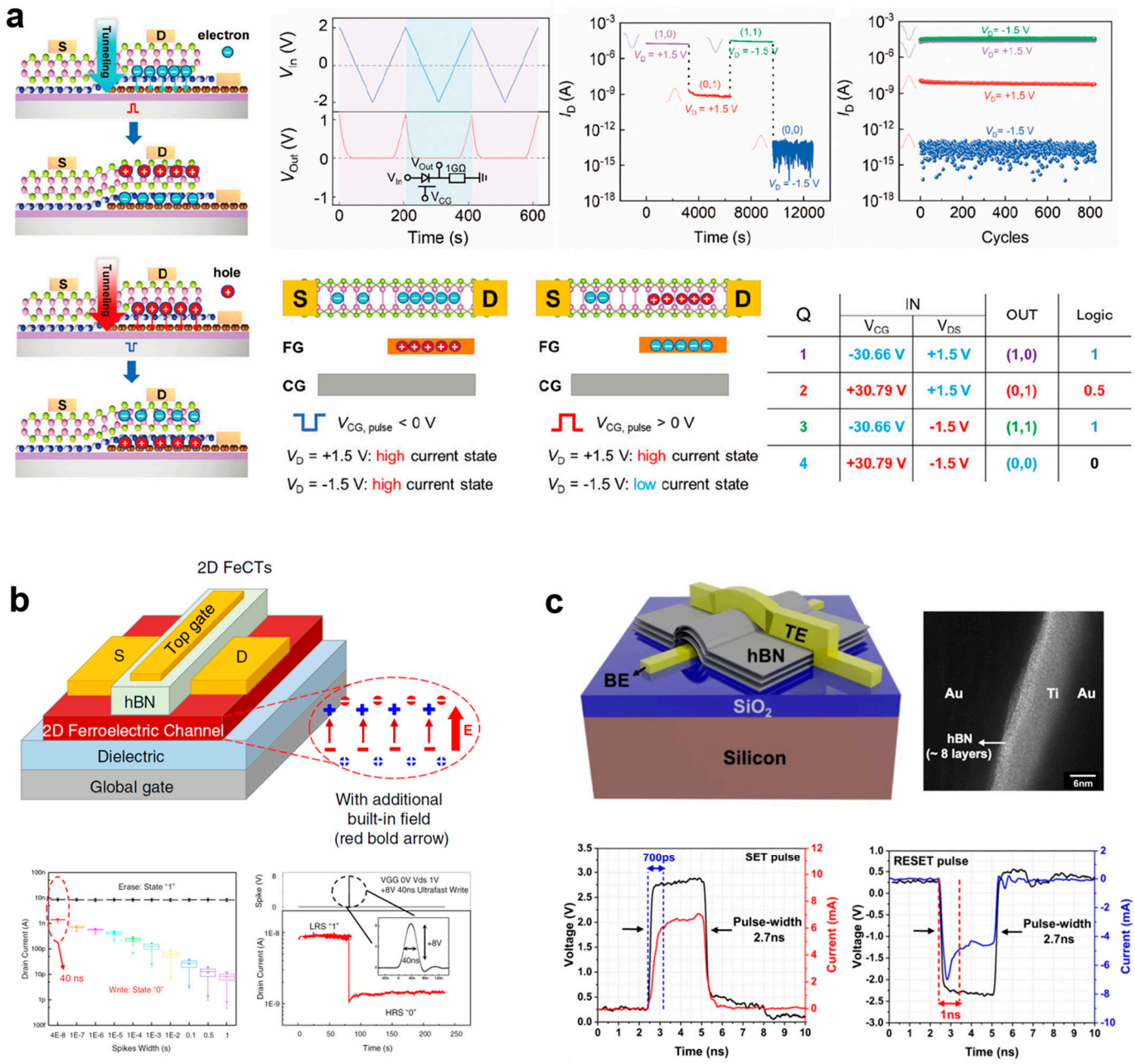


Figure 12. High-speed NVMs: (**a**) Ultrafast programmable floating-gate-controlled structure for non-volatile switching and in-memory logic computing. Reproduced with permission [81], Copyright 2023, Wiley-VCH. (**b**) Two-dimensional α-In_2Se_3 memory device with high-speed ferroelectric switching. Reproduced with permission [6], Copyright 2021, Springer Nature. (**c**) Atomically thin 2D h-BN-based memristor with 120 ps switching speed. Reproduced with permission [67], Copyright 2024, Springer Nature.

4.4. Endurance

Endurance means the ability of an NVM device to undergo a certain number of cycles while the state of the device remains stable. Endurance is quantified by the maximum number of writing cycles. In real applications, memory devices are required to keep stable after several rounds of data updates. In edge computing scenarios, when in situ learning of neural networks is required, the weights of neural networks are updated many times during the iterations of learning processes, and memory cells should be stable during the weight update.

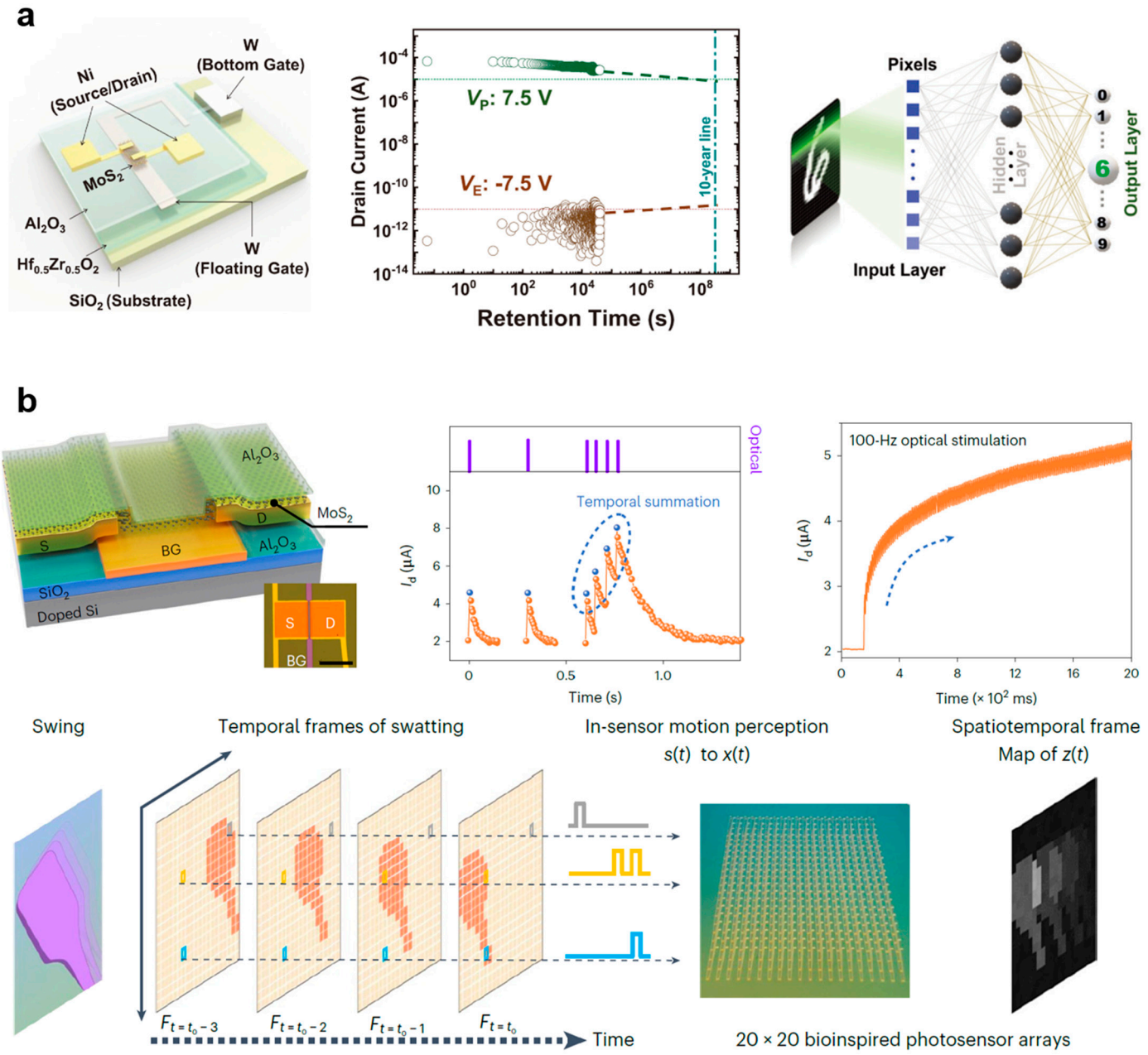


Figure 13. NVMs considering the retention performance: (**a**) A long-term retention ferroelectric transistor for neuromorphic computing. Reproduced with permission [84], Copyright 2023, Wiley-VCH. (**b**) A short-term retention 2D charge-trapping transistor for motion perception [86], Copyright 2023, Springer Nature.

Floating gate devices are commonly used for high-endurance devices. Two-dimensional floating gate devices are developed and exhibit large endurance. Jiang et al. proposed a scalable integration process for ultrafast 2D floating gate memory devices based on MoS_2 channels with $HfO_2/Pt/HfO_2$ and $Al_2O_3/Pt/Al_2O_3$ memory stack (Figure 14a) [70]. A large endurance of more than 10^5 is exhibited in this structure. Other than 2D floating gate memories, 2D ferroelectric memories have been investigated in recent years to enhance endurance by developing high-performance 2D materials and advanced nanostructures. Sliding ferroelectricity is reported to have extremely large endurance, and sliding ferroelectric devices have been investigated recently [87]. Yasuda et al. reported a high-endurance sliding ferroelectric memory device with monolayer graphene and parallel-stacked bilayer

BN (Figure 14b) [69]. This device exhibits ultrafast switching speeds on the nanosecond scale and high endurance exceeding 10^{11} switching cycles.

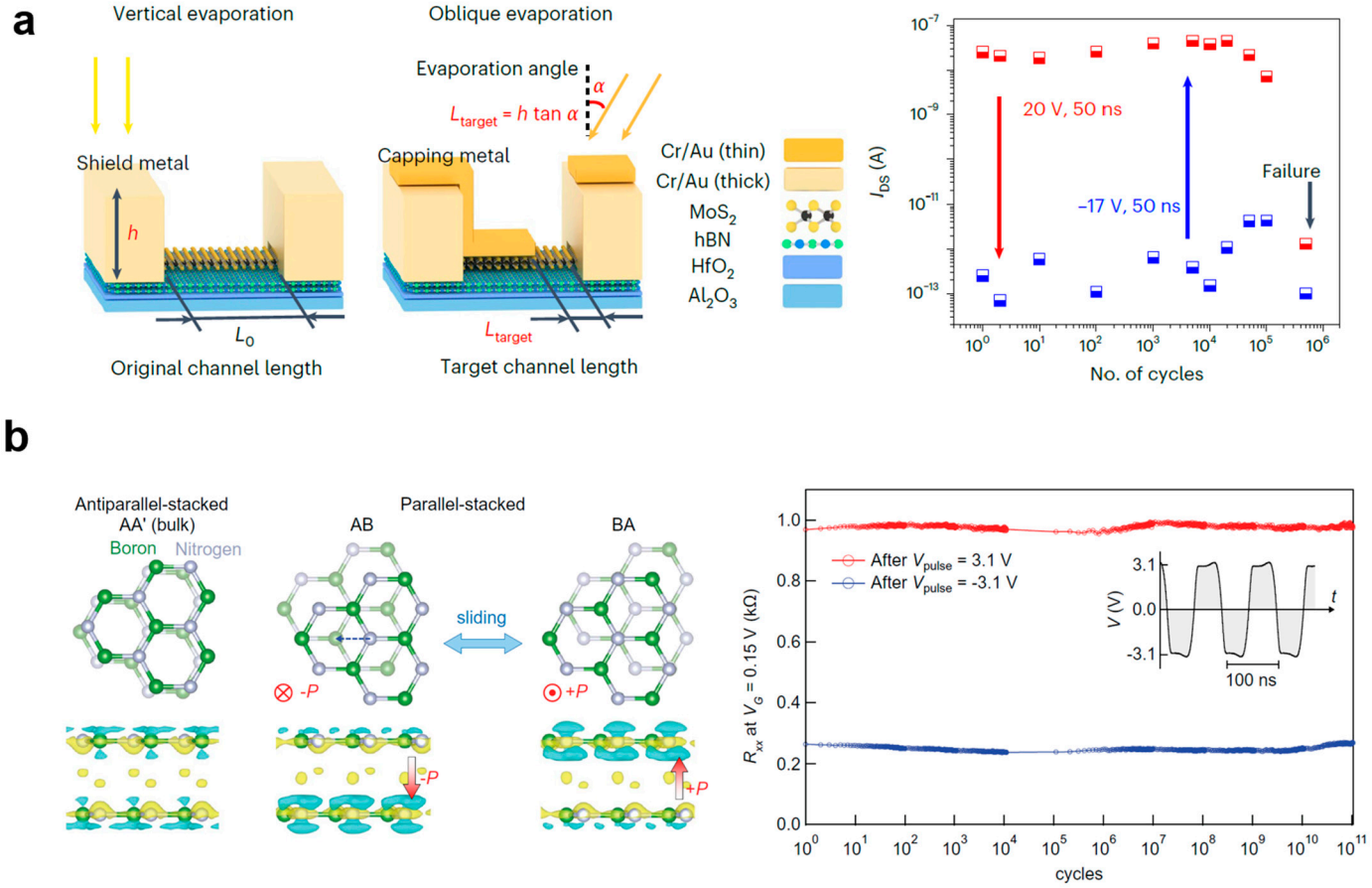


Figure 14. High-endurance NVMs: (**a**) A 2D floating gate memory device with MoS_2 channel exhibiting more than 10^5 cycle endurance. Reproduced with permission [70], Copyright 2024, Springer Nature. (**b**) A high-endurance 2D sliding ferroelectric memory device with high endurance exceeding 10^{11} switching cycles. Reproduced with permission [69], Copyright 2024, American Association for the Advancement of Science.

4.5. Variations

Cycle-to-cycle variation is a significant criterion to evaluate the value variations of a memory device in different data writing cycles. Low cycle-to-cycle variation is required for the high accuracy of weight update in NVM-based artificial neural networks (ANNs) with variable weights. Device-to-device variation is a critical specification for NVM arrays with multiple devices. Different devices in an NVM array need to have low enough value variations.

Low cycle-to-cycle and device-to-device variations of 2D NVMs can be achieved by high-quality growth of 2D materials and fabrication processes that have little effect on the material performance. Memory device structures with small feature sizes and high densities have the potential to be fabricated as NVM arrays with low variations; 1R RRAM arrays have the theoretical minimum feature size, i.e., $4F^2$ (F is the footprint), which results in their high density. Chen et al. developed high-density memristive crossbar arrays for artificial neural networks. The resistive switching medium is a chemical-vapour-deposited (CVD) multilayer h-BN with small sizes of 150 nm × 150 nm for each memristor cell (Figure 15a) [66]. The h-BN layer has high conformity, and ultralow variations of the device are achieved, i.e., 1.53% cycle-to-cycle variation and 5.74% device-to-device variation.

Apart from ANNs that require low enough cycle-to-cycle and device-to-device variations, some of the other computing architectures utilize the variations of devices and data

writing cycles, and are more tolerant of variations. For example, due to the cycle-to-cycle variation, the intrinsic probability distribution of the stored values of a non-volatile memory device after data writing that approximates Gaussian distribution can be used to construct Bayesian neural networks (BNNs) [88]. Zheng et al. proposed a two-dimensional memtransistor-based BNN (Figure 15b) [89]. The BN architecture is composed of 29 devices and has a low energy cost of about 1.2 nJ. Device-to-device variations can be used in reservoir computing (RC) systems. The device-to-device variation can expand the reservoir size and improve the system's performance [90]. The defects in 2D material interfaces can be utilized to generate device-to-device variation, and 2D RC systems have been developed in recent years to perform recurrent artificial intelligent computing with reduced hardware costs [85].

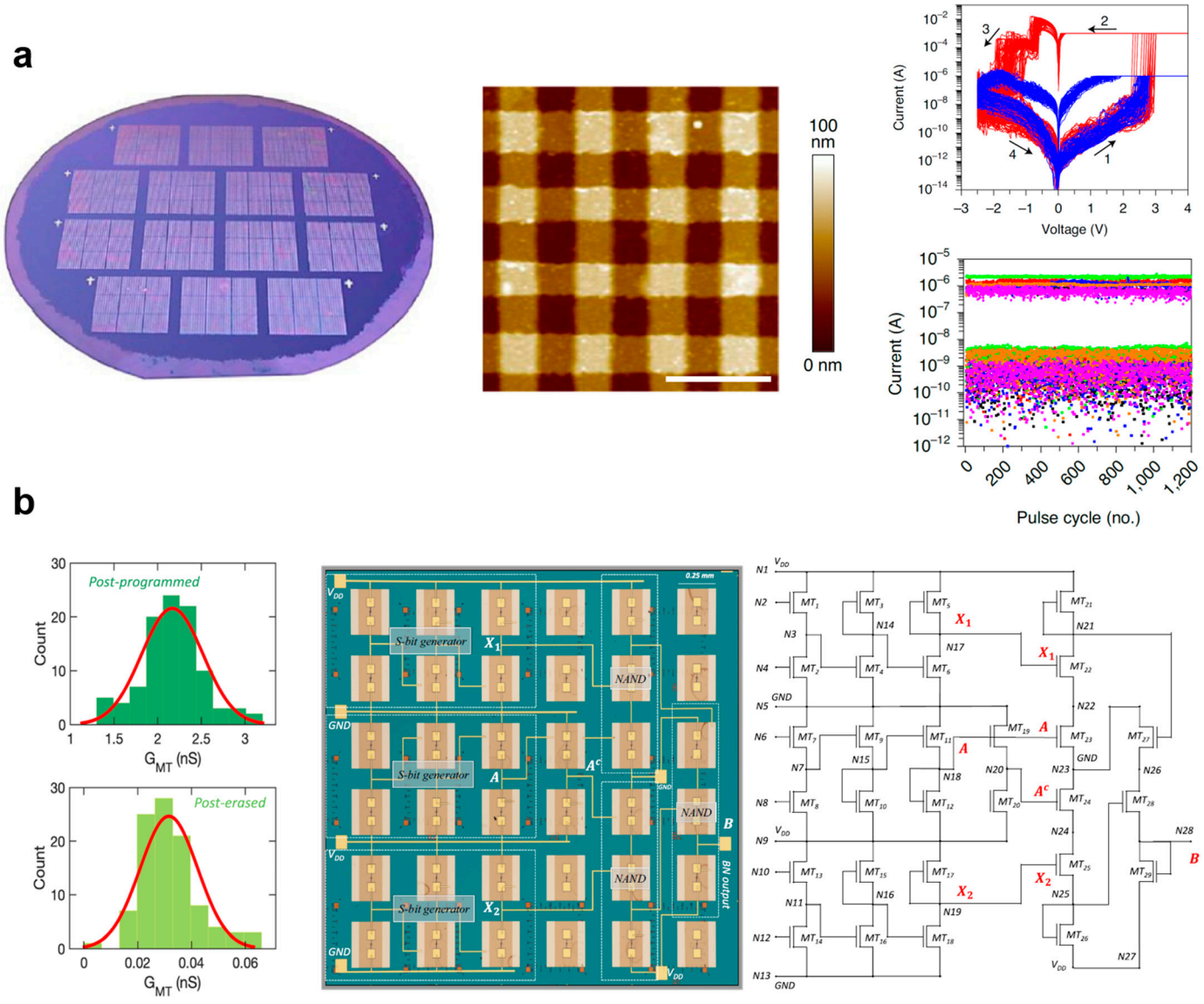


Figure 15. NVMs considering the variation performance: (**a**) A low-variation NVM based on high-density h-BN array. Reproduced with permission [66], Copyright 2020, Springer Nature. (**b**) A hardware-implemented 2D Bayesian neural network that utilizes the large variations of the device. Reproduced with permission [89], Copyright 2022, Springer Nature.

4.6. Integration

NVM devices should be integrated as multiple device-based functional systems and large-scale memory arrays to have the potential as memory devices in real cases. The polarization reconfigurable property of ferroelectric materials can be used to program the

junction distribution of 2D material transistors and construct reconfigurable device systems and in-memory logic computing architectures. Tong et al. reported a WSe_2-on-lithium niobate (LNO) cascaded architecture and showed the reconfigurable functions of the architecture for nonlinear transistor and NVM cells (Figure 16a) [91]. An operational amplifier based on multiple devices is also fabricated and verified. This work envisions the perspective of ferroelectric proximity effect-based 2D FeFETs on promoting module integration. Ferroelectrics can also be used for weight programming for in-sensor computing systems. Wu et al. reported ferroelectric-defined reconfigurable homojunctions and fabricated an array for in-memory sensing and computing applications [92].

Designs of NVM devices need to be compatible with the present integrated circuit technology. A promising strategy of 2D NVM integration is hybrid 2D-CMOS architecture, where circuits and units by CMOS devices are fabricated front-end-of-line, and fabrication processes for 2D NVM devices that are relatively newly developed and sensitive to process fluctuation are conducted on the top of CMOS device arrays. This back-end-of-line integration of 2D NVMs exhibits high performance. Zhu et al. reported a hybrid 2D–CMOS chip with 2D h-BN memristor and CMOS circuits for spiking neural networks (SNNs) (Figure 16b) [93]. Integrated hybrid 2D–CMOS systems are fabricated on a 200 mm wafer with memristor cells as small as 0.053 μm^2. Two-dimensional NVMs can also be compatible with advanced 3D integration technology to enable large integration levels [94]. Kang et al. developed a monolithic 3D integration of 2D material memristor arrays (Figure 16c) [11]. The WSe_2/h-BN memristors and MoS_2 transistors are all made of 2D materials. The 3D integrated array based on 2D materials reveals an innovative design of next-generation high-density memory chips. Also, Park et al. reported lateral gated ferroelectric transistor arrays based on 2D α-In_2Se_3 and demonstrated 3D integration of ferroelectric arrays [95].

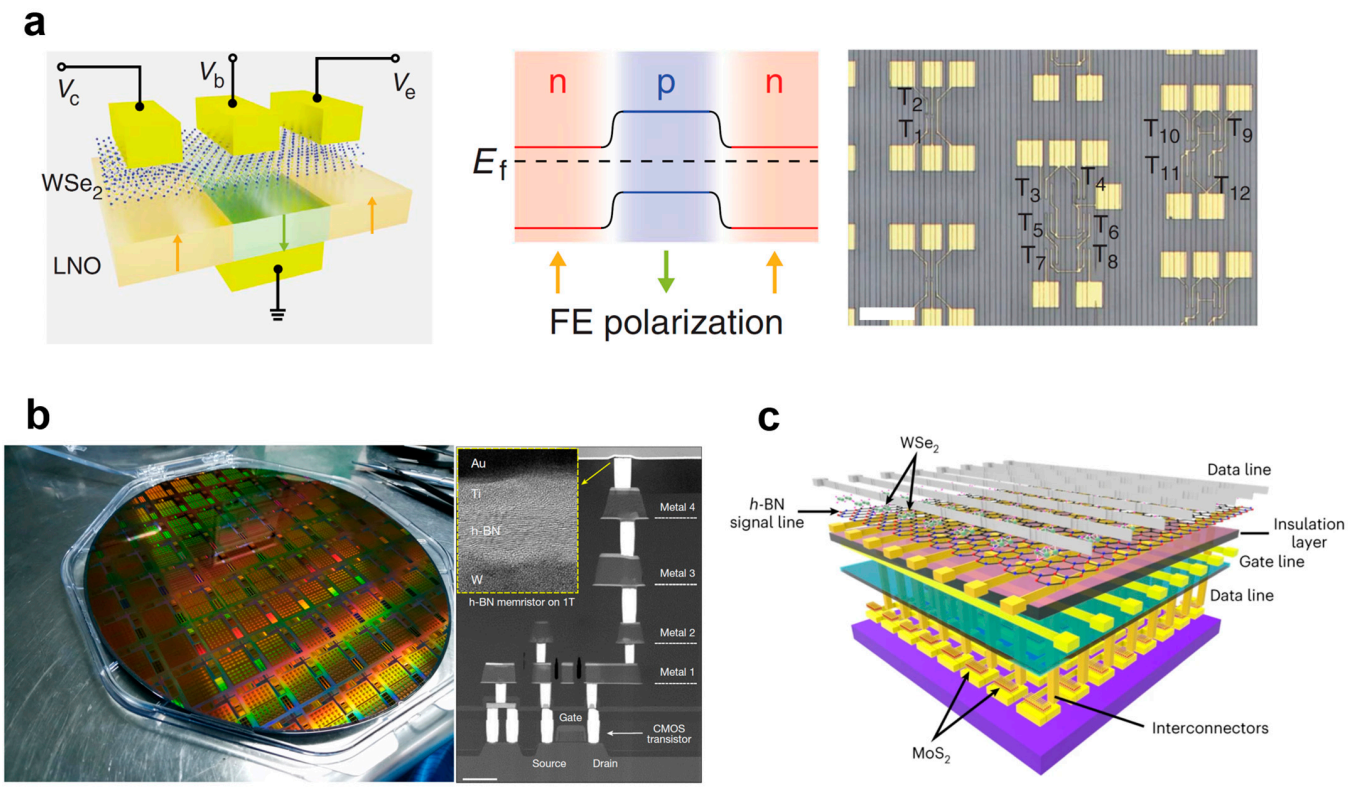


Figure 16. Integration of NVMs: (**a**) WSe2-on-LNO multifunctional architecture and a multiple device-based operational amplifier for module integration. Reproduced with permission [91], Copyright 2021, American Association for the Advancement of Science. (**b**) Hybrid 2D-CMOS integrated memristor chip. Reproduced with permission [93], Copyright 2023, Springer Nature. (**c**) Three-dimensional integration of 2D material-based memristor array. Reproduced with permission [11], Copyright 2023, Springer Nature.

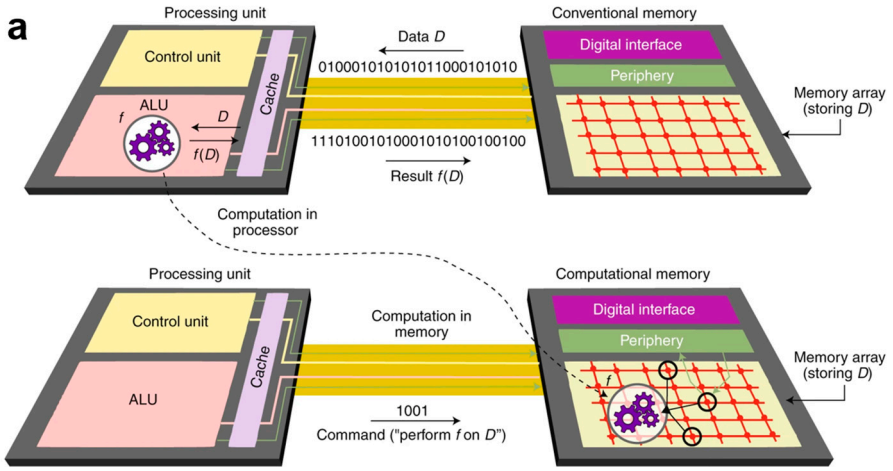
5. Two-Dimensional Non-Volatile Memory Arrays for In-Memory Computing

5.1. In-Memory Computing Architecture Mechanisms

Recent years have witnessed rapid advances in artificial intelligence and edge computing. However, the growing demands of high-performance memory devices are harder to be reached by conventional von Neumann architecture applied to most computational electronics due to the large power consumption and latency caused by information transmission processes between memory units and data processing units [96,97]. To address this problem, in-memory computing architectures are proposed and developed. For in-memory computing architectures, certain tasks of data processing are performed in the memory array, avoiding a large amount of data transmission (Figure 17a) [98]. In-memory computing architectures have the perspective to exceed the present performance limit of computational electronics [99]. Recently, most research focuses on applications of matrix-vector multiplication (MVM) based on in-memory computing architectures, as MVM is the fundamental operation of common algorithms of artificial intelligence, including perceptron and neural networks [100]. Figure 17b shows a typical architecture for in-memory computing based on RRAM, where NVM cells are aligned as an array and connected as a crossbar. Each cell stores a value of weight data (w) by its conductance (g). Input signals (x) in voltage form (V) are from bit lines (BLs), and output signals in current form (I) are detected at search lines (SLs). Word lines (WLs) controlling transistors in each cell are for data writing and weight updates. During the operation of MVM, SLs are grounded and WLs are constantly high, and the output current at the i^{th} SL according to Ohm's law is given by

$$I(i) = \sum_j g(i,j)V(j) \tag{1}$$

where i and j are serial numbers of SLs and BLs, respectively. The computation process of the array is equivalent to the MVM computation. Since devices like memristors do not have negative conductance to represent negative weight values, a commonly applied method is to double the number of cells and lines in the array, where positive cells represent positive weight values for MVM computing, and negative cells represent negative weight values. NVMs also need peripheral circuits to drive the inputs and convert output signals from the analog current form to the digital form.



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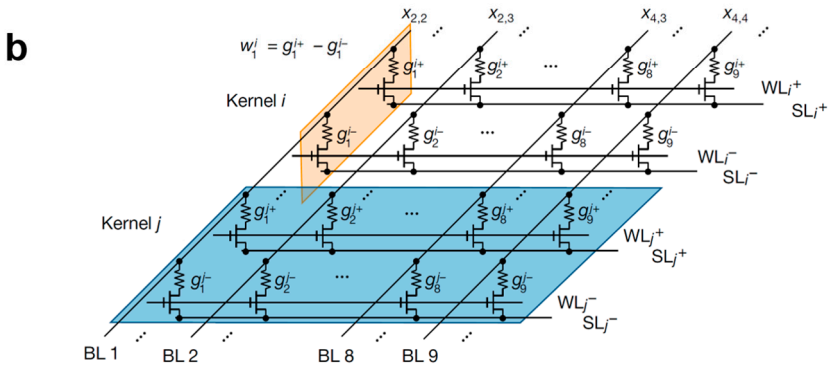
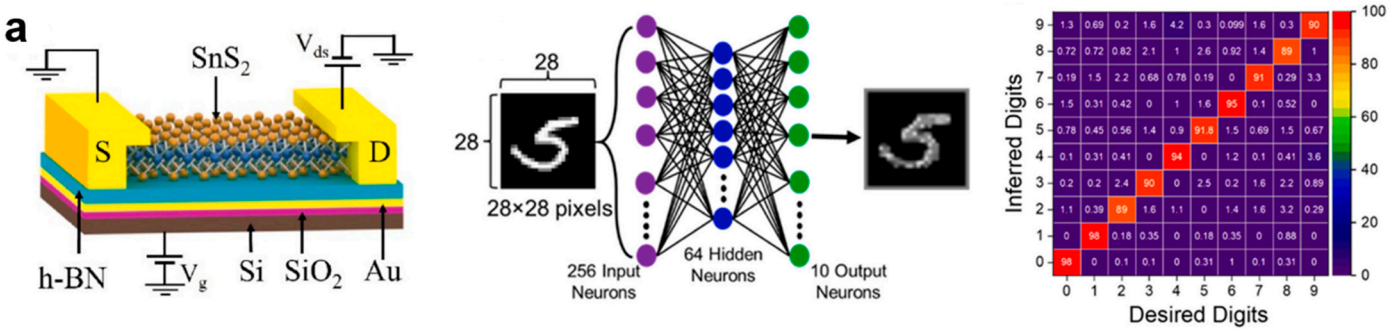


Figure 17. In-memory computing architectures: (**a**) Comparison of conventional and in-memory computing architectures. Reproduced with permission [98], Copyright 2020, Springer Nature. (**b**) Typical architecture of in-memory computing. Reproduced with permission [101], Copyright 2020, Springer Nature.

5.2. In-Memory Computing Systems

In-memory computing systems are designed to mimic the operation of human brains, where computing processes are performed in memory units [10,102,103]. Most in-memory computing systems are constructed in crossbar arrays. In-memory computing artificial intelligent systems can be used to various applications [47,96,104,105], including object recognition, robot control, financial trading, etc. Liu et al. proposed a dual-gate-controlled 2D MoS2 FET with stacked HfZrOx gates for ferroelectric programming [106]. An ANN is constructed by the device for the recognition of Iris. Khan et al. proposed a floating gate memory device based on 2D material channels and demonstrated a neural network for digit classifications with about 92% accuracy (Figure 18a) [53]. Most neural network systems by NVM devices focus on forward propagation operations. The training and weight update processes of neural networks are conducted off-line. With the increasing demand for high-performance edge computing devices, there is a trend to develop in-memory computing systems that are trained in situ [100,107]. Ning et al. reported an in situ training ferroelectric memory device system based on MoS_2 channel and a duplex structure for both training and inference operations (Figure 18b) [68]. The in situ training reaches 99.86% accuracy, and the work paves the way for NVM-based edge computing electronics for life-long learning applications. Apart from conventional crossbar architectures, array structures that are more efficient for artificial intelligence computations have been investigated. Liu et al. proposed a recirculated logic operation structure based on 2D MoS_2 transistors and $Ag/HfO_2/Pt$ filament memristors for cellular automata (CA) evolution operations (Figure 18c) [13]. The promoted structure design significantly reduces the hardware complexity for CA operations and is reported to have a 79-fold reduction in hardware costs compared to FPGA-based counterparts. An RC system is demonstrated that reaches over 96% accuracy.



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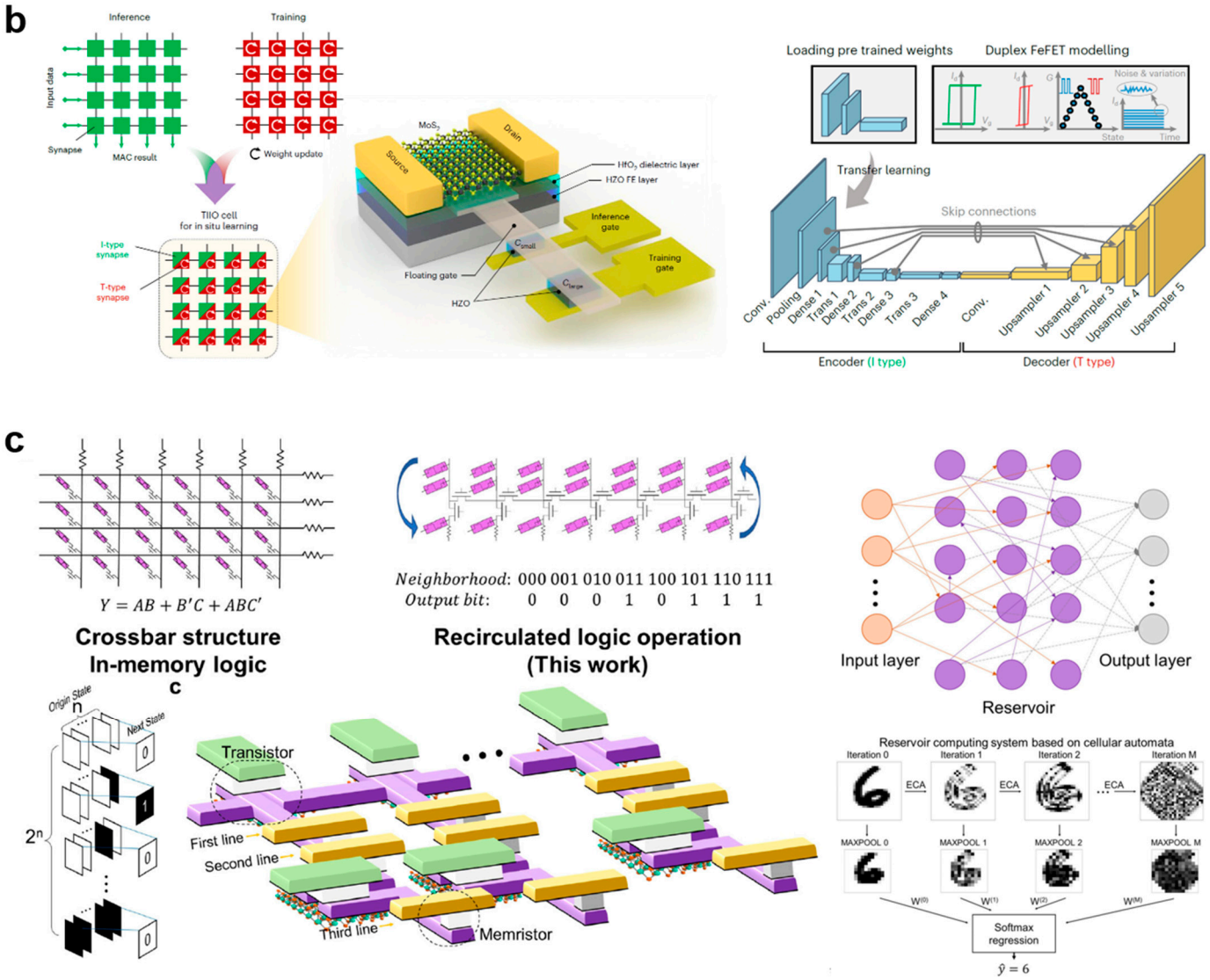

Figure 18. NVM device arrays for in-memory computing systems: (**a**) 2D floating gate memory device for artificial neural networks. Reproduced with permission [53], Copyright 2023, Elsevier Ltd. (**b**) Ferroelectric in-memory computing system with in situ learning. Reproduced with permission [68], Copyright 2023, Springer Nature. (**c**) Recirculated memristor array structure for efficient cellular automata evolution operations. Reproduced with permission [13], Copyright 2023, Springer Nature.

5.3. In-Memory Sensing and Computing Systems

The entire signal chain of edge computing vision architectures includes image data sensing, data storage, and computing. In conventional architecture, those functions are separated, and the extremely high cost of a large amount of data transmission restricts the performance of edge computing vision architectures [108]. Therefore, apart from in-memory computing architectures, in-sensor computing architectures for image data processing have been developed to accelerate operations of image sensing and processing [109,110]. Recently, vision systems combining in-memory sensing and computing have been developed, realizing the integration of the entire signal chain. Zhang et al. proposed a retinomorphic device based on 2D heterostructures and floating gate structures. The non-volatile hole and electron storage capability of the WSe_2 floating gate enables the programming of the BP channel junction and thereby controls the direction of the photocurrent response by optical signals (Figure 19a) [111]. An integrated system for optical perception, memory, and computation is constructed. Wu et al. reported an integrated in-memory sensing and computing

system based on ferroelectric-defined reconfigurable homojunctions (Figure 19b) [92]. The polarity direction of the WSe_2 channel junction is defined by the ferroelectric gate, and the number of weight states is over 51 (>5 bit). Touch is another important type of sense apart from vision. Tactile in-memory sensing and computing has been investigated in recent years [112,113]. Mo et al. developed a multi-terminal MoS2 transistor with a Au nanoparticle floating gate and constructed an integrated neuromorphic system for tactile sensing and synaptic plasticity computing [114].

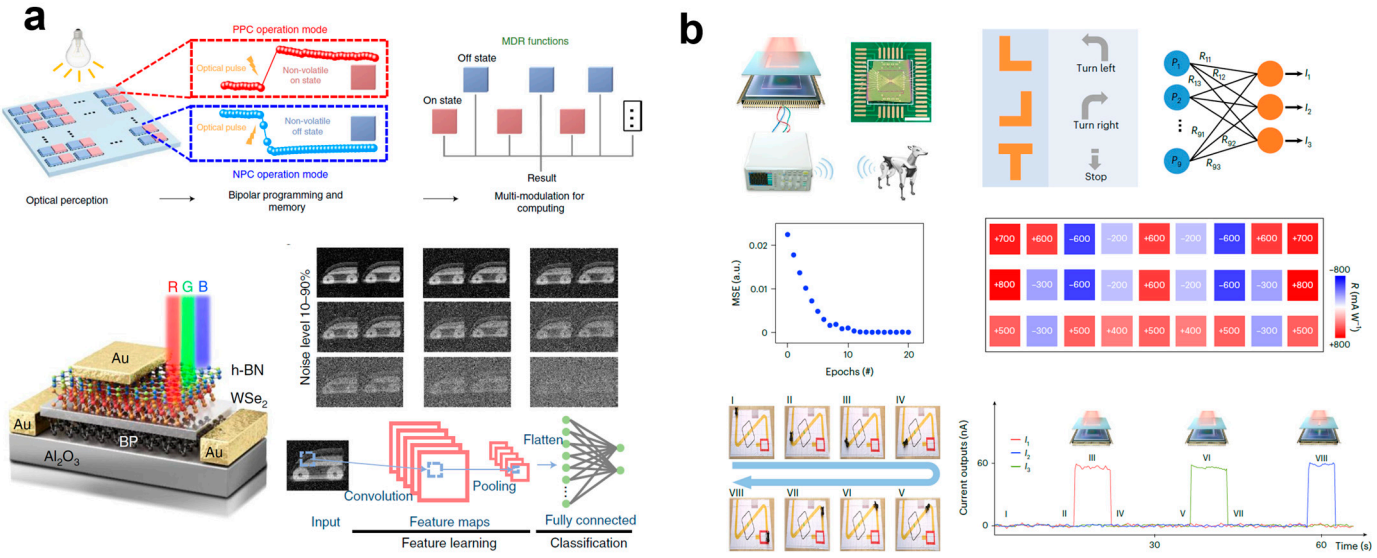

Figure 19. In-memory computing and sensing systems based on 2D NVMs: (**a**) 2D heterostructures and floating gate structure-based retinomorphic device for integrated optical perception, memory, and computation. Reproduced with permission [111], Copyright 2022, Springer Nature. (**b**) Ferroelectric-defined reconfigurable 2D homojunctions for integration of in-memory sensing and computing. Reproduced with permission [92], Copyright 2023, Springer Nature.

6. Conclusions and Outlooks

NVM devices are promising for constructing advanced memory systems. Two-dimensional material-based NVMs have improved performance and extended functionalities, and are candidates for next-generation memory electronics. Two-dimensional NVMs have been developed for functional integration, including in-memory computing and in-sensor computing systems, and the combination systems of the entire signal chain. This review discussed 2D materials with different properties, NVM devices based on 2D materials, performance criteria of 2D NVMs, and the integration of 2D NVM arrays for in-memory computing systems. In the future, novel 2D materials with more advanced performance and new properties have the potential to be explored; NVM devices should be improved by novel 2D materials with more advanced performance, alongside innovative structures for lower power consumption, larger data retention, faster data setting and resetting, and higher integration levels. Moreover, novel operation mechanisms should be researched by improving the designs of NVM cell structures, reconstructing array circuit diagrams, and developing efficient computational system architectures for specific scenarios to exceed the present performance limit of processor systems. The functional integration of signal processing including in-memory computing and sensing needs to be further improved for higher device consistency and larger integration for practical cases. Besides vision processing systems, multisensory processing including tactile, olfactory, and acoustic in-memory sensing and computing systems needs to be developed in the future. To achieve commercialization and applications of 2D NVMs in the future, stable and large-scale production of high-performance 2D materials by large-area growth such as CVD and epitaxial growth should be developed. Fabrication processes of 2D NVMs with sufficiently high yield and integration levels should be constructed. Algorithms and system-level designs of

novel computing architectures including compute-in-memory architectures and SNNs that can fit with 2D NVM systems should also be further progressed to reach sufficiently high performance to be used in real cases.

Author Contributions: Writing—original draft preparation, J.P. and Z.W.; writing—review and editing, J.P., Z.W., B.Z., J.Y. and P.G.; supervision, T.-L.R. and Y.Y.; funding acquisition, T.-L.R. and Y.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the National Key R&D Program (2022YFB3204100, 2021YFC3002200), the National Natural Science Foundation of China (U20A20168), the Research Fund from Tsinghua University Initiative Scientific Research Program, and a grant from the Guoqiang Institute, Tsinghua University.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

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